Salvador - Bahia - Brazil
August 31st to September 4th

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- Chair's Welcome -

It is our great pleasure to welcome you to the Chip in Bahia 2015 to be held in Salvador, Bahia, from 31st August to 4th September 2015.

The Chip in Bahia 2015, organized by Federal University of Bahia-UFBA and CIMATEC, is the premier conference in South America for attendees to learn about the latest information in the Microelectronics related topics. The Chip in Bahia will be held in the Hotel Pestana.

The Chip in Bahia mission is to facilitate a rich attendee experience by providing a forum for presenting state-of-the-art technical papers in Microelectronics; bringing together managers, leading researchers from academia and industry; and students to present and discuss relevant topics in Microelectronics and exhibiting the latest products and technology solutions.

Salvador, a coastal city, capital of Bahia and first capital of Brazil in its colonial past, peculiarly placed on a graben of Bay of All Saints, is the center of Afro-Brazilian culture. The three core peoples present in Brazil foundation have harmoniously blended at Salvador. You can enjoy the local culture by visiting the colorful architecture of Pelourinho district and the many gold dressed baroque style churches, portuguese legacies. Salvador is also a paradise for tasting traditional dishes, mostly african-inspired and based on the ingredients such as dendê (palm oil) and milky coconut juice.

The Chip in Bahia 2015 is composed of six events: SBCCI 2015, SBMICRO 2015, WCAS 2015, SFORUM 2015; and PATMOS 2015 and VARI 2015, which, for the first time, take places outside Europe; and an exhibition which represents the state-of-the-art when it comes to materials, devices, components, and subsystems, as well as design and simulation software and test/measurement equipment related to microelectronics world.

The Technical Program of the Chip in Bahia is enriched by 3 keynote speakers: Prof. Jan Rabaey (University of California at Berkeley, USA) presenting Lessons from Brain Connectivity for Future Interconnect in ICs; Prof. Giovanni de Micheli (EPFL, Switzerland) presenting Majority-based Synthesis for Digital Nano-technologies and Prof. Peter Beerel (University of Southern California in Los Angeles, USA) presenting A Path towards Average-Case Silicon via Asynchronous Resilient Bundled-Data Design; by 8 invited talks and a Panel on Challenges for Semiconductor in

Brazil and 10 years of the program IC Brazil, moderated by Prof. Jacobus W. Swart.

The SBCCI 2015 has been steadily growing as an important international forum for presentation of advanced research results on leading edge aspects of integrated circuits and systems design, such as analog circuits, mixed-signal, and digital integrated circuits design, dedicated and reconfigurable architectures, CAD. The SBCCI Symposium is co-sponsored by IEEE CAS Society, ACM-SigDA, IFIP Group 10, Brazilian Computer Society (SBC) and Brazilian Microelectronics Society (SBMICRO). The SBCCI 2015 Program Committee has made a major effort to thoroughly review 98 papers which were electronically submitted. After Double-blind-reviewing, the TPC finally selected 43 papers for the final program which are distributed in 7 technical sessions. These technical sessions deal with analog design and modeling, RF circuits, CAD methods and synthesis, circuit and SoC testing, embedded systems, low power digital design, on-chip communication (networks-on-chip), and reconfigurable systems.

The SBMicro 2015 is an international forum dedicated to fabrication and modeling of microsystems, integrated circuits and devices, held annually in Brazil. The goal of the symposium is to bring together researchers in the areas of processing, materials, characterization, modeling and TCAD of integrated circuits, microsensors, microactuators and MEMS. This year SBMICRO will present 54 scientific papers distributed in 7 sessions and one poster section.

The WCAS 2015 is devoted to the presentation and discussion of design experiences with a high degree of relevance in industrial and educational contexts, as well as innovative design methodologies and applications of specific design. The main idea of the workshop is to offer the chance (primarily to industry) of pointing out to the community real-life design and technology challenges which should be addressed in the short–to-medium term. This year WCAS 2015 is presenting 25 technical papers distributed in 5 technical sessions.

The SForum 2015 is part of the Chip in Bahia Conference. The main purpose of this event is to promote the participation of students in the main Brazilian symposia in the area of Microelectronics. It provides an opportunity for the presentation and discussion of research projects developed by undergraduate students in microelectronics. This year SFORUM received 27 papers, and the Program Committee has selected 21 papers,

8 for oral sessions as well as 13 papers in a poster session.

PATMOS has a history of 25 years and it is one of the first conferences world-wide to focus on low power. The traditional scope of the PATMOS conference series has mainly been about and around the design of circuits and architectures optimized for highest performance at lowest power consumption. But meanwhile, power-efficiency has become extremely important for many more areas spreading far beyond this traditional R&D niche. Energy-efficient ICT (Information and Communication Technology) infrastructures are a key issue of local and global economies. It is the intention of PATMOS 2015 to think beyond current solutions such that the very wide gap between computation and the massive energy consumption for ICT infrastructures can be closed. This year the Program Committee has selected 26 papers which will be presented in 5 technical sessions. VARI 2015 is the 6th International Workshop on CMOS Variability. The increasing variability in CMOS transistor characteristics, as well as its sensitivity to environmental variations has become a major challenge to scaling and integration. This leads to major changes in the way that future integrated circuits and systems are designed. Strong links must be established between circuit design, system design and device technology. The VARI workshop answers to the need to have an event on variability in CMOS technology development and circuit design, where industry and academia meet. VARI objective is to provide a forum to discuss and investigate the CMOS process and environmental variability issues in methodologies and tools for the design of current and upcoming generations of integrated circuits and systems. The technical program will focus on performance and power consumption as well as architectural aspects like adaptability or resilience, with particular emphasis on modeling, design, characterization, analysis and optimization in respect to variability. This year the Program Committee has selected 13 papers which will be presented in 3 technical sessions.

The Program Committee (PC) and external reviewers worked very hard in reviewing papers and providing suggestions for their improvement, which were keys to the final program quality. All our six Program Committees have members from all regions of the world: Europe, Asia, South America and USA. The Chairs thank also our co-sponsoring societies: the IEEE Circuits and Systems Society, the ACM SigDA, the Brazilian Computer Society (SBC), the Brazilian Microelectronics Society (SBMICRO), as well as the technical co-sponsorship from IFIP Working Group 10.5. Finally, the institutional and/or financial support provided by the local public funding agencies (CAPES, CNPq)

and by the industrial sponsors is gratefully acknowledged which are presenting their tools, projects, products and commercial possibilities for all community.

Special thanks go to the authors that spent precious time on the preparation of their works. We deeply thank the six Program Committees, the keynotes and invited talk speakers, and also the members of the various meeting committees and reviewers, panelists and chairs. The volunteers at the Conference Secretariat from UFBA and CIMATEC, and students deserve our appreciation for their dedication to the Organization. We hope that you enjoy the Chip in Bahia 2015 technical and social programs, which were carefully prepared for you.

The entire Chip in Bahia 2015 Organizing Committee is looking forward to seeing you and extending our hands for a warm welcome!

See you soon!

Robson Nunes de Lima,
Chip in Bahia 2015 General Chair

- Fringe and Social Meetings -

Monday, August 31st

Registration
13:40 h - 17:00 h

SBMicro Meeting
Room: Florbela Spanca
13:40 h - 15:20 h

SBCCI Meeting
Room: Florbela Spanca
15:40 h - 17:00 h

SBMicro and SBCCI Steering
Room: Florbela Spanca
17:00 h - 18:00 h

Tuesday, September 1st

Registration
08:00 h - 08:40 h

Opening
Room: Fernando Pessoa 1 & 2
18:00 h - 18:20 h

SBmicro Awards
Room: Fernando Pessoa 1 & 2
18:20 h - 18:40 h

Reception and Cocktail
Foyer S1
18:40 h - 21:00 h

Wednesday, September 2nd

Registration
08:00 h - 08:40 h

CA-ME CNPq Meeting
Room: Fernando Pessoa 1
18:00 h - 19:00 h

CECCI / SBC Assembly
Room: Fernando Pessoa 3
18:00 h - 19:00 h

SBmicro Assembly
Room: Fernando Pessoa 3
19:00 h - 20:00 h

Thursday, September 3rd

CI Brazil Meeting
Room: Zélia Gatai 1
14:00 h - 17:20 h

IEEE CEDA Brazil Chapter Meeting
Room: Luandino Vieira
10:00 h - 12:00 h

Conference Dinner
19:20 h

Friday, September 4th

Best Papers Awards
Room: Fernando Pessoa 1 & 2
16:00 h - 16:20 h

Closing Ceremony
Room: Fernando Pessoa 1 & 2
16:20 h - 16:40 h

- Chip in Bahia KEYNOTES -

Wednesday September 2nd
08:40 h - 09:40 h

Room: Fernando Pessoa 1 & 2

The Human Intranet - Where Swarms and Humans meet ou Lessons from Brain Connectivity for Future Interconnect in ICs
JAN RABAEY
University of California at Berkeley (UCB)

Thursday September 3rd
08:40 h - 09:40 h

Room: Fernando Pessoa 1 & 2

Majority-based synthesis for digital nano-technologies
GIOVANNI DE MICHELI
École Polytechnique Fédérale de Lausanne (EPFL)

Friday September 4th
08:40 h - 09:40 h

Room: Fernando Pessoa 1 & 2

A Path towards Average-Case Silicon via Asynchronous Resilient Bundled-Data Design
PETER BEEREL
University of Southern California (USC) in Los Angeles

- Chip in Bahia PANEL -

Thursday September 3rd
17:20 h - 19:00 h

Room: Fernando Pessoa 1 & 2
Moderator: Jacobus W. Swart

Challenges for Semiconductor in Brazil and 10 years of the program IC Brazil

- SBCCI 2015 -

28th Symposium on Integrated Circuits and Systems Design

SBCCI is an international forum dedicated to integrated circuits and systems design, test and electronic design automation (EDA), held annually in Brazil. The 28th SBCCI will take place in Salvador, capital of the State of Bahia.

The goal of the symposium is to bring together researchers in the areas of EDA, design and test of integrated circuits and systems. The scope of the symposium includes technical sessions, tutorials and panels, as well as an exhibition and working group meetings.

The best papers presented at the symposium will be invited to resubmit an extended version to be considered for publication at the IEEE Design & Test and at the JICS - Journal of Integrated Circuits and Systems.

- 28th SBCCI 2015 -

-- Committees --

General Chair

Robson Nunes de Lima | *UFBA, Brazil* | *delima@ufba.br*

Program Chairs

Ana Isabela Araújo Cunha | *UFBA, Brazil* | *aisacunha@gmail.com*

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Latin America Liaison

Victor Grimblatt | *Synopsys, Chile*

IEEE Design&Test Liaison

Yervant Zorian | *Synopsys, USA*

- Tutorials -

Tuesday, September 1st

Room: Fernando Pessoa 2

Tutorial 1

8:40 h - 10:20 h
Low Power Design Essentials
JAN RABAEY
University of California at Berkeley - UCB

Coffee Break & Exhibitors
10:20 h - 10:40 h

Tutorial 2

10:40 h - 12:20 h
Ultra-Low-Voltage (ULV) IC Design: Designing for VDD below kT/q
MÁRCIO CHEREM SCHNEIDER
Universidade Federal de Santa Catarina - UFSC

Lunch
12:20 h - 14:00 h

Tutorial 3A

13:40 h - 15:20 h
Impact of Low Frequency Noise on the Reliability and Variability of Nano CMOS devices
JALAL JOMAAH
Institut National Polytechnique de Grenoble - INPG, France; Lebanese University

Coffee Break & Exhibitors
15:20 h - 15:40 h

Tutorial 4A

15:40 h - 17:20 h
Cyber - Physical Systems: Reality, Dreams and Fantasy
MAGDY A. BAYOUMI
University of Louisiana at Lafayette

Room: Fernando Pessoa 3

Tutorial 3B

13:40 h - 15:20 h
3D ICs - Moving from silicon to heterogeneous technologies
MACIEJ OGORZALEK
Jagiellonian University, Krakow, Poland

Coffee Break & Exhibitors
15:20 h - 15:40 h

Tutorial 4B

15:40 h - 17:20 h
Low Loss, High Isolation, Linear RF Switch Design in SOI
PETER H. POPPLEWELL
Skyworks Solutions

- Technical Sessions -

Wednesday, September 2nd

Coffee Break & Exhibitors
09:40 h - 10:00 h

Session 1A –Digital, Reconfigurable and Applications
Wednesday, 10:00 h – 11:40 h

Chair: Ney Laert Vilar Calazans
Room: Fernando Pessoa 2

10:00 h – 10:20 h
DESIGNING CMOS FOR NEAR-THRESHOLD MINIMUM-ENERGY OPERATION AND EXTREMELY WIDE V-F SCALING
André Luís Rodeghiero Rosa, Leonardo Bandeira Soares, Kleber Hugo Stangherlin and Sergio Bampi

10:20 h – 10:40 h
ANALYSIS OF SUPPLY VOLTAGE SCALING ON SDDS-NCL DESIGNS
Ricardo Aquino Guazzelli, Matheus Trevisan Moreira, Ney Laert Vilar Calazans and Fernando Gehm Moraes

10:40 h – 11:00 h
MCML GATE DESIGN FOR STANDARD CELL DESIGN
Bruno Canal, Cicero Nunes, Renato Ribas and Eric Fabris

11:00 h – 11:20 h
MINIMIZATION AND ENCODING OF HIGH PERFORMANCE ASYNCHRONOUS STATE MACHINES BASED ON GENETIC ALGORITHM
Tiago Curtinhas, Duarte Lopes Oliveira, Lester de Abreu Faria, Osamu Saotome and Tassio Cortes Cavalcanti

11:20 h – 11:40 h
A FRAMEWORK FOR MULTI-FPGA INTERCONNECTION USING MULTI GIGABIT TRANSCEIVERS
Michael Dreschmann, Jan Heisswolf, Michael Geiger, Manuel Haussecker and Juergen Becker

Session 1B – Analog & RF & Mixed Signal
Wednesday, 10:00 h – 11:40 h

Chair: Hamilton Klimach
Room: Zélia Gatai 1

10:00 h – 10:20 h
A CURRENT LIMITER FOR LINEAR REGULATORS BASED ON POWER-DISSIPATION THRESHOLD
Jader A. De Lima and Wallace A. Pimenta

10:20 h – 10:40 h
HIGH PSRR NANO-WATT MOS-ONLY THRESHOLD VOLTAGE MONITOR CIRCUIT
Jhon Alexander Gómez Caicedo, Hamilton Klimach, Eric Fabris and Oscar Elisio Mattia

10:40 h – 11:00 h
DESIGN OF HIGH-VOLTAGE LEVEL SHIFTERS BASED ON STACKED STANDARD TRANSISTORS FOR A WIDE RANGE OF SUPPLY VOLTAGES
Sara Pashmineh and Dirk Killat

11:00 h – 11:20 h
0.5 V SUPPLY RESISTORLESS VOLTAGE REFERENCE FOR LOW VOLTAGE APPLICATIONS
Renato Campana, Hamilton Klimach and Sergio Bampi

11:20 h – 11:40 h
0.5 V SUPPLY VOLTAGE REFERENCE BASED ON THE MOSFET ZTC CONDITION
David Cordova, Pedro Toledo, Hamilton Klimach, Sergio Bampi and Eric Fabris

Lunch
11:40 h - 13:20 h

Invited Talk 1
Wednesday, 13:20 h – 14:00 h

Room: Fernando Pessoa 2

Frame Free Vision
TERESA SERRANO-GOTARREDONA
IMSECNM-CSIC, Sevilla; University of Sevilla

Session 2 – SoC, NoC, Embedded
Wednesday, 14:00 h – 15:20 h

Chair: Fernando Gehm Moraes
Room: Fernando Pessoa 2

14:00 h – 14:20 h
A LOW-AREA AND HIGH-THROUGHPUT INTRA PREDICTION ARCHITECTURE FOR A MULTI-STANDARD HEVC AND H.264/AVC VIDEO ENCODER
Marcel Corrêa, Marcelo Porto, Bruno Zatt and Luciano Agostini

14:20 h – 14:40 h
MEMORY-AWARE AND HIGH-THROUGHPUT HARDWARE DESIGN FOR THE HEVC FRACTIONAL MOTION ESTIMATION
Vladimir Afonso, Henrique Maich, Luan Audibert, Bruno Zatt, Marcelo Porto and Luciano Agostini

14:40 h – 15:00 h
REAL-TIME ARCHITECTURE FOR HEVC MOTION COMPENSATION SAMPLE INTERPOLATOR FOR UHD VIDEOS
Wagner Penny, Guilherme Paim, Marcelo Porto, Luciano Agostini and Bruno Zatt

15:00 h – 15:20 h
A DISTRIBUTED ENERGY-AWARE TASK MAPPING TO ACHIEVE THERMAL BALANCING AND IMPROVE RELIABILITY OF MANY-CORE SYSTEMS
Marcelo Mandelli, Guilherme Castilhos, Luciano Ost, Gilles Sassatelli and Fernando Moraes

Coffee Break & Exhibitors
15:20 h - 15:40 h

Session 3 – CAD, Verification & Test
Wednesday, 15:40 h – 18:00 h

Chair: Gilson Inácio Wirth
Room: Fernando Pessoa 2

15:40 h – 16:00 h
OPTIMUM OPERATING POINTS OF TRANSISTORS WITH MINIMAL AGING-AWARE SENSITIVITY
Nico Hellwege, Nils Heidmann, Steffen Paul and Dagmar Peters-Drolshagen

16:00 h – 16:20 h
A NOVEL METHODOLOGY FOR ROBUSTNESS ANALYSIS OF QCA CIRCUITS
Dayane Reis and Frank Sill Torres

16:20 h – 16:40 h
EVALUATING GEOMETRIC ASPECTS OF NON-SERIES-PARALLEL CELLS
Maicon Cardoso, Leomar Rosa Junior and Felipe Marques

16:40 h – 17:00 h
INCREASING OBSERVABILITY IN POST-SILICON DEBUG USING ASYMMETRIC OMEGA NETWORKS
André Gomes, Fredy Alves, Ricardo Ferreira and José Nacif

17:00 h – 17:20 h
POWER-AWARE DESIGN OF ELECTRONIC SYSTEM LEVEL USING INTEROPERATION OF HYBRID AND DISTRIBUTED SIMULATIONS
Helder F. A. Oliveira, Alisson V. Brito, Elmar U. K. Melcher, Harald Bucher, Joseana M. F. R. Araújo, Liana D. Duenha and Rodolfo J. Azevedo

17:20 h – 17:40 h
JEZZ: AN EFFECTIVE LEGALIZATION ALGORITHM FORMINIMUM DISPLACEMENT
Julia Puget, Guilherme Flach, Marcelo Johann and Ricardo Reis

17:40 h – 18:00 h
A PARALLEL STRUCTURE FILTER DESIGN IN MODIFIED LUCY-RICHARDSON DECONVOLUTION ALGORITHM FOR INVERSELY ANALYZING COMPLEX-SHAPED RTN LONG TAIL EFFECTS
Hiroyuki Yamauchi and Worawit Somha

Thursday, September 3rd

Coffee Break & Exhibitors
09:40 h - 10:00 h

Session 4 – Analog & RF & Mixed Signal
Thursday, 10:00 h – 11:40 h

Chair: Fernando Rangel de Sousa
Room: Fernando Pessoa 2

10:00 h – 10:20 h
OPTIMIZATION DESIGN METHODOLOGY FOR A 460-MHZ-GBW AND 80-DB-SNR LOW-POWER CURRENT-MODE AMPLIFIER
Pietro Maris Ferreira, Anthony Kolar and Philippe Bénabès

10:20 h – 10:40 h
LOW POWER, HIGH-SENSITIVITY CLOCK RECOVERY CIRCUIT FOR LF/HF RFID APPLICATIONS
Rafael Cantalice, Fernando Paixão Cortes and Alexandre Simionovski

10:40 h – 11:00 h
DESIGN OF 28 NM CMOS INTEGRATED TRANSFORMERS FOR A 60 GHZ POWER AMPLIFIER
Bernardo Leite, Eric Kerhervé and Didier Belot

11:00 h – 11:20 h
ANALYSIS AND DESIGN OF A MOS RF ENVELOPE DETECTOR IN ALL INVERSION REGIONS
Linder Reyes and Fernando Silveira

11:20 h – 11:40 h
A 25-DBM 1-GHZ POWER AMPLIFIER INTEGRATED IN CMOS 180NM FOR WIRELESS POWER TRANSFERRING
Fabian L. Cabrera and F. Rangel de Sousa

Lunch
11:40 h - 13:20 h

Invited Talk 2
Thursday, 13:20 h – 14:00 h

Room: Fernando Pessoa 2

System-Level Design of Heterogeneous System-on-Chip Architectures
LUCA CARLONI
Columbia University, EUA

Session 5 – SoC, NoC, Embedded
Thursday, 14:00 h – 15:20 h

Chair: Fernanda Lima Kastensmidt
Room: Fernando Pessoa 2

14:00 h – 14:20 h
RECONFIGURABLE GROUP-WISE SECURITY ARCHITECTURE FOR NOC–BASED MPSOCS PROTECTION
Daniel Florez, Guy Gogniat and Martha Johanna Sepulveda

14:20 h – 14:40 h
SMART RECONFIGURATION APPROACH FOR FAULT-TOLERANT

NOC BASED MPSOCS
Jarbas Silveira, Lucas Brahm, Rafael Mota, Alan Cadore, Ramon Fernandes, Cesar Marcon and Paulo Cortez

14:40 h – 15:00 h
PHICIT - IMPROVING HIERARCHICAL NETWORKS-ON-CHIP THROUGH 3D SILICON PHOTONICS INTEGRATION
Cezar Reinbrecht, Martha Johanna Sepúlveda and Altamiro Susin

15:00 h – 15:20 h
LATENCY IMPROVEMENT WITH TRAFFIC FLOW ANALYSIS IN A 3D NOC UNDER MULTIPLE FAULTY TSVS SCENARIO
Anelise Kologeski, Henrique Colao Zanuz and Fernanda Lima Kastensmidt

Coffee Break & Exhibitors
15:20 h - 15:40 h

Session 6 – Analog & RF & Mixed Signal
Thursday, 15:40 h – 17:00 h

Chair: Luciano Volcan Agostini
Room: Fernando Pessoa 2

15:40 h – 16:00 h
WIDEBAND LOW NOISE VARIABLE GAIN AMPLIFIER
Filipe Baumgratz, Hao Li, Sergio Bampi and Carlos Saavedra

16:00 h – 16:20 h
A 2-DECADES WIDEBAND LOW-NOISE AMPLIFIER WITH HIGH GAIN AND ESD PROTECTION
Arthur Liraneto Torres Costa, Hamilton Klimach and Sergio Bampi

16:20 h – 16:40 h
CMOS TRANSCONDUCTOR ANALYSIS FOR LOW TEMPERATURE SENSITIVITY BASED ON THE ZTC MOSFET CONDITION
Pedro Toledo, Hamilton Klimach, David Cordova, Sergio Bampi and Eric Fabris

16:40 h – 17:00 h
DESIGN AND OPTIMIZATION OF HIGH SENSITIVITY TRANSIMPEDANCE AMPLIFIERS IN 0.13 UM CMOS AND BICMOS TECHNOLOGIES FOR HIGH SPEED OPTICAL RECEIVERS
André Ponchet, Ezio Bastida, Roberto Panepucci, Jacobus Swart and Celio Finardi

Friday, September 4rd

Coffee Break & Exhibitors
09:40 h - 10:00 h

Session 7 – Analog & RF & Mixed Signal
Friday, 10:00 h – 11:40 h

Chair: Yuri Sebastian Catunda
Room: Fernando Pessoa 2

10:00 h – 10:20 h
SYSTEM-LEVEL DESIGN OF SINGLE-BIT SIGMA-DELTA MODULATORS BASED ON MSA AND SNR DATA GRAPHICS
Raphael Viera, Jorge de la Cruz, André Luiz Aita, César Augusto Prior and João Baptista Martins

10:20 h - 10:40 h
DIRECT FEEDBACK TOPOLOGY FOR REDUCING RESIDUAL VOLTAGE IN FUNCTIONAL ELECTRICAL STIMULATION
Lucas Teixeira, Cesar Rodrigues and César Prior

10:40 h - 11:00 h
ANALYSIS AND SYSTEM-LEVEL DESIGN OF A HIGH RESOLUTION INCREMENTAL ∑Δ ADC FOR BIOMEDICAL APPLICATIONS
Antonio Soares, Diomadson Belfort, Sebastian Catunda, Raimundo Carlos Silvério Freire

11:00 h - 11:20 h
NOVEL COMPACT ACTIVE DUAL RESPONSE FILTER WITHIN A SINGLE DEVICE
Raafat Lababidi, Frédéric Le Roy, Denis Le Jeune, Ali Mansour, Julien Lintignat and Ali Louzir

11:20 h - 11:40 h
EFFECTIVE CROSS COMPARISON OF MISMATCH EFFECTS ON DIFFERENT LOGARITHMIC PIXEL SENSOR TOPOLOGIES
Ewerton Gomes de Oliveira, Carlos Augusto de Moraes Cruz and Davies William de Lima Monteiro

Lunch
11:40 h - 13:20 h

Invited Talk 3
Friday, 13:20 h – 14:00 h

Room: Fernando Pessoa 2

Device-Circuit Co-design of Multi-Gate FETs in sub-10nm Technologies
KAUSHIK ROY
Purdue University, EUA

Session 8 – Digital, Reconfigurable and Applications
Friday, 14:00 h – 15:20 h

Chair: Ivan Saraiva Silva
Room: Fernando Pessoa 2

14:00 h – 14:20 h
DIFFERENTIAL EVOLUTION TO REDUCE ENERGY CONSUMPTION IN THREE-LEVEL MEMORY HIERARCHY
Abel Silva-Filho and Leonardo Nunes

14:20 h – 14:40 h
IPNOSYS II - A NEW ARCHITECTURE FOR IPNOSYS PROGRAMMING MODEL
Thiago Rodrigues, Ivan Silva and Silvio Fernandes

14:40 h – 15:00 h
IMPROVING THE STATISTICAL VARIABILITY OF DELAY-BASED PHYSICAL UNCLONABLE FUNCTIONS
Jefferson Capovilla, Mario Cortes and Guido Araujo

15:00 h – 15:20 h
RUN-TIME CACHE CONFIGURATION FOR THE LEON-3 EMBEDDED PROCESSOR
Bruno Silva, Lucas Cuminato, Pedro Diniz and Vanderlei Bonato

- SBMicro 2015 -

30th Symposium on Microelectronics Technology and Devices

The SBMicro symposium is an international forum dedicated to fabrication and modeling of microsystems, integrated circuits and devices, held annually in Brazil.

The goal of the symposium is to bring together researchers in the areas of processing, materials, characterization, modeling and TCAD of integrated circuits, microsensors, microactuators and MEMS.

The SBMicro2015 will be located in Salvador, Bahia. This international conference offers a unique blend of microelectronics and serves as a major conference for the discussion of interdisciplinary research around the world through a variety of formats, such as oral presentations, poster sessions, exhibits, panel discussions, and tutorial sessions.

The best papers presented at the symposium will be invited to resubmit an extended version that will be considered for publication at the JICS - Journal of Integrated Circuits and Systems.

- 30th SBMicro 2015 -

-- Committees --

General Chair

Robson Nunes de Lima | *UFBA, Brazil* | *delima@ufba.br*

Program Chairs

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Marcelo Antonio Pavanello | *FEI, Brazil*

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Cor Claeys | *IMEC, Belgium*

Americas Liaison

Fernando Guarin | *IBM, USA*

- Tutorials -

Tuesday, September 1st

Room: Fernando Pessoa 1

Tutorial 1

8:40 h - 10:20 h
Field Effect Transistor: From MOSFET to Tunnel FET
JOÃO ANTONIO MARTINO
Universidade de São Paulo - USP, Brazil

Coffee Break & Exhibitors
10:20 h - 10:40 h

Tutorial 2

10:40 h - 12:20 h
Revisiting Diode and Solar Cell Extraction Methods
ADELMO ORTIZ-CONDE
Universidad Simon Bolivar, Venezuela

Lunch
12:20 h - 14:00h

Tutorial 3

13:40 h - 15:20 h
More , Beyond and More than Moore meeting for 3D
SIMON DELEONIBUS
CEA-Leti, France

Coffee Break & Exhibitors
15:20 h - 15:40 h

Tutorial 4

15:40 h - 17:20 h
Trends and challenges in Nano-electronic Technologies for New Device Concepts
RITA ROOYACKERS
IMEC, Belgium

- Technical Sessions -

Wednesday, September 2nd

Coffee Break & Exhibitors
09:40 h - 10:00 h

Session 1 – Semiconductor Devices
Wednesday, 10:00 h – 12:00 h

Chair: Michelly de Souza, FEI, Brazil
Room:Fernando Pessoa 1

10:00 h – 10:20 h
DYNAMIC THRESHOLD VOLTAGE INFLUENCE ON GE PMOSFET HYSTERESIS
Alberto Oliveira, Paula Agopian, João Martino, Eddy Simoen, Cor Claeys, Hans Mertens, Nadine Collaert and Aaron Thean

10:20 h – 10:40 h
APPARENT SCHOTTKY BARRIER HEIGHT OF MIS NI/SIC DIODES
Ivan Kaufmann, Marcelo Pereira and Henri Boudinov

10:40 h – 11:00 h
ASYMMETRIC SELF-CASCODE VERSUS GRADED-CHANNEL SOI NMOSFETS FOR ANALOG APPLICATIONS
Rafael Assalti, Marcelo Antonio Pavanello, Denis Flandre and Michelly de Souza

11:00 h – 11:20 h
BACK ENHANCED (BE) SOI PMOSFET
Ricardo Rangel and Joao Martino

11:20 h – 11:40 h
HEIGHTENING THE ELECTRICAL PERFORMANCE OF MOSFET SWITCHES BY APPLYING ELLIPSOIDAL LAYOUT STYLE
Marcello Marcelino Correia and Salvador P. Gimenez

11:40 h – 12:00 h
RELIABILITY OF FILM THICKNESS EXTRACTION THROUGH CV CURVES OF SOI P-I-N GATED DIODES
Katia Sasaki, Carlos Navarro, Maryline Bawedin, François Andrieu, Joao Martino and Sorin Cristoloveanu

Lunch
12:00 h - 13:20 h

Invited Paper 1
Wednesday, 13:20 h – 14:00 h

Room: Fernando Pessoa 1

CMOS-Compatible Spintronic Devices
Viktor Sverdlov, Joydeep Ghosh, Alexander Makarov, Thomas Windbacher, and Siegfried Selberherr

Session 2 – Device Physics and Modeling
Wednesday, 14:00 h – 15:20 h

Chair: Gilson Inácio Wirth, UFRGS, Brazil
Room:Fernando Pessoa 1

14:00 h – 14:20 h
MODELLING OF DARK CURRENT IN ALGAAS/GAAS QWIPS
Diogo de Moura Pedroso and Angelo Passaro

14:20 h – 14:40 h
IMPACT OF TEMPERATURE ON ELECTROMIGRATION LIFETIME EXTRAPOLATION
Roberto Lacerda de Orio

14:40 h – 15:00 h
LIMITATIONS OF COUPLED MODE THEORY TO MODEL COUPLED MICRORESONATORS "DARK STATES"
Guilherme de Rezende, Mario Souza and Newton Frateschi

15:00 h – 15:20 h
NUMERICAL EVALUATION OF WARPAGE IN POP ENCAPSULATED SEMICONDUCTORS
Fabiano Alex Colling, Celso Renato Peter, Carlos Alberto Mendez Moraes, Eduardo Luiz Rhod, Willyan Hasenkamp Carreira, Dong-Hyun Park and Tae Sung Oh

Coffee Break & Exhibitors
15:20 h - 15:40 h

Session 3 – Fabrication Technology
Wednesday, 15:40 h – 17:40 h

Chair: José Alexandre Diniz, Unicamp, Brazil
Room:Fernando Pessoa 1

15:40 h – 16:00 h
SPACER LITHOGRAPHY FOR 3D MOS DEVICES USING AMOR-

PHOUS SILICON DEPOSITED BY ECRCVD
Andressa Rosa, José Diniz, Ioshiaki Doi, Mara Canesqui, Alfredo Vaz and Marcos dos Santos

16:00 h – 16:20 h
DEVELOPMENT OF MCM-D TECHNOLOGY WITH PHOTOSENSITIVE BENZOCYCLOBUTENE
Cristina Adamo, Alexander Flacker, Hercílio Cavalcanti, Ricardo Teixeira, Antônio Rotondaro and Leandro Manera

16:20 h – 16:40 h
CHARACTERIZATION OF HFO2 ON HAFNIUM-INDIUM-ZINC OXIDE HIZO LAYER METAL-INSULATOR- SEMICONDUCTOR STRUCTURES DEPOSITED BY RF SPUTTERING
Isai Hernandez, Magali Estrada, Ivan Garduño, Julio Tinoco and Antonio Cerdeira

16:40 h – 17:00 h
INVESTIGATIONS OF CAPACITIVELY-COUPLED PLASMAS BY ELECTROSTATIC PROBE TECHNIQUE
Giuseppe Cirino, Raul Castro, Marcelo Pisani, Patrick Verdonck, Ronaldo Mansano, Marcos Massi, Rodrigo Pessoa, Luis Alberto Barea, Tayeb Brahim and Homero Maciel

17:00 h – 17:20 h
REACTIVE SPUTTERING OF SIXNY FOR MONOS MEMORY FABRICATION
Matheus Adam, Artur Coelho, Marcelo Pereira and Henri Boudinov

17:20 h – 17:40 h
FROM INAS EXTENDED MONOLAYER FLAT 2D TERRACES TO 3D ISLANDS GROWN ON GAAS SUBSTRATES
Guilherme Torelly, Roberto Jakomin, Mauricio P. Pires, Luciana P. Dornelas, Rodrigo Prioli, Paula G. Caldas, Hongen Xie, Fernando A. Ponce and Patricia L. Souza

Thursday, September 3rd

Coffee Break & Exhibitors
09:40 h - 10:00 h

Session 4 – Devices and Circuits
Thursday, 10:00 h – 12:00 h

Chair: Salvador Gimenez, FEI, Brazil
Room:Fernando Pessoa 1

10:00 h – 10:20 h
USE OF BACK GATE BIAS TO ENHANCE THE ANALOG PERFORMANCE OF PLANAR FD AND UTBB SOI TRANSISTORS-BASED SELF-CASCODE STRUCTURES
Rodrigo Doria, Denis Flandre, Renan Trevisoli, Michelly de Souza and Marcelo Pavanello

10:20 h – 10:40 h
EFFECT OF CHANNEL DOPING CONCENTRATION ON THE HARMONIC DISTORTION OF ASYMMETRIC N- AND P-TYPE SELF-CASCODE MOSFETS
Lígia d'Oliveira, Rodrigo Doria, Marcelo Pavanello, Denis Flandre and Michelly de Souza

10:40 h – 11:00 h
PERFORMANCE COMPARISON BETWEEN TFET AND FINFET DIFFERENTIAL PAIR
Marcio Martino, João Martino and Paula Agopian

11:00 h – 11:20 h
DESIGN AND COMPARATIVE PERFORMANCE SIMULATION OF RHBD INVERTER CELLS IN 180NM CMOS
Pablo Vaz

11:20 h – 11:40 h
COMPARATIVE ANALYSIS OF 350NM CMOS ACTIVE PIXEL SENSOR ELECTRONICS
Lidiane Costa, Artur Mello, Luciana Salles and Davies William Monteiro

11:40 h – 12:00 h
WIRELESS TRANSDUCER BASED ON SPLIT-RING RESONATOR
Roddy Alexander Romero, Renato Feitoza, Carlos Renato Rambo and Fernando Rangel de Sousa

Lunch
12:00 h - 13:20 h

Invited Paper 2
Thursday, 13:20 h – 14:00 h

Room: Fernando Pessoa 1

The smaller the noisier? Low Frequency Noise Diagnostic of Advanced Semiconductor Devices
C. Claeys, E. Simoen, P.G.D. Agopian, J.A. Martino, M. Aoulaiche, B. Cretu, W. Fang, R. Rooyackers, A. Vandooren, A. Veloso, M.

Jurczak, N. Collaert and A. Thean

Flash Presentation and Poster Session
Thursday, 14:00 h – 15:20 h

Chair: Marcelo Antonio Pavanello, FEI, Brazil
Room: Fernando Pessoa 1 & Foyer S1

ELECTRICAL AND OPTICAL BEHAVIOR OF ZNO NANOWIRES IRRADIATED BY HIGH-ENERGY IONS
C. I. L. Sombrio, A. L. F. Cauduro, P. L. Franzen, H. I. Boudinov and D. L. Baptista

FABRICATION OF 60 CHANNEL MICROELECTRODE ARRAYS FOR FUTURE USE WITH CULTURED NEURONAL NETWORKS
Vanessa Gomes, Angelica Barros, João Filho,
Sergio Martinoia, Alberto Pasquarelli and Jacobus Swart

ROLE OF THE EXTENSIONS IN DOUBLE-GATE JUNCTIONLESS MOSFETS IN THE DRAIN CURRENT AT HIGH GATE VOLTAGE
Antonio Cerdeira, Fernando Ávila, Bruna Cardoso, Magali Estrada and Marcelo Pavanello

PHOTOACTIVE THIN FILMS BASED ON BENZOXAZOLE DERIVATIVES
Louise Etcheverry, Fabiano Rodembusch, Henri Boudinov, André Gündel and Eduardo Moreira

FATIGUE ANALYSIS OF IC PACKAGING
Vanessa Davanço Pereira de Lima and Antônio Luis Pacheco Rotondaro

PRODUCTION OF YB3+/ER3+ CODOPED PBO-GEO2 PEDESTAL TYPE WAVEGUIDES FOR PHOTONIC APPLICATIONS
Francisco Bomfim, Davinson da SIlva, Vanessa Del Cacho, Luciana Kassab and Marco Alayo

ON THE ORIGIN OF LOW-FREQUENCY NOISE OF SUBMICRON GRADED-CHANNEL FULLY DEPLETED SOI NMOSFETS
Allan Molto, Rodrigo Doria, Michelly Souza and Marcelo Pavanello

GROUND PLANE INFLUENCE ON UTBB SOI NMOSFET ANALOG PARAMETERS
Vitor Itocazu, Victor Sonnenberg, Eddy Simoen, Cor Claeys and Joao Antonio Martino

ARRAY OF MINIATURIZED STRUCTURES APPLIED O SMALL-LABS DEVELOPMENT
Alisson R. Leite, Roberto R. Lima, Eliphas W.Simões and Maria Lúcia P. da Silva

CARBON DIOXIDE SENSING AT NEAR INFRARED USING ZEOLITIC IMIDAZOLATE FRAMEWORK-8 (ZIF- 8) ABSORBERS
Ademauro Volponi and Sebastião Gomes dos Santos Filho

IMAGING AMPLIFICATION FOR MINIMALLY INVASIVE MEDICAL DEVICES
Jose Correia, Jose Gomes, Catarina Costa, Reinoud Wolffenbuttel, Joao Carmo

Coffee Break & Exhibitors
15:20 h - 15:40 h

Session 5 – Sensors
Thursday, 15:40 h – 17:00 h

Chair: Jacobus Swart, Unicamp, Brazil
Room: Fernando Pessoa 1

15:40 h – 16:00 h
NOVEL SAW GAS SENSOR BASED ON GRAPHENE
Ioannis NIKOLAOU, Hamida Hallil, George Deligeorgis, Veronique Conedera, Hermenegildo Garcia, Corinne Dejous and Dominique Rebière

16:00 h – 16:20 h
POROUS SILICON PHOTONIC CRYSTAL APPLIED AS CHEMOSENSOR FOR ORGANIC SOLVENTS
Danilo Huanca and Walter Salcedo

16:20 h – 16:40 h
DESIGN OF AN INTERDIGITATED MICROELECTRODE BIOSENSOR USING A-SIC:H SURFACE TO CAPTURE E. COLI
José Herrera-Celis, Claudia Reyes-Betanzo and Abdu Orduña-Díaz

16:40 h – 17:00 h
ADAPTATION OF THE PEDAGOGICAL APPROACHES FOR MASTER STUDENTS IN MICROELECTRONICS IN THE FRAME OF A FRENCH-CHINESE JOINT PROGRAM
Olivier Bonnaud and Xuefei Zhong

Friday, September 4th

Coffee Break & Exhibitors
09:40 h - 10:00 h

Session 6 – Nanowires and TFETs
Friday, 10:00 h – 12:00 h

Chair: João Antonio Martino, USP, Brazil
Room: Fernando Pessoa 1

10:00 h – 10:20 h
EFFECTIVE CHANNEL LENGTH IN JUNCTIONLESS NANOWIRE TRANSISTORS
Renan Trevisoli, Rodrigo Doria, Michelly de Souza and Marcelo Pavanello

10:20 h – 10:40 h
DETAILED ANALYSIS OF TRANSPORT PROPERTIES OF FINFETS THROUGH Y-FUNCTION METHOD: EFFECTS OF SUBSTRATE ORIENTATION AND STRAIN
Thales Augusto Ribeiro, Eddy Simoen, Cor Claeys, João Antonio Martino and Marcelo Antonio Pavanello

10:40 h – 11:00 h
IMPACT OF DIAMETER ON TFET CONDUCTION MECHANISMS
Victor B. Sivieri, Paula G. D. Agopian and João A. Martino

11:00 h – 11:20 h
ANALYTICAL COMPACT MODEL FOR TRIPLE GATE UNCTION-LESS MOSFETS
Fernando Ávila-Herrera, Antonio Cerdeira, Bruna Cardoso Paz, Magali Estrada and Marcelo Antonio Pavanello

11:20 h – 11:40 h
ANALYSIS OF ANALOG PARAMETERS IN NW-TFETS WITH SI AND SIGE SOURCE COMPOSITION AT HIGH TEMPERATURES
Caio Bordallo, João Martino, Paula Agopian, Rita Rooyackers, Anne Vandooren, Aaron Thean, Eddy Simoen and Cor Claeys

11:40 h – 12:00 h
ELECTRICAL CHARACTERIZATION OF ELECTRODEPOSITED NI NANOWIRES FOR MAGFET APPLICATION
Marcos Vinicius Puydinger dos Santos, Lucas Petersen Barbosa Lima, Rafael Alves Mayer, Jefferson Bettini, Fanny Béron, Kleber Roberto Pirota and José Alexandre Diniz

Lunch
11:40 h - 13:20 h

Invited Paper 3
Friday, 13:20 h – 14:00 h

Room: Fernando Pessoa 1

More Moore and More Than Moore meeting for 3D
Simon Deleonibus

Session 7 – Photonics
Friday, 14:00 h – 16:00 h

Chair: Henri Boudinov, UFRGS, Brazil
Room: Fernando Pessoa 1

14:00 h – 14:20 h
ALL-OPTICAL MAJORITY AND FEYNMAN GATES IN PHOTONIC CRYSTALS
Luis Eduardo Pedraza Caballero, Juan Pablo Vasco Cano, Paulo Sérgio Soares Guimarães and Omar Paranaiba Vilela Neto

14:20 h – 14:40 h
ENGINEERING OF THE PHOTOLUMINESCENCE OF ZNO NANOWIRES BY DIFFERENT GROWTH AND ANNEALING ENVIRONMENTS
A. L. F. Cauduro, C. I. L. Sombrio, P. L. Franzen, H. I. Boudinov and D. L. Baptista

14:40 h – 15:00 h
PHOTO AND ELECTROLUMINESCENCE FROM SINX LAYERS DEPOSITED BY REACTIVE SPUTTERING
Guilherme Sombrio, Frâncio Rodrigues, Paulo Franzen, Paulo Soave and Henri Boudinov

15:00 h – 15:20 h
INAS QUANTUM DOTS ON GAAS FOR INTERMEDIATE BAND SOLAR CELLS
Daniel Micha, Eleonora Weiner, Roberto Jakomin, Rudy Kawabata, Renato Mourão, Mauricio Pires and Patricia Souza

15:20 h – 15:40 h
NEW HYBRID STRUCTURES BASED ON CDSE/ZNS QUANTUM DOTS AND MULTILAYER GRAPHEME FOR PHOTONICS APPLICATIONS
Andrei Alaferdov, Raluca Savu, Simas Rackauskas, Tatiana Rac-

kauskas, Mara Canesqui, Yulia Gromova, Anna Orlova, Alexander Baranov, Analoty Fedorov and Stanislav Moshkalev

15:40 h – 16:00 h

FRESNEL ZONE PLATE ARRAY FABRICATED BY MASKLESS LITHOGRAPHY

Luís Alberto Barêa, Antonio A. von Zuben, Tayeb Mohammed-Brahim, Arlindo Neto Montagnoli, Michel Hospital, Newton Cesário Frateschi and Giuseppe Antonio Cirino

- WCAS 2015 -

5th Workshop on Circuits and Systems Design

This fith Workshop on Circuits and System Design - WCAS 2015 is devoted to the presentation and discussion of design experiences with a high degree of relevance in industrial, educational and research contexts, as well as innovative design methodologies and application of specific design technologies in an industrial context.

The workshop is organized within two tracks: industrial and academic. Contributions should illustrate state-of-the-art designs, design methodologies or tools, which will provide viable solutions in tomorrow's silicon and embedded systems. The contribution should present electronic circuit and system design results from FPGA and/or ASIC prototypes, or from simulation. Designs that achieve a specific record in terms of performance, power management or any other concrete advantage compared to the state-of-the-art for a given application domain should also be submitted to this workshop. Validated methodologies and techniques through demonstration are welcome.

- 5th WCAS 2015 -

-- Committees --

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- Technical Sessions -

Wednesday, September 2nd

Sponsor Presentations 1
Wednesday, 13:35 h – 15:20 h

Room: Zélia Gatai 1

13:35 h – 13:50 h
FPGAs em aplicações de IoT
Fabio Petrassem de Sousa, *Macnica DHW*

13:50 h – 14:05 h
Access to ASIC Prototyping and Production Services
Carl Das, *IMEC*

14:05 h – 14:20 h
MCTI and imec partnership: learning for excellence in nano -electronics
Liesbet Van der Perre, *MCTI/IMEC*

14:20 h – 14:35 h
Mentor Graphics
Alexandre Lerer, *Mentor Graphics*

14:35 h – 14:50 h
O projeto Unitec e a importância da contratação de Recursos Humanos
Edelweis Ritt, *Unitec*

14:50 h – 15:05 h
Empowering Innovation - Tools and Solutions for IP Migration, Analysis, Modeling & Sizing of Nanometer IC Designs
Gunter Strube, *MunEDA*

15:05 h – 15:20 h
Nano Imprint Lithography: Basics, Benefits and Applications
Otto Bobenstetter, *EVG Group*

Coffee Break & Exhibitors
15:20 h - 15:40 h

Sponsor Presentations 2
Wednesday, 15:40 h – 18:10 h

Room: Zélia Gatai 1

15:40 h – 15:55 h
CEITEC – PMUB (Projeto Multiusuário Brasileiro)
Fernando Chávez, *CEITEC*

15:55 h – 16:10 h
3D Electromagnetic Simulation using CST STUDIO SUITE 2015
Rodrigo Enjiu, *3Dtronic/CST*

16:25 h – 16:40 h
Electronic Systems and IoT trends
Victor Grimblatt, *Synopsys*

16:40 h – 16:55 h
Técnicas de medição e Análise para dispositivos Semicondutores
Keysight

16:55 h – 17:10 h
O poder dos FPGAs programáveis pelo usuário em suas aplicações de teste
Lincoln Ferreira Lúcio, *National Instruments*

17:10 h – 17:25 h
Advanced Packaging Technologies
David Rasmussen, *Palomar*

17:25 h – 17:40 h
MOSIS

17:40 h – 17:55 h
Heidelberg

17:55 h – 18:10 h
Osciloscópios Rhode & Schwarz: ferramentas essenciais para análise avançada de protocolos
Rhode & Schwarz

18:10 h - 18:25 h
Innovative solutions for advanced nanofabrication
André Linden, Raith

Thursday, September 3rd

Coffee Break & Exhibitors
09:40 h - 10:00 h

Invited Paper 1
Thursday, 10:00 h – 10:40 h

Chair:
Room: Zélia Gatai 1

SoC Self-test with Logic BIST
Alexandre S. Lujan, Rubens Takiguti, Marcelo Fukui

Session 1 – Digital Design
Thursday, 10:40 h – 12:00 h

Chair: Alexandre Lujan
Room: Zélia Gatai 1

10:40 h – 11:00 h
ASIC IMPLEMENTATION OF A POWER QUALITY DATA COMPRESSION / DECOMPRESSION CORE
Marcos Hervé, Cristiano Thiele, César Crovato, Guilherme Soares and Sergio Bampi

11:00 h – 11:20 h
A COMPREHENSIVE GUIDE FOR CRC HARDWARE IMPLEMENTATION
Dawood Alnajjar and Mauricio Suguiy

11:20 h – 11:40 h
MEMORY OPTIMIZATIONS ON A WINDOWING/BLOCK SWITCHING MODULE
Joaquim Oliveira, Wagner Oliveira and Fábio Jesus

11:40 h – 12:00 h
IZHIKEVICH-NEURON MODEL ON FPGA: A HIGHLY COMBINATIONAL IMPLEMENTATION
Vitor Bandeira, Vivianne Costa, Guilherme Bontorin and Ricardo Reis

Lunch
12:00 h - 13:20 h

Session 2 – Analog
Thursday, 13:20 h – 15:20 h

Chair:
Room: Zélia Gatai 1

13:20 h – 13:40 h
A NEW READOUT STRATEGY FOR MICROBOLOMETER INFRARED FOCAL PLANE ARRAYS
Leonardo Sa, Germano Fonseca and Antonio Mesquita

13:40 h – 14:00 h
BROADBAND HIGH DYNAMIC SURVEILLANCE
Renan dos Santos Fagundes, Denis Le Jeune and Ali Mansour

14:00 h – 14:20 h
A 10-BIT SD A/D CONVERTER FOR THE SBCD IN 180NM CMOS TECHNOLOGY
Helga U. Dornelas, Roger L. B. Zamparette, Juan C. Monsalve D. and Eric Fabris

14:20 h – 14:40 h
DESIGN METHODOLOGY OF SIGMA-DELTA MODULATORS BASED ON Q FACTOR FOR STABILITY CONTROL
José Andrade, Marlon Filho, Heider Madureira and Rafael Ferreira

14:40 h – 15:00 h
PUSH PULL BASED TRANSCONDUCTOR FOR ULTRA LOW VOLTAGE APPLICATIONS
Luís Henrique Rodovalho, Eric Fabris and Hamilton Klimach

15:00 h – 15:20 h
MIXED RF-DIGITAL DESIGN-TO-TEST FRAMEWORK FOR POWER AMPLIFIER DIGITAL PREDISTORTION
Takao Inoue and Alexsanser Loula

Coffee Break & Exhibitors
15:20 h - 15:40 h

Session 3 – Digital Design for Wireless Applications
Thursday, 15:40 h – 16:40 h

Chair:
Room: Zélia Gatai 1

15:40 h – 16:00 h
FPGA IMPLEMENTATION AND ASIC RESOURCE ESTIMATION OF AN FFT/IFFT FOR AN MR-OFDM TRANSCEIVER COMPLAINT WITH IEEE802.15.4G
Daniel Garcia Urdaneta, Eduardo Rodrigues de Lima, Gabriel Santos da Silva, Cesar Giovanni Chaves Arroyave, Jacqueline Gomes Mertes and Luís Geraldo Pedroso Meloni

16:00 h – 16:20 h
HARDWARE IMPLEMENTATION OF AN OFDMA-WRAN AUTO-CORRELATION
João Carlos Nunes Bittencourt, Nelson Alves Ferreira Neto and Wagner Luiz Alves de Oliveira
16:20 h – 16:40 h

SYSTEM-LEVEL ANALYSIS FOR A NEW SBCD TRANSPONDER SOC
Marcelo Negreiros, David Cordova, Everton Reckziegel, Lucas Paris, Jerson Guex, Pedro Toledo and Eric Fabris

Friday, September 4th

Coffee Break & Exhibitors
09:40 h - 10:00 h

Session 4 – Analog & RF & Mixed Signal
Friday, 10:00 h – 12:00 h

Chair: Victor Grimblatt
Room: Zélia Gatai 1

10:00 h – 10:20 h
STANDARD CELL LIBRARY DATABASE GENERATION FOR DIGITAL ASIC DESIGN FLOW
Luís Henrique Reinicke, Lauro Puricelli, Cícero Nunes, Maurício Altieri, Marcelo Erigson, Augusto Neutzling, Alonso Schmidt, Paulo Francisco Butzen, Renato Perez Ribas and Eric Fabris

10:20 h - 10:40 h
PYHDL HIGH-LEVEL SYNTHESIS THROUGH A CROSS-COMPILER FROM PURE PYTHON TO HARDWARE DESCRIPTION LANGUAGES
Jaime-Alberto Parra-Plaza

10:40 h - 11:00 h
FAST INSTRUCTION-DRIVEN TIMING PROCESSOR MODEL FOR MANY-CORE EMBEDDED SYSTEMS
Felipe Rocha Rosa, Luciano Ost and Ricardo Reis

11:00 h - 11:20 h
AN OVERVIEW OF STATIC AND SIMULATION-BASED TECHNIQUES FOR SYSTEMS-ON-CHIP VERIFICATION
João Carvalho and Wagner Oliveira

11:20 h - 11:40 h
FORMAL VERIFICATION IN COMMERCIAL SEMICONDUCTOR IP DEVELOPMENT: A RECOLLECTION
Walter Encinas

11:40 h - 12:00 h
EFFECT OF HIERARCHICAL ATPG ON SCAN PATTERN VOLUME
Alexandre Lujan, Cezar Santos, Jorge Corso and Rubens Takiguti

Lunch
11:40 h - 13:20 h

Session 5 – EDA and Methodology - State Machines and Process Related
Friday, 14:00 h – 16:00 h

Chair:
Room: Zélia Gatai 1

14:00 h – 14:20 h
A NOVEL ARCHITECTURE FOR LOCALLY-CLOCKED EXTENDED BURST-MODE FINITE STATE MACHINES
Duarte Oliveira, Tiago Curtinhas and Lester Faria

14:20 h – 14:40 h
A NOVEL SYNTHESIS METHOD BASED ON DIRECT MAPPING OF LOW-POWER SYNCHRONOUS FINITE STATE MACHINES
Duarte Oliveira, Tiago Curtinhas, Lester Faria and Leonardo Romano

14:40 h – 15:00 h
A STATE ASSIGNMENT METHOD FOR LOW-POWER SYNCHRONOUS FINITE STATE MACHINES BASED ON GENETIC ALGORITHM
Gabriel Dalario, Tiago Curtinhas, Jocemar Souza, Duarte Oliveira and Lester Faria

15:00 h – 15:20 h
SIGNAL ELECTROMIGRATION IN NANO-SCALE TECHNOLOGIES
Gracieli Posser, Vivek Mishra, Palkesh Jain, Ricardo Reis and Sachin S. Sapatnekar

15:20 h – 15:40 h
ELECTRICAL CHARACTERIZATION OF INTEGRATED CIRCUIT INTERCONNECTS PROCESSED WITH FOCUSED ION BEAM
Emmanuel Petitprez, Saulo Jacobsen, Ronald Tararam, Cristiano Krug and Marcelo Lubaszewski

15:40 h – 16:00 h

NEW TECHNOLOGY MIGRATION METHODOLOGY FOR ANALOG IC DESIGN

Helga Dornelas, Alonso Schmidt, Gunter Strube and Eric Fabris

- SForum 2015 -

15th Microelectronics Students Forum

The Microelectronics Students Forum is an event promoted by the Brazilian Microelectronics Society (SBMicro) and the Brazilian Computer Society (SBC) with the following main goals:

- Promote the participation of undergraduate students in the two most important international events in the area of Microelectronics organized each year in Brazil: "SBCCI: Symposium on Integrated Circuits and Systems Design" and "SBMicro: Symposium on Microelectronics Technology and Devices";

- Promote the realization of student's projects in a variety of topics within the field of microelectronics;

- Provide an opportunity for the presentation and discussion of research projects developed by undergraduate students;

- Promote advanced tutorial presentations on microelectronics understandable for undergraduate and graduate students starting or willing to start in this promising field.

- 15th SForum 2015 -

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- Technical Sessions -

Thursday, September 3rd

Coffee Break & Exhibitors
09:40 h - 10:00 h

SForum Oral Session
Thursday, 10:00 h – 12:00 h

Chair: José Camargo da Costa, UnB, Brazil
Room: Zélia Gatai 2

10:00 h – 10:15 h
BEHAVIORAL MODELING OF DUAL-BAND RADIO FREQUENCY POWER AMPLIFIERS USING VOLTERRA SERIES
Thierry Dompsin, Otávio Riba and Eduardo Lima

10:15 h – 10:30 h
DESIGN AND LINEARITY ANALYSIS OF A M--2M DAC FOR VERY LOW SUPPLY VOLTAGE
Israel Sperotto, Hamilton Klimach and Sergio Bampi

10:30 h – 10:45 h
DINAMIC THRESHOLD VOLTAGE CONFIGURATION TO REDUCE THE PARASITIC EDGE TRANSISTOR ON SOI TECHNOLOGY
José Augusto Padovese, Ricardo Rangel and João Martino

10:45 h – 11:00 h
IMPROVING TRANSISTOR FOLDING TECHNIQUE IN ASTRAN CAD TOOL
Gustavo Henrique Smaniotto, Matheus Trevisan Moreira, Adriel Mota Ziesemer Jr., Felipe de Souza Marques and Leomar Soares da Rosa Jr.

11:00 h – 11:15 h
STUDY OF OXIDIZED-POROUS SILICON AS INSULATING FILM FOR HI-PS FIELD EMISSION DEVICES
Débora Ariana Corrêa da Silva, Michel Oliveira da Silva Dantas, Elisabete Galeazzo, Henrique Estanislau Maldonado Peres and Francisco Javier Ramirez-Fernandez

11:15 h – 11:30 h
STUDY OF THERMAL ANNEALING ON IRRADIATED MOSFET DEVICES
Karlheinz Cirne, Marcilei Silveira, Felipe Leite, Nilberto Medina and Roberto Baginski

11:30 h – 11:45 h
THRESHOLD VOLTAGE TIME-VARIATIONS IN MOSFETS UNDER TOTAL IONIZING DOSE EFFECTS
Nícolas Evaristo Araújo, Felipe G. H. Leite, Roberto B. B. Santos, Karlheinz H. Cirne, Luis E. Seixas Jr and Marcilei Aparecida Guazzelli da Silveira

11:45 h – 12:00 h
TOPOLOGICAL ASPECTS OF NON-SERIES-PARALLEL TRANSISTORS NETWORKS
Maicon S. Cardoso, Regis Zanandrea, Renato S. de Souza, Leomar S. da Rosa Jr. and Felipe S. Marques

Friday, September 4th

Coffee Break & Exhibitors
09:40 h - 10:00 h

SForum Poster Session
Friday, 10:00 h – 12:00 h

Chair: Rodrigo Doria, FEI, Brazil

Room: Foyer S1

A VHDL IMPLEMENTATION OF THE LIGHTWEIGHT CRYPTOGRAPHIC ALGORITHM HIGHT
Fernando Melo Nascimento, Fernando Messias dos Santos and Edward David Moreno

DESIGN AND CHARACTERIZATION OF A 2.4GHZ LNA IN 180NM CMOS TECHNOLOGY
Elmo Luiz Fechine Sette, Ranieri Saldanha, Emmanuel Dupouy and Antonio Augusto Lisboa de Souza

DESIGN AND IMPLEMENTATION IN VHDL OF RPU COMPONENTS OF IPNOSYS ARCHITECTURE
José Neto and Sílvio Araújo

EFFICIENT LOOK-UP TABLE-BASED FPGA IMPLEMENTATION OF THE SIMPLIFIED BI-DIMENSIONAL MEMORY POLYNOMIAL MODEL
André Machoski, Otavio Riba, Luis Schuartz and Eduardo Lima

FPGA-BASED IMPLEMENTATION OF A BIOMEDICAL SIGNAL PROCESSING UNIT FOR BIOIMPEDANCE MEASUREMENT APPLICATION

Raphael Pereira, Allan Oliveira and Andre Mariano

IMPLEMENTATIONS AND COMPARISONS OF HIGH-SPEED MULTIPLIERS FOR RECONFIGURABLE DEVICES
Tiago Patrocinio, Sinésio Santos da Silva Neto and Ivan Saraiva Silva

MODELING AND SIMULATION OF LASER RANGEFINDER ARCHITECTURE
Fábio Jesus, Joel Filho, João Bittencourt and Thiago Jesus

MULTI-SHAPE HARDWARE DESIGN FOR THE ADAPTIVE LOOP FILTER
Ruhan Conceição, Andrio Araujo, Bruno Zatt, Marcelo Port and Luciano Agostini

POWER NMOSFET DEVICES UNDER X-RAY EFFECT
Denis Loesch, Marcilei A. G. Silveira, John Paul Hempel Lima, Kimon Stylianos, Mario Kawano, Devair Arrabaça, Milene Galeti and Michele Rodrigues

ROBUST PROCESSOR BASED ON ALTERNATING MODULE ACTIVATION
Daniel Sarsur Câmara, Lucas Gomes and Frank Sill Torres

STUDY OF OXIDIZED-POROUS SILICON AS INSULATING FILM FOR HI-PS FIELD EMISSION DEVICES
Débora Ariana Corrêa da Silva, Michel Oliveira da Silva Dantas, Elisabete Galeazzo, Henrique Estanislau Maldonado Peres and Francisco Javier Ramirez-Fernandez

STUDY OF THERMAL ANNEALING ON IRRADIATED MOSFET DEVICES
Karlheinz Cirne, Marcilei Silveira, Felipe Leite, Nilberto Medina and Roberto Baginski

THRESHOLD VOLTAGE TIME-VARIATIONS IN MOSFETS UNDER TOTAL IONIZING DOSE EFFECTS
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TOPOLOGICAL ASPECTS OF NON-SERIES-PARALLEL TRANSISTORS NETWORKS
Maicon S. Cardoso, Regis Zanandrea, Renato S. de Souza, Leomar S. da Rosa Jr. and Felipe S. Marques

VERITRACE: A TOOL TO GENERATE TRACE BUFFERS FOR POST-SILICON DEBUG

Danilo D. Almeida, Fredy A. M. Alves
and José Augusto M. Nacif

- PATMOS 2015 -

25th International Workshop on Power and Timing Modeling, Optimization and Simulation

PATMOS has a history of 25 years and it is one of the first conferences world-wide to focus on low power. PATMOS 2015 is co-located with VARI 2015 and SBCCI 2015 in Salvador, Brazil. The traditional scope of the PATMOS conference series has mainly been about and around the design of circuits and architectures optimized for highest performance at lowest power consumption. But meanwhile, power-efficiency has become extremely important for many more areas spreading far beyond this traditional R&D niche. Energy-efficient ICT (Information and Communication Technology) infrastructures are a key issue of local and global economies. Some predict that until the year 2030, if current trends continue, the electricity consumption caused by the Internet to grow by up to 30 times. Energy prices will grow substantially. The next generation of oil and gas seismic simulations, for ins-tance, will require orders of magnitude more computational power. Already during the past 11 years the price of crude oil increased by a factor of 9 with significantly increasing tendency in the future. The strong increase of wireless communication and the growth of cloud computing will further contribute to this trend. A future peta- or exa-flop supercomputer would need its own power plant if the gap between computation and power consumption could not be resolved: It is the intention of PATMOS 2015 to think beyond current solutions such that the very wide gap between computation and the massive energy consumption for ICT infrastructures can be closed.

- 25th PATMOS 2015 -

-- Committees --

General Co-Chairs

Ricardo Reis | *FRGS, Brazil* | *reis@inf.ufrgs.br*

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Márcio Fontana | *UFBA, BRAZIL*

Edson Santana | *UFBA, BRAZIL*

Finance Chair

Gracieli Posser | *UFRGS*

Publication Chair

Carolina Metzler | *UFRGS*

- Tutorials -

Tuesday, September 1st

Room: Fernando Pessoa 2

Tutorial 1

8:40 h - 10:20 h
Low Power Design Essentials
JAN RABAEY
University of California at Berkeley - UCB

Coffee Break & Exhibitors
10:20 h - 10:40 h

Tutorial 2

10:40 h - 12:20 h
Ultra-Low-Voltage (ULV) IC Design: Designing for VDD below kT/q
MÁRCIO CHEREM SCHNEIDER
Universidade Federal de Santa Catarina - UFSC

Lunch
12:20 h - 14:00 h

Tutorial 3A

13:40 h - 15:20 h
Impact of Low Frequency Noise on the Reliability and Variability of Nano CMOS devices
JALAL JOMAAH
Institut National Polytechnique de Grenoble - INPG, France; Lebanese University

Coffee Break & Exhibitors
15:20 h - 15:40 h

Tutorial 4A

15:40 h - 17:20 h
Cyber - Physical Systems: Reality, Dreams, and Fantasy
MAGDY A. BAYOUMI
University of Louisiana at Lafayette

Room: Fernando Pessoa 3

Tutorial 3B

13:40 h - 15:20 h
3D ICs - Moving from silicon to heterogeneous technologies
MACIEJ OGORZALEK
Jagiellonian University, Krakow, Poland

Coffee Break & Exhibitors
15:20 h - 15:40 h

Tutorial 4B

15:40 h - 17:20 h
Low Loss, High Isolation, Linear RF Switch Design in SOI
PETER H. POPPLEWELL
Skyworks Solutions

- Technical Sessions -

Wednesday, September 2nd

Coffee Break & Exhibitors
09:40 h - 10:00 h

Session 1 – Circuit and system optimization
Wednesday, 10:00 h – 12:00 h

Chair: Ran Ginosar, Technion-Israel Institute of Technology, Israel
Room: Fernando Pessoa 3

10:00 h – 10:20 h
EXACT SCHEDULABILITY ANALYSIS FOR HARD REAL-TIME SYSTEMS ACCOUNTING DVFS LATENCY ON HETEROGENEOUS CLUSTER-BASED PLATFORM
Eduardo Bezerra Valentin, Mario Salvatierra, Rosiane Freitas and Raimundo Barreto

10:20 h – 10:40 h
INFERRING CUSTOM ARCHITECTURES FROM OPENCL
Krzysztof Kepa, Ritesh Soni and Peter Athanas

10:40 h – 11:00 h
ABEEMAP: A MAPPING ALGORITHM BASED ON MULTI-OBJECTIVE ARTIFICIAL BEE COLONY
Viviane Souza and Abel Silva-Filho

11:00 h – 11:20 h
EFFICIENT PARALLELIZATION OF THE DISCRETE WAVELET TRANSFORM ALGORITHM USING MEMORY-OBLIVIOUS OPTIMIZATIONS
Anastasis Keliris, Olympia Kremmyda, Vasilis Dimitsas, Michail Maniatakos and Dimitris Gizopoulos

11:20 h – 11:40 h
CALCULATION OF WORST-CASE EXECUTION TIME FOR MULTI-CORE PROCESSORS USING DETERMINISTIC EXECUTION
Hamid Mushtaq, Zaid Al-Ars and Koen Bertels

11:40 h – 12:00 h
AN UNCONVENTIONAL COMPUTING TECHNIQUE FOR ULTRA-FAST AND ULTRA-LOW POWER DATA MINING
Vincent Canals, Antoni Morro, Antoni Oliver, Miquel Lleó Alomar and Josep L. Rosselló

Lunch
12:00 h - 13:20 h

Invited Talk 1
Wednesday, 13:20 h – 14:00 h

Room: Fernando Pessoa 2

Frame Free Vision
TERESA SERRANO-GOTARREDONA
IMSECNM-CSIC, Sevilla; University of Sevilla

Coffee Break & Exhibitors
15:20 h - 15:40 h

Session 2 – System-level design and management
Wednesday, 16:00 h – 17:20 h

Chair: Vincent Canals, Balearic Islands University, Spain
Room: Fernando Pessoa 3

16:00 h – 16:20 h
TEJAS: A JAVA BASED VERSATILE MICRO-ARCHITECTURAL SIMULATOR
Smruti R. Sarangi, Rajshekar Kalayappan, Prathmesh Kallurkar, Seep Goel and Eldhose Peter

16:20 h – 16:40 h
DEDICATED NETWORK FOR DISTRIBUTED CONFIGURATION IN A MIXED-SIGNAL WIRELESS SENSOR NODE CIRCUIT
Soundous Chairat, Edith Beigné and Marc Belleville

16:40 h – 17:00 h
ENERGY MANAGEMENT VIA PI CONTROL FOR DATA PARALLEL APPLICATIONS WITH THROUGHPUT CONSTRAINTS
Anca Molnos, Warody Lombardi, Suzanne Lesecq, Julien Mottin, Diego Puschini and Arnaud Tonda

17:00 h – 17:20 h
VLSI ARCHITECTURE DESIGN AND IMPLEMENTATION OF A LDPC ENCODER FOR THE IEEE 802.22 WRAN STANDARD
Nelson Alves Ferreira Neto, Wagner Luiz Alves de Oliveira, João Carlos Nunes Bittencourt and Joaquim Ranyere Santana de Oliveira

Special Session - Celebrating the 25th Anniversary of PATMOS
Wednesday, 17:20 h – 18:20 h

Chair: Ricardo Reis, UFRGS, Brazil
Room: Fernando Pessoa 2

How to Cope with the Power Wall
REINER HARTENSTEIN,
TU Kaiserslautern, Germany

Thursday, September 3rd

Coffee Break & Exhibitors
09:40 h - 10:00 h

Session 3 – Low power design techniques
Thursday, 10:00 h – 12:00 h

Chair: Jose Luis Guntzel, UFSC, Brazil
Room: Fernando Pessoa 3

10:00 h – 10:20 h
DYNAMIC CURRENT REDUCTION OF CMOS DIGITAL CIRCUITS THROUGH DESIGN AND PROCESS OPTIMIZATIONS
Jordan Innocenti, Loïc Welter, Nicolas Borrel, Franck Julien, Jean-Michel Portal, Jacques Sonzogni, Laurent Lopez, Pascal Masson, Stephan Niel, Philippe Dreux and Julia Castellan

10:20 h – 10:40 h
UNIFIED POWER FORMAT (UPF) METHODOLOGY IN A VENDOR INDEPENDENT FLOW
Emilie Garat, David Coriat, Edith Beigné and Leandro Stefanazzi

10:40 h – 11:00 h
ASYNCHRONOUS SUB-THRESHOLD ULTRA-LOW POWER PROCESSOR
Ron Diamant, Ran Ginosar and Christos Sotiriou

11:00 h – 11:20 h
CONSTRUCTING STABILITY-BASED CLOCK GATING WITH HIERARCHICAL CLUSTERING
Bao Le, Djordje Maksimovic, Dipanjan Sengupta, Erhan Ergin, Ryan Berryhill and Andreas Veneris

11:20 h – 11:40 h
ADAPTIVE ENERGY MINIMIZATION OF EMBEDDED HETEROGENEOUS SYSTEMS USING REGRESSION-BASED LEARNING
Sheng Yang, Rishad Shafik, Geoff Merrett, Ed Stott, Josh Levine, James Davis and Bashir Al-Hashimi

11:40 h – 12:00 h
EVALUATION AND MITIGATION OF AGING EFFECTS ON A DIGITAL ON-CHIP VOLTAGE AND TEMPERATURE SENSOR
Mauricio Altieri, Suzanne Lesecq, Diego Puschini, Olivier Heron, Edith Beigne and Jorge Rodas

Lunch
12:00 h - 13:20 h

Invited Talk 2
Thursday, 13:20 h – 14:00 h

Room: Fernando Pessoa 2

System-Level Design of Heterogeneous System-on-Chip Architectures
LUCA CARLONI,
Columbia University, EUA

Session 4 – Reliability, noise reduction and robustness
Thursday, 14:00 h – 15:20 h

Chair: Jorge Juan-Chico, Seville University, Spain
Room: Fernando Pessoa 3

14:00 h – 14:20 h
EXPLORATION OF TECHNOLOGY PARAMETER VALUES OF INTEGRATED CIRCUIT TECHNOLOGIES
Rodrigo Fonseca Rocha Soares, Frank Sill Torres and Dirk Timmermann

14:20 h – 14:40 h
FREQUENCY-DOMAIN MODELING OF GROUND BOUNCE AND SUBSTRATE NOISE FOR SYNCHRONOUS AND GALS SYSTEMS
Milan Babic, Xin Fan and Milos Krstic

14:40 h – 15:00 h
BETTER-THAN-VOLTAGE SCALING ENERGY REDUCTIONIN APPROXIMATE SRAMS VIA BIT DROPPING AND BIT REUSE
Fabio Frustaci, David Blaauw, Dennis Sylvester and Massimo Alioto

15:00 h – 15:20 h
A VERSATILE AND RELIABLE GLITCH FILTER FOR CLOCKS
Robert Najvirt and Andreas Steininger

Coffee Break & Exhibitors
15:20 h - 15:40 h

Friday, September 4th

Coffee Break & Exhibitors
09:40 h - 10:00 h

Session 5 – Energy-efficiency sytems
Friday, 10:00 h – 12:00 h

Chair: Frank Sill Torres, UFMG, Brazil
Room: Fernando Pessoa 3

10:00 h – 10:20 h
ENERGY-EFFICIENT LEVEL SHIFTER TOPOLOGY
Roger Llanos, Diego Sousa, Marco Terres, Guilherme Bontorin, Ricardo Reis and Marcelo Johann

10:20 h – 10:40 h
ENERGY EFFICIENCY OF ZIPF TRAFFIC DISTRIBUTIONS WITHIN FACEBOOK'S DATA CENTER FABRIC ARCHITECTURE
Lisa Durbeck

10:40 h – 11:00 h
ENERGY-AWARE MAPPING FOR DEPENDABLE VIRTUAL NETWORKS
Victor Lira and Eduardo Tavares

11:00 h – 11:20 h
REUSING SMALLER OPTIMIZED FFT BLOCKS FOR THE REALIZATION OF LARGER POWER EFFICIENT RADIX-2 FFTS
Sidinei Ghissoni, Eduardo Da Costa and Ricardo Reis

11:20 h – 11:40 h
COMBINING PEL DECIMATION WITH PARTIAL DISTORTION ELIMINATION TO INCREASE SAD ENERGY EFFICIENCY
Ismael Seidel, André Beims Bräscher and Jose Luis Güntzel

11:40 h – 12:00 h
WIDEBAND DYNAMIC VOLTAGE SENSING MECHANISM FOR EH SYSTEMS
Kaiyuan Gao, Yuqing Xu, Delong Shang, Fei Xia and Alex Yakovlev

Lunch
12:00 h - 13:20 h

Invited Talk 3
Friday, 13:20 h – 14:00 h

Room: Fernando Pessoa 2

Device-Circuit Co-design of Multi-Gate FETs in sub-10nm Technologies
KAUSHIK ROY
Purdue University, EUA

- VARI 2015 -

6th International Workshop on CMOS Variability

VARI 2015 is the 6th International Workshop on CMOS Variability. The increasing variability in CMOS transistor characteristics, as well as its sensitivity to environmental variations has become a major challenge to scaling and integration of nano-scale devices. This leads to major changes in the way that future integrated circuits and systems are designed. Strong links must be established between circuit design, system design and device technology. The VARI workshop answers to the need to have an event on variability in CMOS technology development and circuit design, where industry and academia meet.

The main VARI objective is to provide a forum to discuss and investigate the CMOS process and environmental variability issues in methodologies and tools for the design of current and upcoming generations of integrated circuits and systems. The technical program will focus on performance and power consumption as well as architectural aspects like adaptability or resilience, with particular emphasis on modeling, design, characterization, analysis and optimization in respect to variability. Digital, Analog, Mixed Signal and RF circuits are within VARI scope.

The VARI Workshop is organized outside Europe for the first time, in this edition occurring in Salvador, Brazil, from September 1st through September 4th, 2015. The Program Committee of VARI 2015 counted on 29 members from European and South American Institutions to review all paper submissions. Every paper went through at least three reviews, leading to a judicious selection for the Program. A total of 13 regular papers were selected for the VARI 2015 Program, which is also comprised of 06 Tutorials, and 06 Keynotes/Invited Talks. All the Tutorials and Keynotes are shared by VARI 2015 attendees and the participants of the collocated events PATMOS 2015 – 25th International Workshop on Power Modeling, Timing and Optimization, and the SBCCI2015 – 28th Symposium on Circuits and Systems Design.

On behalf of all participants of VARI 2015, we would like to thank the General Chair of Chip in Bahia Robson Nunes de Lima, and all the Organizing Committee members of this exciting multi-events week.

Welcome to the 6th edition of VARI, in the beautiful city of Salva-

dor in Bahia.

Ricardo Reis
Nadine Azemard
Co-Chairs – VARI 2015

Sergio Bampi
Massimo Alioto
Technical Program Co-Chairs

- 6th VARI 2015 -

-- Committees --

General Chair

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Sergio Bampi | *UFRGS, Brazil*

Local Arrangements Chair

Robson Nunes de Lima | *UFBA, Brazil*

Márcio Fontana | *UFBA, Brazil*

Edson Santana | *UFBA, Brazil*

Finance Chair

Gracieli Posser | *UFRGS, Brazil*

Publication Chair

Guilherme Bontorin | *UFGRS, Brazil*

- Tutorials -

Tuesday, September 1st

Room: Fernando Pessoa 2

Tutorial 1

8:40 h - 10:20 h
Low Power Design Essentials
JAN RABAEY
University of California at Berkeley - UCB

Coffee Break
10:20 h - 10:40 h

Tutorial 2

10:40 h - 12:20 h
Ultra-Low-Voltage (ULV) IC Design: Designing for VDD below kT/q
MÁRCIO CHEREM SCHNEIDER
Universidade Federal de Santa Catarina - UFSC

Lunch
12:20 h - 14:00 h

Tutorial 3A

13:40 h - 15:20 h
Impact of Low Frequency Noise on the Reliability and Variability of Nano CMOS devices
JALAL JOMAAH
Institut National Polytechnique de Grenoble - INPG, France; Lebanese University

Coffee Break
15:20 h - 15:40 h

Tutorial 4A

15:40 h - 17:20 h
Cyber - Physical Systems: Reality, Dreams, and Fantasy
MAGDY A. BAYOUMI,
University of Louisiana at Lafayette

Room: Fernando Pessoa 3

Tutorial 3B

13:40 h - 15:20 h
3D ICs - Moving from silicon to heterogeneous technologies
MACIEJ OGORZALEK
Jagiellonian University, Krakow, Poland

Coffee Break
15:20 h - 15:40 h

Tutorial 4B

15:40 h - 17:20 h
Low Loss, High Isolation, Linear RF Switch Design in SOI
PETER H. POPPLEWELL
Skyworks Solutions

- Technical Sessions -

Wednesday, September 2nd

Invited Talk 1
Wednesday, 13:20 h – 14:00 h

Room: Fernando Pessoa 2

Frame Free Vision
TERESA SERRANO-GOTARREDONA
IMSECNM-CSIC, Sevilla; University of Sevilla

Coffee Break & Exhibitors
15:20 h - 15:40 h

Session 1 - Compensation at Architectural or Application Level
Wednesday, 14:00 h – 15:20 h

Chair: Gilles Jacquemod | *Polytechnique de Nice, France*
Room: Fernando Pessoa 3

14:00 h – 14:20 h
AN APPLICATION-SPECIFIC NBTI AGEING ANALYSIS METHOD
Haider Abbas, Mark Zwolinski and Basel Halak *(University of Southampton, UK)*

14:20 h – 14:40 h
DELAY VARIATION COMPENSATION THROUGH ERROR CORRECTION USING RAZOR
Adelson N. Chua, Rico Jossel M. Maestro, Mark Earvin V. Alba, Wes Vernon V. Lofamia, Bernard Raymond D. Pelayo, Ken Bryan F. Fabay, John Cris F. Jardin, Kervin John C. Jocson, Joy Alinda R. Madamba, John Richard E. Hizon, and Louis P. Alarcon *(University of the Philippines Diliman, Philippines)*

14:40 h – 15:00 h
2.64 PJ REFERENCE-FREE POWER SUPPLY MONITOR WITH A WIDE TEMPERATURE RANGE
Hernán Cerqueira, Pablo Ituero and Marisa Lopez-Vallej *(Universidad Politecnica de Madrid, Spain)*

15:00 h – 15:20 h
EXPLORATION OF NOISE ROBUSTNESS AND SENSITIVITY OF BULK CURRENT SENSORS FOR SOFT ERROR DETECTION
João Guilherme Mourão Melo[1], Frank Sill Torres[1] and Rodrigo Possamai Bastos[2]

(Universidade Federal de Minas Gerais[1], Brazil and Université de Grenoble-TIMA[2], France)

Thursday, September 3rd

Invited Talk 2
Thursday, 13:20 h – 14:00 h

Room: Fernando Pessoa 2

System-Level Design of Heterogeneous System-on-Chip Architectures
LUCA CARLONI
Columbia University, EUA

Coffee Break & Exhibitors
15:20 h - 15:40 h

Session 2 – Simulation and Characterization of Devices and Processing Variations
Thursday, 14:00 h – 15:20 h

Chair: Nadine Azemard, LIRMM, France
Room: Fernando Pessoa 3

15:40 h – 16:00 h
STUDY AND REDUCTION OF VARIABILITY IN 28NM FDSOI TECHNOLOGY
Gilles Jacquemod[1], Zhaopeng Wei[1], Jad Modad[1], Emeric de Foucauld[2], Frederic Hameau[2], Yves Leduc[1] and Philippe Lorenzini[1]
(Université Nice Sophia Antipolis[1], France and CEA-LETI[2], France)

16:00 h – 16:20 h
ENERGY STUDY FOR 28NM FDSOI TECHNOLOGY
Rida Kheirallah[1], Nadine Azemard[1] and Gilles Ducharme[2], *(LIRMM[1], France and Université Montpellier[2], France)*

16:20 h – 16:40 h
WITHIN-DIE AND DIE-TO-DIE VARIABILITY ON 65NM CMOS: OSCILLATORS EXPERIMENTAL RESULTS
Juan Pablo Martinez Brito[1,2], Marcelo Lubaszewski[1,2] and Sergio Bampi
(UFRGS[1], Brazil and CEITEC S.A[2], Brazil)

16:40 h – 17:00 h
MOSFET STACKED-PAIR TEST STRUCTURE FOR MISMATCH EVALUATION BY ESTIMATING THE ON-RESISTANCE RATIO

Juan Pablo Martinez Brito[1,2], Marcelo Lubaszewski[1,2] and Sergio Bampi *(UFRGS[1], Brazil and CEITEC S.A[2], Brazil)*

17:00 h – 17:20 h
GLOBAL STATISTICAL METHODOLOGY FOR THE ANALYSIS OF EQUIPMENT PARAMETER EFFECTS ON TSV FORMATION
Frederic Roger[1], Lado Filipovic[2], Anderson Singulani[1], Sara Carniello[1] and Siegfried Selberherr[2] *(ams AG[1], Austria and TU Wien[2], Austria)*

Friday, September 4th

Invited Talk 3
Friday, 13:20 h – 14:00 h

Room: Fernando Pessoa 2

Device-Circuit Co-design of Multi-Gate FETs in sub-10nm Technologies
KAUSHIK ROY,
Purdue University, EUA

Session 3 – Noise and Variability Modeling in CMOS Circuits
Friday, 14:00 h – 15:20 h

Chair: Mark Zwolinski, Univ. of Southampton, GBR
Room: Fernando Pessoa 3

14:00 h – 14:20 h
IS INTRINSIC NOISE A LIMITING FACTOR FOR SUBTHRESHOLD DIGITAL LOGIC IN NANOSCALE CMOS?
Francisco Veirano[1], Fernando Silveira[1] and Lirida Naviner[2], *(Universidad de la Republica[1], Uruguay and TELECOM ParisTech[2], France)*

14:20 h – 14:40 h
A NOISE SUPPRESSING FILTER DESIGN FOR REDUCING DECONVOLUTION ERROR OF BOTH-DIRECTIONS DOWNWARD SLOPED ASYMMERIC RTN LONG-TAIL DISTRIBUTIONS
Hiroyuki Yamauchi[1] and Worawit Somha[2]
(Fukuoka Institute of Technology[1], Japan and King Mongkut's Institute of Technology Ladkrabang[2], Thailand)

- General Scheduling -

-- Monday, August 31st --

HOUR / DAY			Monday August 31st	
ROOM			Florbela Espanca	Foyer S1
08h00min	-	08h20min		
08h20min	-	08h40min		
08h40min	-	09h00min		
09h00min	-	09h20min		
09h20min	-	09h40min		
09h40min	-	10h00min		
10h00min	-	10h20min		
10h20min	-	10h40min		
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11h20min	-	11h40min		
11h40min	-	12h00min		
12h00min	-	12h20min		
12h20min	-	12h40min	LUNCH	
12h40min	-	13h00min		
13h00min	-	13h20min		
13h20min	-	13h40min		
13h40min	-	14h00min	SBMicro Meeting	Registration Starts
14h00min	-	14h20min		
14h20min	-	14h40min		
14h40min	-	15h00min		
15h00min	-	15h20min		
15h20min	-	15h40min		
15h40min	-	16h00min	SBCCI Meeting	Registration
16h00min	-	16h20min		
16h20min	-	16h40min		
16h40min	-	17h00min		
17h00min	-	17h20min	SBMicro and SBCCI Steering	
17h20min	-	17h40min		
17h40min	-	18h00min		
18h00min	-	18h20min		
18h20min	-	18h40min		
18h40min	-	19h00min		
19h00min	-	19h20min		
19h20min	-	19h40min		
19h40min	-	20h00min		
20h00min	-	20h20min		
20h20min	-	20h40min		
20h40min	-	21h00min		

- General Scheduling -

-- Tuesday, September 1st --

HOUR / DAY			Tuesday September 1st.					
ROOM			Fernando Pessoa 1	Fernando Pessoa 2	Fernando Pessoa 3	Fernando Pessoa 4	Foyer S2 & Praça Luiz de Camões	Foyer S1
08h00min	-	08h20min						Registration
08h20min	-	08h40min						
08h40min	-	09h00min	SBMicro Tutorial 1	SBCCI / PATMOS / VARI Tutorial 1		Exhibitors		
09h00min	-	09h20min						
09h20min	-	09h40min						
09h40min	-	10h00min						
10h00min	-	10h20min						
10h20min	-	10h40min				Coffee Break		
10h40min	-	11h00min	SBMicro Tutorial 2	SBCCI / PATMOS / VARI Tutorial 2		Exhibitors		
11h00min	-	11h20min						
11h20min	-	11h40min						
11h40min	-	12h00min						
12h00min	-	12h20min						
12h20min	-	12h40min	LUNCH					
12h40min	-	13h00min						
13h00min	-	13h20min						
13h20min	-	13h40min						
13h40min	-	14h00min						
14h00min	-	14h20min	SBMicro Tutorial 3	SBCCI / PATMOS / VARI Tutorial 3A	SBCCI / PATMOS / VARI Tutorial 3B	Exhibitors		
14h20min	-	14h40min						
14h40min	-	15h00min						
15h00min	-	15h20min						
15h20min	-	15h40min						
15h40min	-	16h00min				Coffee Break		
16h00min	-	16h20min	SBMicro Tutorial 4	SBCCI / PATMOS / VARI Tutorial 4A	SBCCI / PATMOS / VARI Tutorial 4B	Exhibitors		
16h20min	-	16h40min						
16h40min	-	17h00min						
17h00min	-	17h20min						
17h20min	-	17h40min						
17h40min	-	18h00min						
18h00min	-	18h20min	Opening					
18h20min	-	18h40min	SBmicro Awards					
18h40min	-	19h00min						Cocktail
19h00min	-	19h20min						
19h20min	-	19h40min						
19h40min	-	20h00min						
20h00min	-	20h20min						
20h20min	-	20h40min						
20h40min	-	21h00min						

- General Scheduling -

-- Wednesday, September 2nd --

HOUR / DAY			Wednesday September 2nd.					
ROOM			Fernando Pessoa 1	Fernando Pessoa 2	Fernando Pessoa 3	Zélia Gatai 1	Foyer S1	Fernando Pessoa 4
08h00min	-	08h20min					Registration	
08h20min	-	08h40min						
08h40min	-	09h00min	Keynote 1					
09h00min	-	09h20min						
09h20min	-	09h40min						
09h40min	-	10h00min						Coffee Break & Exhibitors
10h00min	-	10h20min	SBMicro Paper Session 1	SBCCI Paper Session 1A	PATMOS Paper Session 1	SBCCI Paper Session 1B		Exhibitors
10h20min	-	10h40min						
10h40min	-	11h00min						
11h00min	-	11h20min						
11h20min	-	11h40min						
11h40min	-	12h00min						
12h00min	-	12h20min	LUNCH					
12h20min	-	12h40min						
12h40min	-	13h00min						
13h00min	-	13h20min						
13h20min	-	13h40min	SBMicro Invited Talk 1	SBCCI/PATMOS/VARI Invited Talk 1		WCAS Sponsor Session 1		Exhibitors
13h40min	-	14h00min						
14h00min	-	14h20min	SBMicro Paper Session 2	SBCCI Paper Session 2	VARI Paper Session 1			
14h20min	-	14h40min						
14h40min	-	15h00min						
15h00min	-	15h20min						
15h20min	-	15h40min						Coffee Break & Exhibitors
15h40min	-	16h00min	SBMicro Paper Session 3	SBCCI Paper Session 3	PATMOS Paper Session 2	WCAS Sponsor Session 2		Exhibitors
16h00min	-	16h20min						
16h20min	-	16h40min						
16h40min	-	17h00min						
17h00min	-	17h20min			PATMOS Special Session			
17h20min	-	17h40min						
17h40min	-	18h00min						
18h00min	-	18h20min	CA-ME CNPq Meeting		CECCI/SBC Assembly			
18h20min	-	18h40min						
18h40min	-	19h00min						
19h00min	-	19h20min			SBmicro Assembly			
19h20min	-	19h40min						
19h40min	-	20h00min						
20h00min	-	20h20min						
20h20min	-	20h40min						
20h40min	-	21h00min						

- General Scheduling -

-- Thursday, September 3rd --

HOUR / DAY			Thursday September 3rd.		
ROOM			Fernando Pessoa 1	Fernando Pessoa 2	Fernando Pessoa 3
08h00min	-	08h20min			
08h20min	-	08h40min			
08h40min	-	09h00min	Keynote 2		
09h00min	-	09h20min			
09h20min	-	09h40min			
09h40min	-	10h00min			
10h00min	-	10h20min	SBMicro Paper Session 4	SBCCI Paper Session 4	PATMOS Paper Session 3
10h20min	-	10h40min			
10h40min	-	11h00min			
11h00min	-	11h20min			
11h20min	-	11h40min			
11h40min	-	12h00min			
12h00min	-	12h20min	LUNCH		
12h20min	-	12h40min			
12h40min	-	13h00min			
13h00min	-	13h20min			
13h20min	-	13h40min	SBMicro Invited Talk 2	SBCCI/PATMOS/VARI Invited Talk 2	
13h40min	-	14h00min			
14h00min	-	14h20min	SBMicro Flash Paper Session	SBCCI Paper Session 5	PATMOS Paper Session 4
14h20min	-	14h40min			
14h40min	-	15h00min			
15h00min	-	15h20min			
15h20min	-	15h40min			
15h40min	-	16h00min	SBMicro Paper Session 5	SBCCI Paper Session 6	VARI Paper Session 2
16h00min	-	16h20min			
16h20min	-	16h40min			
16h40min	-	17h00min			
17h00min	-	17h20min			
17h20min	-	17h40min	Panel		
17h40min	-	18h00min			
18h00min	-	18h20min			
18h20min	-	18h40min			
18h40min	-	19h00min			
19h00min	-	19h20min			
19h20min	-	19h40min	Conference Dinner		
19h40min	-	20h00min			
20h00min	-	20h20min			
20h20min	-	20h40min			
20h40min	-	21h00min			

- General Scheduling -

-- Thursday, September 3rd --

HOUR / DAY			Thursday September 3rd.				
ROOM			Zélia Gatai 1	Zélia Gatai 2	Foyer S1	Luandino Vieira	Fernando Pessoa 4
08h00min	-	08h20min					
08h20min	-	08h40min					
08h40min	-	09h00min					
09h00min	-	09h20min					
09h20min	-	09h40min					
09h40min	-	10h00min					Coffee Break & Exhibitors
10h00min	-	10h20min	WCAS Invited Talk	SFORUM Paper Session		IEEE CEDA Brazil Chapter Meeting	Exhibitors
10h20min	-	10h40min					
10h40min	-	11h00min	WCAS Paper Session 1				
11h00min	-	11h20min					
11h20min	-	11h40min					
11h40min	-	12h00min					
12h00min	-	12h20min	LUNCH				
12h20min	-	12h40min					
12h40min	-	13h00min					
13h00min	-	13h20min					
13h20min	-	13h40min	WCAS Paper Session 2				Exhibitors
13h40min	-	14h00min					
14h00min	-	14h20min		CI Brazil Meetng	SBMicro Poster Session		
14h20min	-	14h40min					
14h40min	-	15h00min					
15h00min	-	15h20min					
15h20min	-	15h40min					Coffee Break & Exhibitors
15h40min	-	16h00min	WCAS Paper Session 3	CI Brazil Meetng			Exhibitors
16h00min	-	16h20min					
16h20min	-	16h40min					
16h40min	-	17h00min					
17h00min	-	17h20min					
17h20min	-	17h40min					
17h40min	-	18h00min					
18h00min	-	18h20min					
18h20min	-	18h40min					
18h40min	-	19h00min					
19h00min	-	19h20min					
19h20min	-	19h40min	Conference Dinner				
19h40min	-	20h00min					
20h00min	-	20h20min					
20h20min	-	20h40min					
20h40min	-	21h00min					

- General Scheduling -

-- Friday, September 4th --

HOUR / DAY			Friday September 4th.					
ROOM			Fernando Pessoa 1	Fernando Pessoa 2	Fernando Pessoa 3	Zélia Gatai 1	Foyer S1	Fernando Pessoa 4
08h00min	-	08h20min						
08h20min	-	08h40min						
08h40min	-	09h00min	Keynote 3					
09h00min	-	09h20min						
09h20min	-	09h40min						
09h40min	-	10h00min						Coffee Break & Exhibitors
10h00min	-	10h20min	SBMicro Paper Session 6	SBCCI Paper Session 7	PATMOS Paper Session 5	WCAS Paper Session 4	SFORUM Poster Session	Exhibitiotrs
10h20min	-	10h40min						
10h40min	-	11h00min						
11h00min	-	11h20min						
11h20min	-	11h40min						
11h40min	-	12h00min						
12h00min	-	12h20min	LUNCH					
12h20min	-	12h40min						
12h40min	-	13h00min						
13h00min	-	13h20min						
13h20min	-	13h40min	SBMicro Invited Talk 3	SBCCI/PATMOS/VARI Invited Talk 3				
13h40min	-	14h00min						
14h00min	-	14h20min	SBMicro Paper Session 7	SBCCI Paper Session 8	VARI Paper Session 3	WCAS Paper Session 5		
14h20min	-	14h40min						
14h40min	-	15h00min						
15h00min	-	15h20min						
15h20min	-	15h40min						
15h40min	-	16h00min						
16h00min	-	16h20min	AWARDS					
16h20min	-	16h40min	CLOSING					
16h40min	-	17h00min						
17h00min	-	17h20min						
17h20min	-	17h40min						
17h40min	-	18h00min						
18h00min	-	18h20min						
18h20min	-	18h40min						
18h40min	-	19h00min						
19h00min	-	19h20min						
19h20min	-	19h40min						
19h40min	-	20h00min						
20h00min	-	20h20min						
20h20min	-	20h40min						
20h40min	-	21h00min						