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Invited Speakers

29 AUGUST • 03 SEPTEMBER

2016

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Overview

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Keynote SBCCI (Wednesday, 31st of August 2016)

Rajiv Joshi

IBM Thomas J. Watson Research Center (USA)

Topic: From Low Power to Predictive Analytics – Beyond Guessing

Bio: *Dr. Rajiv V. Joshi is a research staff member at T. J. Watson research center, IBM. He received his B.Tech I.I.T (Bombay, India), M.S (M.I.T) and Dr. Eng. Sc. (Columbia University). His novel interconnects processes and structures for aluminum, tungsten and copper technologies which are widely used in IBM for various technologies from sub-0.5µm to 14nm. He has led successfully pervasive statistical methodology for yield prediction and also the technology-driven SRAM at IBM Server Group. He commercialized these techniques. He received 3 Outstanding Technical Achievement (OTAs), 3 highest Corporate Patent Portfolio awards for licensing contributions, holds 57 invention plateaus and has over 215 US patents and over 350 including international patents. He has authored and co-authored over 185 papers. He is recipient of 2015 BMM award. He is inducted into New Jersey Inventor Hall of Fame in Aug 2014 along with pioneer Nikola Tesla. He is a recipient of 2013 IEEE CAS Industrial Pioneer award and 2013 Mehboob Khan Award from Semiconductor Research Corporation. He is a member of IBM Academy of technology and master inventor. He served on committees of ISLPED (Int. Symposium Low Power Electronic Design), IEEE VLSI design, IEEE CICC, IEEE Int. SOI conference, ISQED and Advanced Metallization Program committees. He served as a general chair for IEEE ISLPED. He is an industry liaison for universities as a part of the Semiconductor Research Corporation. Also he is in the industry liaison committee for IEEE CAS society.*

Abstract: Moore's law drives lowering cost/function ratio and thus pushes addition of more functions on a chip. This requires reduction in power. In Internet of Everything (IoE), System on Chip (SOC), flexible electronics, 3D printing the drive towards low power while maintaining functionality will be essential. Also power has become the key driving force in high performance processor designs as the frequency scale-up is reaching saturation. In order to achieve low power system, circuit and technology co-design is essential. This talk focuses on pros and cons analysis of technology and circuit techniques from power perspective and various techniques to exploit lower power. The talk highlights fundamentals and the direction for low power optimization such as reduction in active, leakage, short circuit power and collision power will continue to be the focal area for in the scaled world. Conventional and advanced techniques (e.g. clock gating, power gating, longer channel, multi-Vt design, stacking, header-footer device techniques and new developments etc.) will be described for logic and memories. Finally key challenges in achieving low power will be described.

As the technology pushes towards sub-14nm era, process variability and geometric variation in devices can cause variation in power, performance and functionality. Predictive Analytics to capture systematic and random variation and to aid in robust design optimization in nm regime will be discussed. Also the talk will describe future growth directions and role of such predictive algorithms.

Keynote SBMicro (Thursday, 1st of September 2016)

Lorenzo Faraone

The University of Western Australia (Australia)

Topic: Optical MEMS Technologies for Infrared Spectroscopy, Sensing, and Imaging

Bio: *Professor Faraone is a Member of the Order of Australia (AM), and a Fellow of the Institute of Electrical and Electronic Engineers (FIEEE), Australian Academy of Science (FAA) and the Australian Academy of Technological Sciences and Engineering (FTSE). He has published more than 250 international journal papers on his research work, and supervised more than 35 PhD student completions. He is currently Head of the Microelectronics Research Group (MRG) at The University of Western Australia (UWA), and Director of the WA Centre for Semiconductor Optoelectronics and Microsystems (WACSOM). Prior to joining UWA in 1987, he worked primarily in the area of silicon CMOS-based microelectronics and non-volatile memory technology with RCA Labs in Princeton, NJ, USA. Since joining UWA he has worked on compound semiconductor materials and devices, including AlGaN/GaN HEMTs, HgCdTe-based infrared sensor technology and MBE growth, as well as optical MEMS technologies for infrared spectroscopy and imaging applications. His research activities also include mobility spectrum techniques for magneto-transport studies, which allow the transport properties and mobility distributions of individual carriers in multi-layer/multi-carrier semiconductor systems to be determined.*

Abstract: Current research efforts to further improve state-of-the-art infrared (IR) detector and imaging focal plane array (FPA) technologies are focused on reducing system cooling requirements, developing larger-format 2-dimensional imaging FPAs, extending the technology to longer wavelengths, and/or adding so-called multi-colour/hyper-spectral capability, which allows real-time spectral information to be gathered from multiple wavelength bands. Multi/hyper-spectral imaging in defence & aerospace scenarios provides enhanced target detection, improved target recognition, and reduced false alarm rates. In civilian, industrial and commercial arenas, such a technology is applicable to numerous remote sensing spectroscopy/imaging applications in agriculture, medical diagnostics, process control, food security, etc. This presentation will focus on recent advances in optical MEMS technologies that are capable of providing reduced size, weight and power (SWaP) solutions for field-portable and airborne drone/UAV applications. In particular, a number of micro-electromechanical systems (MEMS) based electrically tuneable Fabry-Perot filter technologies will be presented that are compatible with either individual detectors or large format 2-dimensional imaging IRFPAs. Such a technology can be hybridised with any existing optoelectronic detector/sensing/imaging technology, and is capable of low-voltage tuning across the NIR/SWIR, MWIR or LWIR wavelength bands for field-portable or airborne spectroscopy and/or imaging applications.

Invited SBCCI (Wednesday, 31st of August 2016)

Eduardo de la Torre

Universidad Politécnica de Madrid (Spain)

Topic: Towards Smarter Reconfigurable Systems

Bio: *Eduardo de la Torre is an Associate Professor of Electronics since 2002, and obtained his MSC and PhD degrees in Electrical Engineering from UPM in 1989 and 2000, respectively. His main expertise is in FPGA-based design and, in particular, on partial and dynamic reconfiguration of digital systems and emulation platforms for digital communications. He has more than 40 papers on reconfigurable systems in the last five years, and he is or has been Program Co-Chair of Reconfig (2012 and 2013), DASIP (20123) and SPIE VLSI Circuits & Systems (2009 and 2011) Conferences, as well as Program Committee member of Conferences such as FPL, ReCoSoC, RAW, WRC, ISVLSI, SIES. He is also reviewer of numerous Conferences and Journals such as IEEE Transactions on Computers, IEEE Transactions on Industrial Informatics, IEEE Transactions on Industrial Electronics, Sensor Magazine.ork security and privacy.*

Abstract: End users of electronic products demand not only more performant systems, but also to be lower energy consuming and more trustable and durable than ever. Durability refers to two aspects: on one side, products are expected to be robust enough so they can operate without problems for long periods of time, without visible malfunction and, on the other side, flexible enough so they may react to changing operational conditions, including environmental changes, functional changes or system changes (wear out, occurrence of faults, etc).

Traditionally, hardware systems offer good performance and, compared to software-based systems, low energy consumption. However, they are not as flexible as software. So, how to combine both aspects? Reconfigurable systems offer an intermediate solution with hardware-equivalent performance and software-equivalent flexibility. Even under the consideration of reconfigurable systems, flexibility and smartness are not easy to achieve. To guarantee adaptiveness, of even better, self-adaptiveness, adaptiveness, several of the so called self-* features, such as self-reconfiguration, self-calibration, self-protection, self-awareness or even self-repair, are able to provide this referred smartness.

This talk provides a general overview on the benefits of using FPGA-based reconfigurable systems, some application examples and, later on, it goes deeper on how these systems may contribute to higher adaptiveness and smartness. Later, a classification of autonomy levels is presented. In the second part of the talk, two example systems are presented. First, a reconfigurable architecture to dynamically trade-off between performance, fault tolerance and energy consumption is shown, demonstrating how systems may adapt to changing execution conditions. Second, an evolvable hardware system, able of self-adapting to changing functionality and even self-healing from faults, is presented.

Invited SBCCI (Thursday, 1st of September 2016)

Rajeev Ranjan

Cadence Design System, Inc. (USA)

Topic: Formal Technology in Modern SoC Flow: Establishing Correctness for Functionality and Security

Bio: *Rajeev Ranjan is leading the business development efforts of a newly formed business unit at Cadence following the acquisition of Jasper Design Automation, where he was the CTO and was responsible for developing Jasper's overall technology vision and driving the business value of formal.*
Rajeev has been active in the area of formal verification for over 20 years. He has served in the organization and program committee of many international conferences including DAC, ICCAD, FMCAD, and CHARME. He has published numerous articles and has 12 patents in the area of functional verification. Rajeev received his Bachelor's degree from Indian Institute of Technology, Kanpur (aka IIT Kanpur), his Master's degree from University of Illinois at Urbana-Champaign (aka UIUC), and his doctorate degree from University of California at Berkeley (aka UC Berkeley). He also has an MBA degree from Wharton School of Business with a focus on entrepreneurial management and finance.

Abstract: Over the last decade, formal verification technology has made significant impact in bringing quality and productivity gains in SoC design and verification flow – ranging from architectural modeling to RTL development to SoC integration all the way to post-silicon debugging. Today, a variety of targeted verification tasks, e.g. register verification, x-propagation verification, connectivity verification, etc. can be performed solely by formal verification technology without depending on a complementary simulation flow. Verifying security attributes of an SoC is emerging as a challenging area as the IoT era dawns upon us. While the security risks in a system pertain to potential flaws in both hardware and software components, establishing hardware security is critical, because it forms the foundation for secure applications and a security hole in hardware implementation can compromise the entire system.
In this talk, we will first provide a brief overview of formal technology and its applications, followed by a broader discussion on the scalable methods of applying formal technology for hardware security verification.

Invited SBCCI (Friday, 2nd of September 2016)

Jeffrey Bokor

UC Berkeley (USA)

Topic: Speed and Reliability of Nanomagnetic Logic (NML) Technology

Bio: *Jeffrey Bokor is the Paul R. Gray Distinguished Professor of Engineering in the department of Electrical Engineering and Computer Sciences at UC Berkeley. In 2012, he was named Associate Dean for Research in the UC Berkeley College of Engineering. From 2004 until 2012, Prof. Bokor held a joint appointment as Deputy Director for Science at the Molecular Foundry, a nanoscale science research center at Lawrence Berkeley National Laboratories (LBNL). He currently holds a joint appointment as Senior Scientist in the Materials Science Division at LBNL. He received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology in 1975, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1976 and 1980, respectively. From 1980 to 1993, he was at AT&T Bell Laboratories where he did research on a variety of topics in laser science, as well as semiconductor physics and technology, and held several management positions. He joined the Berkeley faculty in 1993. His current research activities include nanomagnetics/spintronics, carbon nanotube and graphene electronics, nanophotonics, and nano-electromechanical systems. He is a fellow of IEEE, APS, and OSA.*

Abstract: Nanomagnetic logic (NML) is an alternative to electron charge-based information processing for energy efficient computing applications. However, experiments indicate that nanomagnets are susceptible to thermal and lithographic noise, resulting in logical errors during signal transmission and computation. Here, we study the origins of errors in NML and present a technique for reducing error rates based on anisotropy engineering. Using photoelectron emission microscopy (PEEM), we verify the functionality and error-immunity properties of anisotropy-engineered nanomagnets in NML applications. Further, we use time-resolved PEEM to follow the sub-nanosecond dipolar coupling signal propagation dynamics in optimized chains with 100 ps time resolution as they are cycled with nanosecond field pulses at a rate of 3 MHz. A switching time for individual nanomagnetic elements near 100 ps is observed. These experiments, and accompanying macro-spin and micromagnetic simulations, provide deeper insight into the underlying physics of NML architectures operating on nanosecond timescales and help identify relevant engineering parameters to optimize performance and reliability.

Invited SBMicro (Wednesday, 31st of August 2016)

Tayeb Mohammed-Brahim

Université de Rennes (France)

Topic: Silicon: a flexible material for bendable electronics and sensors

Bio: *Tayeb Mohammed-Brahim is currently professor in Rennes 1 University (France), Head of Microelectronics & Microsensors Department of the Institute of Electronics and Telecommunications of Rennes and Director of the Common Center on Microelectronics in the west of France. He got his PhD (Doctorat d'Etat) in Paris-XI University (France) and he founded the thinfilm Laboratory in Algiers University (Algeria). Then he moved to Caen University (France) where he created the reliability Laboratory. After that and since 2000, he moved to Rennes University where he became the head of Microelectronics Group becoming the Microelectronics and Microsensors Department after 2002.*
He is mainly involved in low temperature fabrication of thin film electronic devices for flexible electronics and in the fabrication of sensors. Previously he activated a lot on chemical and biologic sensors for the measurement of pH, the detection of DNA and the quantification of proteins. Presently, his main activities focus on mechanical sensors for health applications. He is author of more than 300 papers on these different fields.

Abstract: Directly crystallized deposited silicon at low temperature is shown to be the right material when bendable system including treatment electronics and sensing functions is needed. This is true particularly when process reproducibility, electrical and mechanical reliability of the devices are the most important parameters implying the success of the technology. Indeed, these parameters are the main issues when we need to go beyond the publication of a paper, towards actual commercial application.
Electrical and mechanical performances of microcrystalline silicon thin film transistors and deformation sensors on 25 µm thick flexible plastics under high bending, still 0.75 mm curvature radius, are presented. These devices are fabricated directly on this substrate at a maximum temperature of 180°C.

Invited SBMicro (Wednesday, 31st of August 2016)

Fernando Guarín

Global Foundries (USA)

Topic: Leveraging semiconductor technology for the benefit of society

Bio: *Dr. Fernando Guarín is a Distinguished Member of Technical Staff at Global Foundries in East Fishkill NY and Adjunct Lecturer at SUNY New Paltz. He retired from IBM's SRDC after 27 years as Senior Member of Technical Staff. He earned his BSEE from the "Pontificia Universidad Javeriana", in Bogotá, Colombia, the M.S.E.E. degree from the University of Arizona, and the Ph.D. in Electrical Engineering from Columbia University, NY He has been actively working in microelectronic reliability for over 35 years. From 1980 until 1988 he worked in the Military and Aerospace Operations division of National Semiconductor Corporation. In 1988 he joined IBM's microelectronics division where he worked in the reliability physics and modeling of Advanced Bipolar, CMOS and Silicon Germanium BiCMOS technologies. Dr. Guarín is an IEEE Fellow, Distinguished Lecturer for the IEEE Electron Device Society, where he has served in many capacities including; member of the IEEE's EDS Board of governors, chair of the EDS Education Committee, Secretary for EDS. He is the EDS President-Elect 2016-2017.*

Abstract: Electron devices, thanks to relentless scaling, coupled along with advances in material science, have enabled the exponential growth of the information technologies that have transformed society. This increased information content gives us a unique path to alleviate and find solutions to the problems of many of the most important issues facing the world today. These advances must remind us that we are all now connected – economically, technically and socially. But we are also learning that just being connected may not be sufficient. We must solve many problems. As engineers, we have the knowledge and the responsibility to do so. The level of instrumentation grows daily with ever increasing intelligence and ability to communicate and automate many processes and industries in what is now known as the Internet of Things (IoT). Thanks to these advances the world is smaller and flatter. The reality of living in a globally integrated world is upon us and is presenting us with many opportunities and challenges. In this talk, we will discuss how Semiconductor technology and electron devices have benefited society and the world in which we live. The multiple advances in devices and materials have provided us with unprecedented amounts of information at continually decreasing costs. We will provide tangible evidence that illustrates how electron devices are influencing society, changing our interaction with other people near and far, while providing many people the ability to have access to light and information technology even in the most remote corners of the planet. We must leverage these advances to expand educational opportunities while helping to preserve a sustainable and greener environment. We will provide information on initiatives and access to funding for engineering projects at the local level. Ultimately we must always bear in mind that the large number of scientific and technological advances must produce tangible results for the benefit and progress of humanity.

Invited SBMicro (Wednesday, 31st of August 2016)

Yeshaiahu Fainman

University of California San Diego (USA)

Topic: Nanoscale Light Emitters

Bio: *Professor Fainman received the Ph. D. from Technion in 1983. He is a Cymer Professor of Advanced Optical Technologies and Distinguished Professor of ECE at the University of California, San Diego (UCSD). His current research involves near field optical science and technology, nanophotonics, nanolasers, nanoiplasmonics and ultrafast optics. He is a Fellow of OSA, IEEE, and SPIE. He Chaired, co-Chaired and served on numerous program committees for various conferences for OSA, IEEE/LEOS, and SPIE. He is a recipient of the Miriam and Aharon Gutvirt Prize, Technion, Haifa, Israel (1982), Lady Davis Fellowship (2006), Brown award (2006), Gabor Award (2012) and E. Leith Medal (2015). He served as a topical editor and board member for various journals. He contributed over 250 manuscripts in peer review journals and over 450 conference presentations and conference proceedings.*

Abstract: Nanocavity light-emitters with high spontaneous emission factors, β, have attracted considerable attention in the past decade in light of their technical applications ranging from optical interconnects, sensing and imaging to fundamental research on thresholdless lasers quantum cavity electrodynamics. Theoretically a high-β nanolaser is more energy efficient as most spontaneous emission is funneled into the lasing mode, resulting in an extremely low lasing threshold. In this talk we will focus on three promising candidates for the next generation of densely packed chip-scale photonic circuits: metal-clad subwavelength lasers, coaxial lasers and luminescent hyperbolic metamaterials. We will summarize the recent research efforts in the theory, design, fabrication, and characterization of such devices.

Invited SBMicro (Thursday, 1st of September 2016)

Patrick Fay

University of Notre Dame (USA)

Topic: Advances in III-V Heterostructure Devices and Integration for Millimeter-Wave and THz Sensing and Imaging

Bio: *Patrick Fay is a Professor in the Dept. of Electrical Engineering at the University of Notre Dame. He received a Ph.D. in electrical engineering from the University of Illinois at Urbana-Champaign in 1996. His research interests include the design, fabrication, and characterization of compound semiconductor electronic devices and circuits, as well as high-speed optoelectronic devices and optoelectronic integrated circuits for fiber optic telecommunications. His research also includes the development and use of micromachining techniques for the fabrication of microwave through sub-millimeter-wave components and packaging. He established the High Speed Circuits and Devices Laboratory at Notre Dame that houses comprehensive device and circuit test capabilities. He also oversaw the design, construction, and commissioning of the class 100 cleanroom housed in Stinson-Remick Hall at Notre Dame, and has served as the director of this facility since 2003. Prof. Fay is a fellow of the IEEE, has published 9 book chapters, more than 130 articles in refereed scientific journals, and more than 180 conference proceedings.*

Abstract: Devices based on GaN and related III-N materials are increasingly well established in RF power applications, and are under active research and development for power conversion and control applications. However, the unique material properties of the III-Ns make them a promising basis for applications well beyond these traditional applications. Novel device concepts that harness these material properties in conjunction with unconventional operational physics are being explored to serve needs in applications as diverse as millimeterwave and THz electronics and sensing, low-power systems, and ultra-scaled low-power logic. Devices exploiting interband tunneling in III-N heterostructures for low-power logic, as well as impact ionization and plasma-wave propagation in GaN 2DEGs for millimeter-wave and THz sensing and electronics are under active investigation to provide new levels of performance.

Invited SBMicro (Thursday, 1st of September 2016)

Libor Rufer

University of Grenoble / TIMA Laboratory (France)

Topic: Approaches to the Design, Fabrication, and Test of Electroacoustic Micro-transducers

Bio: *Libor Rufer received his Engineer degree from the Faculty of Electrical Engineering, Prague and his Ph.D. in Acoustics from Czech Technical University, Prague, Czech Republic. He obtained his DEA diploma (Diplôme d'Etudes Approfondies, eq. Master) in Acoustics from Ecole Centrale, Lyon, France and the HDR (Habilitation à Diriger des Recherches) diploma in physics from Joseph Fourier University, Grenoble, France. Until 1993, he was with the Faculty of Electrical Engineering at the Czech Technical University, Prague. Since then, he is a researcher with the Joseph Fourier University, Grenoble, France. In 1998, he joined the TIMA Laboratory. Currently, he is member of its MNS (Micro- Nano- Systems) Group. His expertise is mainly in MEMS-based sensors and actuators, electro-acoustic and electro-mechanical transducers modeling, design, and applications of these devices in different fields as consumer, biomedical or RF.*

Abstract: Silicon-based microphones are nowadays well-established MEMS components produced by strong industrial actors. The fabrication of such acoustic sensors is based on a dedicated technology fulfilling all designed parameters. On the other hand, the development of such a technology processes is costly and time-consuming. In this paper, we will present approaches based on technologies readily available to small companies and academic institutions. We will show, on several examples, a design process of acoustic micro-transducers fabricated through generic technologies. Focused will be a CMOS-MEMS process applied to the realization of suspended diaphragms that can be part of transducers with piezoresistive, electrostatic, or electrodynamic transduction. We will also briefly present a testing technique that can be used for acoustic sensors calibration. This technique has a special interest for sensors with a frequency response exceeding the typical audible range.

Invited SBMicro (Thursday, 1st of September 2016)

Cor L. Claeys

IMEC (Belgium)

Topic: Random Telegraph Signal Noise in Advanced High Performance and Memory Devices

Bio: *Cor Claeys received the Ph.D. degree from KU Leuven in Belgium, where he is Professor since 1990. At imec he is presently Director of Advanced Semiconductor Technologies responsible for strategic relations. His main interests are silicon technology, device physics, low frequency noise phenomena, radiation effects and defect engineering and material characterization. He co-edited a book on "Low Temperature Electronics" and "Germanium-Based Technologies: From Materials to Devices" and wrote monographs on "Radiation Effects in Advanced Semiconductor Materials and Devices" and "Fundamental and Technological Aspects of Extended Defects in Germanium". Two of these books have translated in Chinese. He authored and coauthored 14 book chapters, over 1000 conference presentations and more than 1200 technical papers. He is also editor or co-editor of 60 Conference Proceedings. Prof. Claeys is a Fellow of the Electrochemical Society and of IEEE. He was the Founder of the IEEE Electron Devices Benelux Chapter, Chair of the IEEE Benelux Section, an elected AdCom Member of the Electron Devices Society and the EDS Vice President for Chapters and Regions. He was EDS President in 2008-2009. He was as Division Director on the IEEE Board of Directors in 2012-2013. He is a recipient of the IEEE Third Millennium Medal and in 2013 he received the IEEE EDS Distinguished Service Award. Within the Electrochemical Society, he was the Chair of the Electronics & Photonics Division from 2001 to 2003. In 2004, he received the Electronics & Photonics Division Award.*

Abstract: Random Telegraph Signal noise has been extensively studied for more than 30 years and gained high interest in recent years due to its importance for scaled down technologies. This review will demonstrate the power of RTS for single defect characterization. Present understanding of the device physics and evolutions in RTS characterization are highlighted. Special attention is given to RTS in memory devices such as DRAMS, ReRAM, planar (2D) and vertical (3D) flash.

Invited SBMicro (Friday, 2nd of September 2016)

Mircea Guina

Tampere University of Technology (Finland)

Topic: III-V/Si integration: technological advances and new application perspectives

Bio: *Mircea Guina received the Ph.D. degree in physics from the Tampere University of Technology, Tampere, Finland, in 2002. In 2008, he was appointed as the Professor and Head of the III–V Optoelectronics Group at the Optoelectronics Research Centre, Tampere University of Technology. He conducts scientific work related to molecular beam epitaxy of novel optoelectronic heterostructures and devices, and their applications. His current projects are concerned with the development of uncooled lasers, amplifiers, and modulators for hybrid-PICs, ordered nanostructures for quantum optics, epitaxy of III-Bi-V alloys, the development of high-power semiconductor lasers (VECSELs and MOPAs), and the development of ultrahigh efficiency multijunction solar cells based on GaInNAsSb-alloys. He has published more than 120 journal papers, several book chapters, holds four international patents, has several position of trust in COST Actions and scientific boards, and has given numerous invited talks at major optoelectronics conferences. He is the Director of the International Summer School "New Frontiers in Optical Technologies," which he established in 2001.*

Abstract: A review of two major directions for integrating optoelectronics and microelectronics technology platforms is presented. As a first approach, we will discuss progress concerning the hybrid integration of silicon photonics, in particular silicon-on-insulator technology, with III-V optoelectronic components. Secondly, we review recent progress concerning direct integrating of III-V alloys on Si by so called heteroepitaxy technology. Applications outlined include realization of integrated optical transceiver for data communication at several hundreds of GB/s and development of multi-wavelength Si-integrated light sources for spectroscopy.

Invited Speaker INSCIT
(Thursday, 1st of September 2016)

Mathias Steiner

IBM Research (Brazil)

Topic: Platform Integration of Novel Materials: From Nanoscale Electronics to Industrial Scale Applications

Bio: *Dr. Mathias Steiner is Manager and Research Staff Member – Industrial Technology & Science at IBM Research | Brazil. His focus is on combining computational and experimental research for industrial scale applications in Oil&Gas and Healthcare/Environment. Mathias has 15 years of experience with applied and industrial research for IT, Electronics, Optics, Materials, Aerospace, Life Sciences, and O&G. He has initiated and managed various multi-national research collaborations with industrial and academic partners, leading to more than 60 technical publications and patents so far. Also, Mathias is frequently invited to speak at international research conferences and industry meetings. Mathias first joined IBM Research in Physical Sciences at the TJ Watson Research Center, Yorktown Heights, New York, USA, where he led research projects concerned with nanometer scale materials and devices, including the demonstration of record speed carbon nanotube array transistors and the development of novel techniques for investigating the optical and electronic properties of functional materials at the nanoscale. Mathias holds a diploma in Physics and a doctorate in Physical Chemistry, as well as a diploma in Business Administration.*

Abstract: The integration of low-dimensional materials with their extreme surface-to-volume ratios opens a route to explore novel device conceptions and to compare them with state-of-the-art semiconductor technology. Implemented based on CMOS compatible workflows, one- and two-dimensional nanomaterials such as carbon nanotubes, graphene, or 2d-semiconductors are enabling electronic and optoelectronic functionalities that cannot be realized in the same fashion with bulk semiconductors. In this presentation, I will discuss how low-dimensional materials can be integrated within instrumentation platforms for characterizing their performance and for realizing sensing functionalities for exploratory on-chip applications. Implementation examples range from light emitters and detectors to sensors for studying liquids at the nanometer scale. Potential industrial application areas for the integrated measurement functionalities include Lab-on-Chip Chemistry and Biotechnology.

Invited Speaker INSCIT
(Friday, 2nd of September 2016)

Mehmet Kaynak

Innovations for High Performance Microelectronics – IHP (Germany)

Topic: MEMS Module Integration into SiGe BiCMOS Technology for Embedded System Applications

Bio: *Dr.–Ing Mehmet Kaynak received his B.S degree from Electronics and Communication Engineering Department of Istanbul Technical University (ITU) in 2004, took the M.S degree from Microelectronic program of Sabanci University, Istanbul, Turkey in 2006 and received the PhD degree from Technical University of Berlin, Berlin Germany in 2014. He joined the technology group of IHP Microelectronics, Frankfurt (Oder), Germany in 2008. Dr. Kaynak has received the young scientist award of Leibniz institute for the year of 2014. Since 2015, he is acting as the department head of technology group at IHP, Germany and network faculty member at Sabanci University, Turkey.*

Abstract: Introduction of radio frequency micro-electro-mechanical structures (RFMEMS) as a monolithic option into state-of-the-art Si/SiGe BiCMOS foundry processes have paved the way for single chip radio frequency microsystems. Deep silicon substrate etch techniques have also allowed to prevent from high substrate losses which helps to achieve high performance passive components at mm-wave frequencies. Using the same process techniques, realization of highly efficient on-chip antennas has become feasible, which in the millimeter-wave range no longer come with a hefty chip real estate penalty. In parallel to the developments on SiGe HBT performance, “More-than-Moore” path, which covers all the additional functionalities to the standard CMOS process (i.e. MEMS devices, microfluidics, etc…), allows to realize multi-functional circuits and systems.
In this talk, the latest developments on embedded BiCMOS+MEMS integration concept will be presented. Reconfigurable circuits using embedded RF-MEMS switches and mm-wave transceivers with on-chip antennas will also be discussed, as the application examples.

Tutorial Speaker SBCCI (Monday, 29th of August 2016)

Reinhart Job

University of Applied Sciences
Muenster (Germany)

Topic: Development Process for MEMS Pressure Sensors with CMOS Read-Out Circuitry

Bio: *Reinhart Job studied physics at the University of Bochum, Germany, and received his doctorate in experimental solid state physics. For 17 years he worked at the Open University in Hagen, first as a scientist, and after his habilitation in the field of technology of electronic components, as a professor. Since 2011 he is with the University of Applied Sciences Muenster, where he acts since 2013 as dean of the Faculty of Electrical Engineering and Computer Science. Reinhart Job authored and co-authored more than 200 publications on Applied Solid State Physics and semiconductor materials research for international journals.*

Abstract: Monolithic integrated pressure sensor systems are realized by the combination of the two different technologies: CMOS-technology for the electrical part and MEMS-technology for the pressure sensor part. The challenge here is to design the pressure sensor cell in such a way that a wide pressure range can be covered with one fix lateral membrane size, as any change in this lateral dimensions would lead to a new CMOS design, resulting in high costs. The detailed knowledge of the generation of the electrical signal of the sensor, and the knowledge of the effect of production process deviations on the characteristics and performance of a sensor is a key for a design of a wide range of applications.

This talk exemplarily describes the approach how to realize such a pressure sensor system to be able on one hand to measure a nominal pressure range of several bar, but also to measure the low pressure range of several tenth of mbar by keeping a sufficient signal to noise ratio, and without changing the original CMOS circuitry. Further on, the influence of certain process deviations is investigated, and the mechanical stability of the membrane concerning pressure overload as an important specification parameter is considered. A method will be presented that allows calculating the electrical signals of Wheatstone-Bridge based silicon pressure sensors, using general semiconductor fundamentals from the theory of piezoresistivity. The effect of different implant profiles and certain production process deviations during the fabrication of the membrane (e.g. membrane thickness deviations) are considered. For the calculation of the sensor signal, an analytical approach, based on the theory of piezoresistivity, is combined it with structural mechanical simulation of mechanical stress, utilizing the Finite Element Analysis (FEA). A comparison between theoretical signal evaluation and measurement as a proof of feasibility of the approach is given. As the requirements of the performance of pressure sensors are increasing by the rapidly growing applications strictly defined procedures during development and production, which confine the options of possible solutions, have to be followed. An investigation of potential failure modes and a systematically development flow of new sensors, also considering the application, as described in the ISO 26262 standard, is mandatory if the application of the sensor is rated as functional safety related.

Tutorial Speaker SBCCI (Monday, 29th of August 2016)

Eduardo de la Torre

Universidad Politécnica de Madrid (Spain)

Topic: Partial Reconfiguration Applied to Dynamic Multithread Hardware Acceleration and Evolvable Hardware

Bio: *Eduardo de la Torre is an Associate Professor of Electronics since 2002, and obtained his MSC and PhD degrees in Electrical Engineering from UPM in 1989 and 2000, respectively. His main expertise is in FPGA-based design and, in particular, on partial and dynamic reconfiguration of digital systems and emulation platforms for digital communications. He has more than 40 papers on reconfigurable systems in the last five years, and he is or has been Program Co-Chair of Reconfig (2012 and 2013), DASIP (20123) and SPIE VLSI Circuits & Systems (2009 and 2011) Conferences, as well as Program Committee member of Conferences such as FPL, ReCoSoC, RAW, WRC, ISVLSI, SIES. He is also reviewer of numerous Conferences and Journals such as IEEE Transactions on Computers, IEEE Transactions on Industrial Informatics, IEEE Transactions on Industrial Electronics, Sensor Magazine.ork security and privacy.*

Abstract: Although partial reconfiguration in FPGAs is theoretically as easy as writing new contents in the configuration memory, the questions on what, when, and how to reconfigure the FPGA may make this task not that easy. The situation may be worse if these questions are merged with an even more important question: what for?

In this tutorial, the basics on partial reconfiguration using position-independent bitstreams are shown. After a brief FPGA internal architecture description (centered on series 7 Xilinx devices), the correspondence between addresses in the configuration memory and its equivalent positions in the reconfigurable fabric are shown. Reconfiguration with position reallocation is introduced afterwards. This solves, in some manner, the question on 'how' to reconfigure. As an application example (trying to partially answer the 'what for' question), we present a multi-slot architecture, called Artico3, which allows dynamic execution of multiple threads by using a variable set of HW accelerators, obtained by means of a High Level Synthesis process (i.e., answering 'what' to reconfigure),. The architecture is suited for, dynamically at runtime, trading performance versus fault tolerance and energy consumption. A task scheduler decides, at runtime, 'when' and 'what' accelerators are to be run, according to possibly changing system requirements. A live demo will be provided, showing this architecture running in different performance/fault tolerance/energy consumption operation points, moving from one mode into another by means of dynamic and partial reconfiguration. As a second application, an evolvable HW platform is presented. In this case, HW is created autonomously, according to changes proposed by an evolutionary algorithm. During evolution, circuit functionality is improved by checking circuit quality, defined by a fitness function which sets the optimization criteria to follow. In this sense, circuits are automatically generated by combining small building blocks (tiny processing elements) into an array structure, whose contents are decided autonomously by evolutionary rules. Every iteration requires new circuits to be generated by using partial reconfiguration. A live demo will also be provided in this case, with an image processing/filtering application which gathers many properties of evolvable HW. Optimized reconfiguration engines allow over 100,000 circuit evaluations/second, with high processing speeds over 400 Mpixels/second. Also, the fact of self-evolving on the reconfigurable array provides self-healing capabilities, which will be shown in the demo by means of artificially injecting faults on the array, and observing how the system reacts to circumvent these faults.

Tutorial Speaker SBCCI (Tuesday, 30th of August 2016)

Rajeev Ranjan

Cadence Design System, Inc. (USA)

Topic: Accelerating SoC Design and Verification with Formal Technology

Bio: *Rajeev Ranjan is leading the business development efforts of a newly formed business unit at Cadence following the acquisition of Jasper Design Automation, where he was the CTO and was responsible for developing Jasper's overall technology vision and driving the business value of formal.*
Rajeev has been active in the area of formal verification for over 20 years. He has served in the organization and program committee of many international conferences including DAC, ICCAD, FMCAD, and CHARME. He has published numerous articles and has 12 patents in the area of functional verification. Rajeev received his Bachelor's degree from Indian Institute of Technology, Kanpur (aka IIT Kanpur), his Master's degree from University of Illinois at Urbana-Champaign (aka UIUC), and his doctorate degree from University of California at Berkeley (aka UC Berkeley). He also has an MBA degree from Wharton School of Business with a focus on entrepreneurial management and finance.

Abstract: Over the last decade, formal verification technology has made significant impact in bringing quality and productivity gains in SoC design and verification flow – ranging from architectural modeling to RTL development to SoC integration all the way to post-silicon debugging. Today, a variety of targeted verification tasks, e.g. register verification, x-propagation verification, connectivity verification, etc. can be performed solely by formal verification technology without depending on a complementary simulation flow. Verifying security attributes of an SoC is emerging as a challenging area as the IoT era dawns upon us. While the security risks in a system pertain to potential flaws in both hardware and software components, establishing hardware security is critical, because it forms the foundation for secure applications and a security hole in hardware implementation can compromise the entire system.
In this talk, we will first provide a brief overview of formal technology and its applications, followed by a broader discussion on the scalable methods of applying formal technology for hardware security verification.

Tutorial Speaker SBCCI (Tuesday, 30th of August 2016)

Bertrand Saillet

Unitec Semicondutores (Brazil)

Topic: Yield learning of CMOS technology during development and mass production

Bio: *Bertrand Saillet is Technology Integrator at Unitec Semicondutores, a Brazilian company developing Integrated Circuits and owning the largest and most modern semiconductor fab in the southern hemisphere. Before joining Unitec, he developed, introduced, and managed a large number of technologies and products into semiconductor fabs by working at LFoundry as Yield and Process Integration manager from 2010 to 2014, Atmel as Yield manager from 2006 to 2010 and previously ST Microelectronics as research engineer. Mr Saillet is a Microelectronics and Telecommunication engineer graduated from Polytech' Marseille and received a Master degree in Nano-electronics and Science Engineering from Aix-Marseille University in France.*

Abstract: Yield is defined as the number of products that can be sold relative to the number of products started. Yield is a quality metric, and high Yield is a major goal of semiconductor operations as it directly impact costs. Semiconductor operations use to monitor and enhance line yields and die yields. The tutorial will focus on die yields, defined as the number of good dice passing wafer probe testing from wafers that reach that part of the process. It will describe how product achievable yields are being evaluated and how yields are improved over time from early development to mass production.

Tutorial Speaker SBCCI (Tuesday, 30th of August 2016)

Shishpal Rawat

Intel Corporation (USA)
Accellera Systems Initiative Chair

Topic: IEEE/CEDA

Bio: *Mr. Shishpal Rawat has been the Chairman of the Board at Accellera Organization Inc. since July 2010. Mr. Rawat served as a Director of EDA Investments and ArchPro Design Automation, Inc. He serves as a Director of Business Enabling Programs with the Design Technology Solutions group, Intel. He has been at Intel for 22 years and has held a variety of Design and CAD management positions. He holds M.S. and Ph.D. degrees in Computer Science from Pennsylvania State University, University Park, and a B.Tech. degree in Electrical Engineering from Indian Institute of Technology, Kanpur, India.*

Abstract: TBD

Tutorial Speaker EDS Workshop
(Monday, 29th of August 2016)

Patrick Fay

University of Notre Dame (USA)

Topic: Advances in III-V Heterostructure Devices and Integration for Millimeter-Wave and THz Sensing and Imaging

Bio: *Patrick Fay is a Professor in the Dept. of Electrical Engineering at the University of Notre Dame. He received a Ph.D. in electrical engineering from the University of Illinois at Urbana-Champaign in 1996. His research interests include the design, fabrication, and characterization of compound semiconductor electronic devices and circuits, as well as high-speed optoelectronic devices and optoelectronic integrated circuits for fiber optic telecommunications. His research also includes the development and use of micromachining techniques for the fabrication of microwave through sub-millimeter-wave components and packaging. He established the High Speed Circuits and Devices Laboratory at Notre Dame that houses comprehensive device and circuit test capabilities. He also oversaw the design, construction, and commissioning of the class 100 cleanroom housed in Stinson-Remick Hall at Notre Dame, and has served as the director of this facility since 2003. Prof. Fay is a fellow of the IEEE, has published 9 book chapters, more than 130 articles in refereed scientific journals, and more than 180 conference proceedings.*

Abstract: The exploration of novel devices and integration technologies, in conjunction with nanometer-scale device geometries enabled by advanced fabrication processing, has the potential to lead to significant improvement in the performance of III-V electronic devices for sensing and imaging applications. In this talk, several device technologies being pursued at the University of Notre Dame will be described. In terms of conventional device scaling, recent advances in scaled GaN-based HEMTs will be presented; experimentally-demonstrated ft's of over 370 GHz indicate that GaN-based devices are not only attractive for microwave power amplification, but also for millimeter-wave and mixed-signal circuit applications as well. Fundamental studies also reveal signatures of plasma waves in GaN-channel HEMTs, suggesting additional avenues for high-frequency device design and optimization. For millimeter-wave and THz detection and imaging, we have been investigating the use of InAs/AlSb/GaSb heterostructure backward diodes. These devices offer extremely low noise performance, have demonstrated record sensitivity performance, and can be integrated monolithically with antennas for focal plane arrays and to implement higher-level imaging and sensing functionalities such as polarimetric and spectroscopic imaging. An overview of this device technology as well as opportunities and challenges will be presented. Finally, the fabrication and performance of a novel interconnect technology that achieves extremely low loss, compact chip-to-chip interconnects for millimeter-wave and THz system integration will be described.

Tutorial Speaker EDS Workshop
(Monday, 29th of August 2016)

Fernando Guarín

Global Foundries (USA)

Topic: Reliability challenges for the qualification of Leading Edge CMOS Technologies

Bio: *Dr. Fernando Guarín is a Distinguished Member of Technical Staff at Global Foundries in East Fishkill NY and Adjunct Lecturer at SUNY New Paltz. He retired from IBM's SRDC after 27 years as Senior Member of Technical Staff. He earned his BSEE from the "Pontificia Universidad Javeriana", in Bogotá, Colombia, the M.S.E.E. degree from the University of Arizona, and the Ph.D. in Electrical Engineering from Columbia University, NY He has been actively working in microelectronic reliability for over 35 years.*
From 1980 until 1988 he worked in the Military and Aerospace Operations division of National Semiconductor Corporation. In 1988 he joined IBM's microelectronics division where he worked in the reliability physics and modeling of Advanced Bipolar, CMOS and Silicon Germanium BiCMOS technologies.
Dr. Guarín is an IEEE Fellow, Distinguished Lecturer for the IEEE Electron Device Society, where he has served in many capacities including; member of the IEEE's EDS Board of governors, chair of the EDS Education Committee, Secretary for EDS. He is the EDS President-Elect 2016-2017.

Abstract: This presentation will address some of the key reliability challenges during the qualification of a 14nm SOI CMOS technology. Some of the issues are driven by self-heating in SOI and some by the latest trends in semiconductor fabrication as we continue to scale and deal with the new reliability challenges introduced by the use of High K Metal Gate (HKMG) and FinFet devices. We will discuss the reliability impact and the qualification activities driven by the introduction of SOI and new materials. . The path to maintaining the advanced CMOS scaling cadence and new reliability limiting factors will be examined from the reliability perspective. A closer look will be given to Hot Carriers, Bias Temperature Instabilities and Gate Dielectric Integrity. The characterization, models and qualification methodologies will be put in the required perspective for the successful qualification and transfer of leading edge technologies to a manufacturing environment.

Tutorial Speaker EDS Workshop
(Monday, 29th of August 2016)

Enrico Sangiorgi

Università di Bologna (Italy)

Topic: Micro- and nano-power management circuit systems for energy harvesting

Bio: *Enrico Sangiorgi received the Laurea degree from the University of Bologna in 1979. He has been a Visiting Scientist at Stanford University and Bell Laboratories, Murray Hill, NJ. In 1993, he was appointed Full Professor of Electronics at the University of Udine, Italy. In 2002, he joined the University of Bologna, where he has been Dean of the Faculty of Engineering, Director of the EE Department "Guglielmo Marconi" and currently Vice-Rector for Teaching and Education. He has been Editor of Electron Device Letters, on the editorial board for the Transactions on Electron Devices and Journal of Photo-Voltaics. His research covers various device modeling and characterization aspects. Enrico Sangiorgi is a Distinguished Lecturer and a Fellow of the IEEE; he has been Chairman of the EDS TCAD Technical Committee, member of the Cledo Brunetti Award , the Education Award, and the Fellow Committees of the EDS.*

Abstract: The present interest on pervasive sensor networks and the steady development of electronic devices with low power consumption motivates the research on electronic systems capable of harvesting energy from the surrounding environment. In this scenario, mechanical vibrations, thermal gradients, and photovoltaics represent the most promising power sources.
A special care has to be devoted to the design of power conversion and management circuits for energy harvesting applications where, in many practical cases, the available power is often as low as few µW. This talk will review a series of design techniques that ensure ultra-low intrinsic consumptions and pursue effective trade-offs with conversion efficiency. Practical cases based on both integrated and off-the-shelf electronics will be discussed.

Tutorial Speaker EDS Workshop
(Monday, 29th of August 2016)

Cor L. Claeys

IMEC (Belgium)

Topic: Challenge of Advanced Semiconductor Devices for future CMOS Technologies

Bio: *Cor Claeys received the Ph.D. degree from KU Leuven in Belgium, where he is Professor since 1990. At imec he is presently Director of Advanced Semiconductor Technologies responsible for strategic relations. His main interests are silicon technology, device physics, low frequency noise phenomena, radiation effects and defect engineering and material characterization. He co-edited a book on "Low Temperature Electronics" and "Germanium-Based Technologies: From Materials to Devices" and wrote monographs on "Radiation Effects in Advanced Semiconductor Materials and Devices" and "Fundamental and Technological Aspects of Extended Defects in Germanium". Two of these books have translated in Chinese. He authored and coauthored 14 book chapters, over 1000 conference presentations and more than 1200 technical papers. He is also editor or co-editor of 60 Conference Proceedings. Prof. Claeys is a Fellow of the Electrochemical Society and of IEEE. He was the Founder of the IEEE Electron Devices Benelux Chapter, Chair of the IEEE Benelux Section, an elected AdCom Member of the Electron Devices Society and the EDS Vice President for Chapters and Regions. He was EDS President in 2008-2009. He was as Division Director on the IEEE Board of Directors in 2012-2013. He is a recipient of the IEEE Third Millennium Medal and in 2013 he received the IEEE EDS Distinguished Service Award. Within the Electrochemical Society, he was the Chair of the Electronics & Photonics Division from 2001 to 2003. In 2004, he received the Electronics & Photonics Division Award.*

Abstract: Advanced devices are not only driven by minimum device geometry, performance enhancement and cost issues, but also require a low power consumption. This is achieved by optimizing process modules, introduction of new materials and modified device concepts. This led to the implementation of stress engineering, ultra-shallow junctions, gate-stacks with EOT's below 1 nm, optimization of process sequences (e.g. gate-first versus replacement gate or gate-last), raised source/drain for resistance control, etc. Improved drive currents and electrostatic control triggered the exploration of Multi-gate devices (MuGFETs). For scaled-down technologies, FD technologies with ultra-thin body and buried oxide (UTBB SOI) have demonstrated their strong potential down to the 14 nm mode. At those dimension there exists a strong competition between planar UTBB SOI and bulk FinFETs. Tunnel-FETs (TFETs), relying on band-to-band-tunneling and allowing to achieve steep subthreshold swings are studied. Both horizontal and vertical TFET approaches are emerging as post-CMOS alternatives. Further scaling leads to gate-all-around and nanowire devices. Optimized epitaxial growth techniques resulted in the fabrication of Ge (p-channel), III-V (n-channel) or hybrid Ge/III-V devices on a Si substrate. These high mobility materials are also implemented in TFET and nanowire structures. Beyond CMOS technologies will be based on alternative technologies such as 2D materials, quantum computing and spintronics. The paper reviews the status and the challenges of several of these advanced technologies and outlines potential limitations.

Tutorial Speaker SBMicro (Tuesday, 30th of August)

Tayeb Mohammed-Brahim

Université de Rennes (France)

Topic: Flexible electronics: the new way towards friendly applications

Bio: *Tayeb Mohammed-Brahim is currently professor in Rennes 1 University (France), Head of Microelectronics & Microsensors Department of the Institute of Electronics and Telecommunications of Rennes and Director of the Common Center on Microelectronics in the west of France. He got his PhD (Doctorat d'Etat) in Paris-XI University (France) and he founded the thinfilm Laboratory in Algiers University (Algeria). Then he moved to Caen University (France) where he created the reliability Laboratory. After that and since 2000, he moved to Rennes University where he became the head of Microelectronics Group becoming the Microelectronics and Microsensors Department after 2002.*
He is mainly involved in low temperature fabrication of thin film electronic devices for flexible electronics and in the fabrication of sensors. Previously he activated a lot on chemical and biologic sensors for the measurement of pH, the detection of DNA and the quantification of proteins. Presently, his main activities focus on mechanical sensors for health applications. He is author of more than 300 papers on these different fields.

Abstract: Flexible electronics is the new paradigm, enlarging the applications of electronics to new fields as health, transport, robotics,…Huge works are devoted now to this electronics involving great number of ways. Different materials from known silicon to multiple organic materials and renewed metal oxides are used. Different techniques from known photolithography to new deposition in solution ones are used also. The main drawback of a lot of ways is the lack of reproducibility in the process and/or of reliability of the devices.
The tutorial is a critical review of these ways focusing on the process reproducibility and the device reliability. Examples of the most important success in this story are given. Applications of the devices in different fields, health particularly, are briefly described.

Tutorial Speaker SBMicro (Tuesday, 30th of August)

Lorenzo Faraone

The University of Western Australia (Australia)

Topic: Infrared optoelectronics technology:
Materials and devices for detectors and imaging applications

Bio: *Professor Faraone is a Member of the Order of Australia (AM), and a Fellow of the Institute of Electrical and Electronic Engineers (FIEEE), Australian Academy of Science (FAA) and the Australian Academy of Technological Sciences and Engineering (FTSE). He has published more than 250 international journal papers on his research work, and supervised more than 35 PhD student completions. He is currently Head of the Microelectronics Research Group (MRG) at The University of Western Australia (UWA), and Director of the WA Centre for Semiconductor Optoelectronics and Microsystems (WACSOM). Prior to joining UWA in 1987, he worked primarily in the area of silicon CMOS-based microelectronics and non-volatile memory technology with RCA Labs in Princeton, NJ, USA. Since joining UWA he has worked on compound semiconductor materials and devices, including AlGaN/GaN HEMTs, HgCdTe-based infrared sensor technology and MBE growth, as well as optical MEMS technologies for infrared spectroscopy and imaging applications. His research activities also include mobility spectrum techniques for magneto-transport studies, which allow the transport properties and mobility distributions of individual carriers in multi-layer/multi-carrier semiconductor systems to be determined.*

Abstract: This tutorial will review the current status and future trends in infrared optoelectronics technology: from material requirements to detector and imaging focal plane array technologies, as well as applications in areas such as defence, security & aerospace, food & agriculture, biomedical diagnostics, process control, etc. In particular, this tutorial will focus on high-performance technologies suitable for remote sensing and spectroscopic applications, as well as large-format 2-D focal plane array technologies for night vision and hyperspectral imaging applications.
The tutorial will be presented in a format that should be suitable for anyone interested in the general area of infrared optoelectronics technology, and will be at a level suitable for non-specialists. The only requirement will be a general knowledge of semiconductor materials and devices at a university undergraduate level.

Tutorial Speaker SBMicro (Tuesday, 30th of August)

Mehmet Kaynak

Innovations for High Performance Microelectronics – IHP (Germany)

Topic: Future of SiGe BiCMOS Technologies with "More-than-Moore" Modules for mm-wave and THz Applications

Bio: *Dr.–Ing Mehmet Kaynak received his B.S degree from Electronics and Communication Engineering Department of Istanbul Technical University (ITU) in 2004, took the M.S degree from Microelectronic program of Sabanci University, Istanbul, Turkey in 2006 and received the PhD degree from Technical University of Berlin, Berlin Germany in 2014. He joined the technology group of IHP Microelectronics, Frankfurt (Oder), Germany in 2008. Dr. Kaynak has received the young scientist award of Leibniz institute for the year of 2014. Since 2015, he is acting as the department head of technology group at IHP, Germany and network faculty member at Sabanci University, Turkey.*

Abstract: In last decade, SiGe BiCMOS technologies open a new cost-efficient market at mm-wave frequencies. Starting with the commercial use of automotive radars at 77 GHz, the market now has a strong interest on radar, sensor and imaging products at mm-wave and sub-THz frequencies. The latest developments on SiGe HBTs with fmax of beyond 600 GHz boosts the research and development effort on circuit and system area to take share from the new market. In parallel to the developments on SiGe HBT performance, "More-than-Moore" path, which covers all the additional functionalities to the standard CMOS process (i.e. MEMS devices, microfluidics, etc…), allows to realize multi-functional circuits and systems.
In this talk, the latest developments regarding the high-speed devices and circuits based on SiGe HBTs will be discussed. The "More-than-Moore" modules for multi-functional device and circuits will also be one of the core topic of discussion.

Tutorial Speaker SBMicro (Tuesday, 30th of August)

Yeshaiahu Fainman

University of California San Diego (USA)

Topic: Nanophotonics Technology and Applications

Bio: *Professor Fainman received the Ph. D. from Technion in 1983. He is a Cymer Professor of Advanced Optical Technologies and Distinguished Professor of ECE at the University of California, San Diego (UCSD). His current research involves near field optical science and technology, nanophotonics, nanolasers, nanoiplasmonics and ultrafast optics. He is a Fellow of OSA, IEEE, and SPIE. He Chaired, co-Chaired and served on numerous program committees for various conferences for OSA, IEEE/LEOS, and SPIE. He is a recipient of the Miriam and Aharon Gutvirt Prize, Technion, Haifa, Israel (1982), Lady Davis Fellowship (2006), Brown award (2006), Gabor Award (2012) and E. Leith Medal (2015). He served as a topical editor and board member for various journals. He contributed over 250 manuscripts in peer review journals and over 450 conference presentations and conference proceedings.*

Abstract: Various future system applications that involve photonic technology rely on our ability to integrate it on a chip to augment and/or interact with other signals (e.g., electrical, chemical, biomedical, etc.). For example, future computing and communication systems will need integration of photonic circuits with electronics and thus require miniaturization of photonic materials, devices and subsystems. Another example, involves integration of microfluidics with nanophotonics, where former is used for particle manipulation, preparation and delivery, and the latter in a large size array form parallel detection of numerous biomedical reactions useful for healthcare applications. To advance the nanophotonics technology we established design, fabrication and testing tools. The design tools need to incorporate not only the electromagnetic equations, but also the material and quantum physics equations to include near field interactions. These designs are integrated with device fabrication and characterization to validate the device concepts and optimize their performance. Our research work emphasizes the construction of passive (e.g., engineered composite metamaterials, filters, etc.) and active (e.g., nanolasers) components on-chip, with the same lithographic tools as electronics. In this talk, we discuss some of the passive metamaterials and devices that recently have been demonstrated in our lab. These include our recent results on nanoscale engineering optical nonlinearities with SOI material platform and design, fabrication and testing of nanolasers constructed using metal-dielectric-semiconductor resonators confined in all three dimensions.