Wednesday, August 30th

14:00 – 15:20 Low Power Design and Verification Bootcamp by Cadence

15:40 – 17:00 Low Power Design and Verification Bootcamp by Cadence

Thursday, August 31st

9:00 – 11:00 State-of-the-art Industry Verification Flow Bootcamp by Ensilica

11:20 -13:00 State-of-the-art Industry Verification Flow Bootcamp by Ensilica

Friday, September 1st

8:40 – 9:40 Test & Measurement Training: Rohde & Schwarz

9:40 – 10:40 Test & Measurement Training: RIGOL

12:00 – 12:20 Industrial session – Ensilica

12:20 – 12:40 Industrial session – Telemetry

12:40 – 13:00 Industrial session – Chipus

13:00 – 13:20 Industrial session – Instituto Eldorado

14:40 – 15:00 Title : An Ultra-Low Power Management Unit for Implantable Biomedical Applications
Authors : Mateus Castro, Tito Burini, Aline Rocha, Karine Santos, Ricardo Valero Castro, José Andrade and Fernando Chavez

15:00 – 15:20 Title : A 500-S/s 8-b 1-V Low Power SAR ADC With 49.92-dB SNR Using a Straightforward Layout Technique in 180-nm CMOS
Authors : Ricardo Valero Castro, Karine Santos, José Alberto Andrade, Mateus Biancarde Castro, Fernando Chavez, Tito Burini and José Bohorquez

15:20 – 15:40 Title : Power impact of data gating multiplier modules in a RISC-V core
Authors : Kaio Fernandes and Lucas Wanner