**IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology**

**Title: UFSC LRF MULTIPROJECT**

**Adviser Professor(s):** Fernando Rangel de Sousa

**Students involved (names and aimed degrees):** Rodrigo Eduardo Rottava, MsC

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**Institution (University/Faculty):** Universidade Federal de Santa Catarina

**Type of Circuit Design:** () Digital; (x) mixed signal; () analog; (x) RF

**Date of the circuit tape-out of the run:** 10/2014

**Date of receiving the chips at your institution:** 04/2015

**Date of the report and/or of later up-date:** 02/2016

**Short Description of the circuit: (function, proposed innovation, number of transistors, passive components, drawing of the chip, etc)**

There are two main circuits in this design: an oscillator and an *LC* tuner.

We designed an efficient oscillator to feed a 50 Ohms load. This oscillator uses two positive-feedback techniques simultaneously in order to increase conversion efficiency (from DC to AC). The first feedback is provided by a conventional common-gate Colpitts topology. The second one is a gate-inductive-regeneration which maximizes the amplitude of the signal applied to the gate-source terminals. By passively amplifying this signal, the conduction angle of the main transistor is narrowed, which in turn increases efficiency. The DC supply is fully applied to the main transistor via RF chokes, to reduce power dissipation in other active components besides the main transistor. The circuit was designed based on two parameters, a Colpitts feedback coefficient and a gate-inductive-degeneration feedback coefficient. These coefficients were optimized through simulation aiming at increasing the conversion efficiency. The circuit is composed by two nFET transistors, seven capacitors (four of them only for signal decoupling), three inductors, and one resistor. It has five pads: two for supplying (vdd and gnd), and three for extracting the signal (coplanar gnd-signal-gnd). The frequency of oscillation is 2.4 GHz, and post-layout simulation resulted in a conversion efficiency between 25 and 30 %. The total area of this circuit is 0.77 mm².

The 125-kHz *LC* tuner is based on negative resistances used to increase the quality factor of an *LC* network. Using an analog amplitude detector a digital finite state machine decides which capacitance configuration tunes the network. The design novelty is the use of the negative resistance structure to help in the tuning procedure allowing a relatively small area tuning system. The capacitors bank and the *LC* network required to test this tuner are off-chip. Roughly, the complete design has 760 CMOS transistors and 3 MIM capacitors are used in a 46 um x 116 um area.

We can see the complete layout of both systems in the figure below. The cells marked in red were made to help with the test of the *LC* tuner. Cell number 1 consists of a pMOS cross coupled pair, cell 2 has the analog blocks of the tuner (that occupies a 30 um x 50 um area), and cell 3 involves the complete *LC* tuner. The cell in blue encloses the 2.4 GHz oscillator.

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| **Complete Circuit layout** | |
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| **Zoom of the circuit layout divided in blocks.** | **Microphotograph of a received die with 1500 um x 1500 um.** |

**Main results and representative performance data or curves, picture of the IC, does circuit function as expected, etc**

We started testing the IC with the pMOS cross coupled pair and we made the test bench of the figure below. In this figure, *IT* is the tail current and vin is a sinusoidal voltage signal with 125 kHz. Then we plotted the expected and measured cross coupled pair parallel resistance versus vin at 125 kHz as seen in the figure below. We noted that for larger input voltages the resistance did not follow the expected. After weeks of investigation, we concluded that it happened due to a current leakage through the pad ring when vin increases. Actually we obtained the same leakage when we increased the voltage on a pad that is not connected to anything inside the chip. Due to this current leak the tests were aborted.

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| PMOS cross coupled pair | Measured and expected parallel resistance |

**Main challenges and difficulties encountered during design, submission, import process and measurements of the circuit.**

Since it was our first design with this technology we encountered difficulties for making the ESD protection and the pad ring. The documentation available was not clear for complex situations as that of our RF/mixed circuit. Several interactions with the support were done, however, the understanding was not easy at a first moment. A new version of the pad ring was made and the circuit was resubmitted in 10/2015.

**Resulting publications (submitted, accepted or published) and degrees earned by students**

We expect to advance in this direction after receiving and testing the new prototypes.