IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology

A. **Title of the Circuit(s)**: *ITA – Interval Type-2Fuzzy Logic Blocks*
   1. Low Power Analog Interval Type-2 Fuzzy Membership Function Generator;
   2. Interval Type-2 Fuzzy Controller Output Processing, Using the Nie-Tan Method.

B. **Advisor Professor**: Prof. Dr. Lester de Abreu Faria

C. **Students involved (names and aimed degrees)**: Gabriel Antonio Fanelli de Souza (Master's degree) and Rodrigo Bispo dos Santos (Master's degree)

D. **Institution (University/Faculty):** Instituto Tecnológico de Aeronáutica - ITA

E. **Type of Circuit Design**: ( ) Digital; ( ) mixed signal; **(X) analog**; ( ) RF
   Date of the circuit tape-out of the run: 23/03/2016
   Date of receiving the chips at your institution: 12/08/2016
   Date of the report and/or of later update: 24/03/2017

F. **Short description of the circuit**: (function, proposed innovation, number of transistors, passive components, screen shot of the chip layout, etc.)

Considering that Type-2 fuzzy controllers are composed of five main blocks (Fuzzifier, Inference Engine, Rule Base, Type-reducer, and Defuzzifier) in this IC we implemented two main blocks/circuits: a fuzzifier and a defuzzifier circuits (the latter performing the functions of a Type-reducer and a Defuzzifier). Both are novel architectures and are the focus of Master's Thesis.

The first block of the controller – the fuzzifier, also called membership function generator – must be able to output a membership function in the form of an interval type-2 fuzzy set. This circuit presents a novel architecture for a type-2 fuzzifier that, unlike the previous type-2 fuzzifier circuits, is capable of generating a membership function without the need of a level shifter circuit nor of a second identical block. The Footprint of Uncertainty (FOU), which is characteristic of an interval type-2 fuzzy set, is generated using a current steering mirror controlled by a voltage input, allowing a width variation based on a central line. This characteristic makes the circuit inherently type-2, i.e., not dependent of a type-1 fuzzifier and is not only simpler, but smaller in area, and less power-consuming.

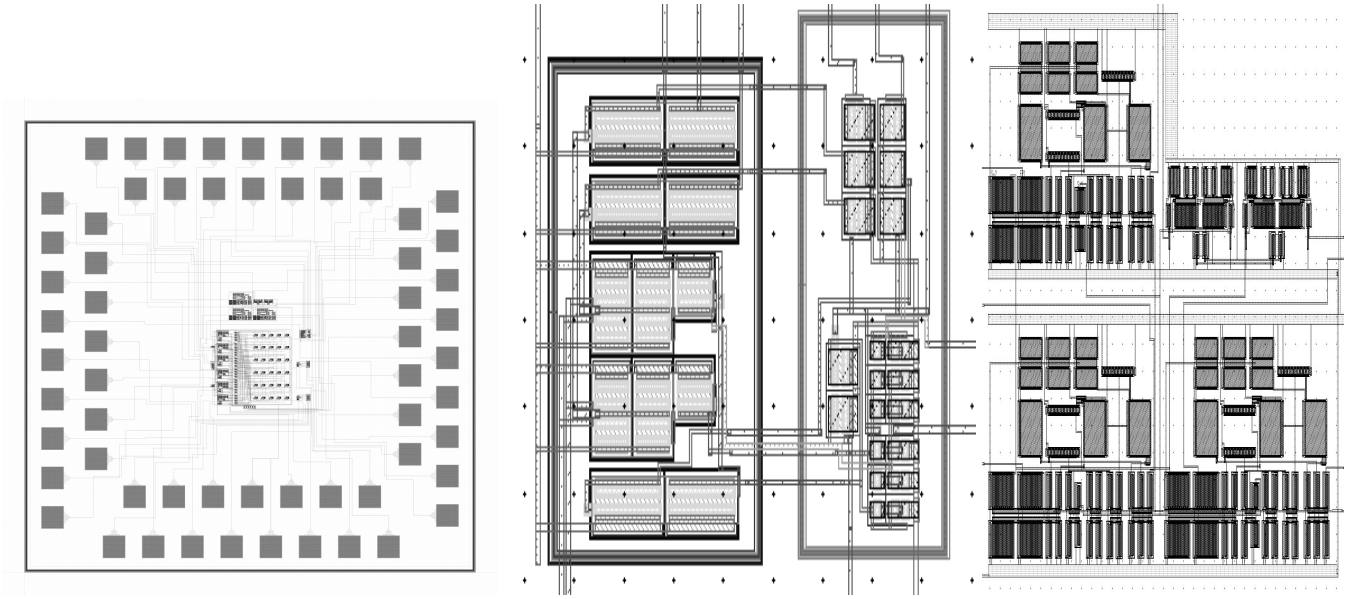
The second circuit is an Interval Type-2 Fuzzy Controller Output Processing, using the Nie-Tan Method. The NT output processing consists of both Type-reducer and defuzzifier operations (blocks). The reduction-type operation is done in order to obtain a type-1 fuzzy set, similar to the type-2 fuzzy set obtained from the rules of the inference circuit. The equation below presents the operation that must be performed in order to obtain the actual value (crisp) directly from the activation degrees, belonging to the type-2 fuzzy sets.

$$Y_{NT} = \sum_{i=1}^{i=N} \frac{x_i\left(\overline{f}_i + \underline{f}_i\right)}{\overline{f}_i + \underline{f}_i} \qquad (1)$$

Expanding (1) and adopting $f_i \equiv I_i$ as the degree of activation of the membership function, we have:

$$I_{NT} = \frac{\left[I_{p1}\left(\underline{I}_1 + \overline{I}_1\right) + I_{p2}\left(\underline{I}_2 + \overline{I}_2\right) + I_{p3}\left(\underline{I}_3 + \overline{I}_3\right)\right]}{\left(\underline{I}_1 + \overline{I}_1\right) + \left(\underline{I}_2 + \overline{I}_2\right) + \left(\underline{I}_3 + \overline{I}_3\right)} \qquad (2)$$

that is the operation to be performed by the circuit that was implemented. Figure 1 (a, b and c) presents the layout of the prototyped circuits.



(a) (b) (c)

Figure 1 – IC layout. (a)Complete Layout; (b) Fuzzifier Layout; and (c) Defuzzifier Layout.

G. **Main results and representative performance data or curves, picture of the IC, does circuit function as expected, etc.**

Figure 2(a) shows how the membership function generator circuit (Circuit #1) was capable of generating different type-2 membership functions, while Figure 2(b) shows the power consumption profile of the triangular membership function. Both figures were traced in MatLab Software, based on the data acquired in the experimental measurements.

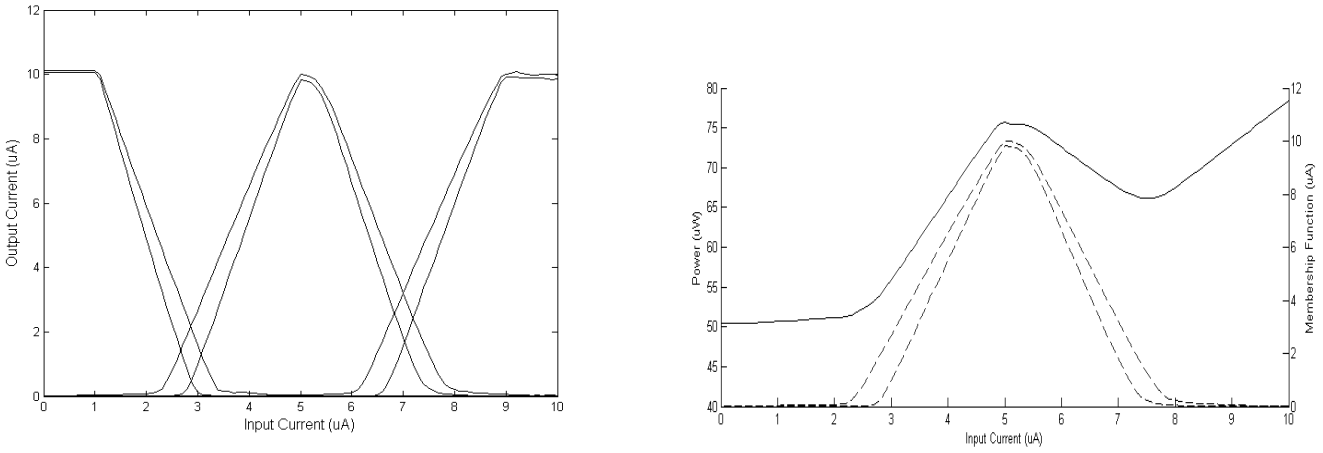


Figure 2 – (a) Different fuzzy type-2 membership function shapes (S, Z and triangular, overlapped in the same figure); and (b) Triangular shape power consumption profile.

The results confirm not only the potential to generate different kinds of membership functions (figure 2) but also the low power characteristic of the circuit (figure 3), with an average power consumption of only 72,56 µW, both considering Circuit #1.

Considering Circuit #2, figure 3(a) presents the results obtained with the NT Method Direct Defuzzification circuit. It shows the results obtained by varying the degree of activation of the circuit from 15uA to 60uA. As a minimum error of 5% was stipulated, the reliable operating range of the circuit was defined as being from 15uA to 50uA. On the other hand, Figure 3(b) shows the power consumption for the circuit. Considering the previously acquired operating range of the circuit (from 15uA to 50uA), it was measured that the minimum power was approximately 170 uW and the maximum power is 550uW.

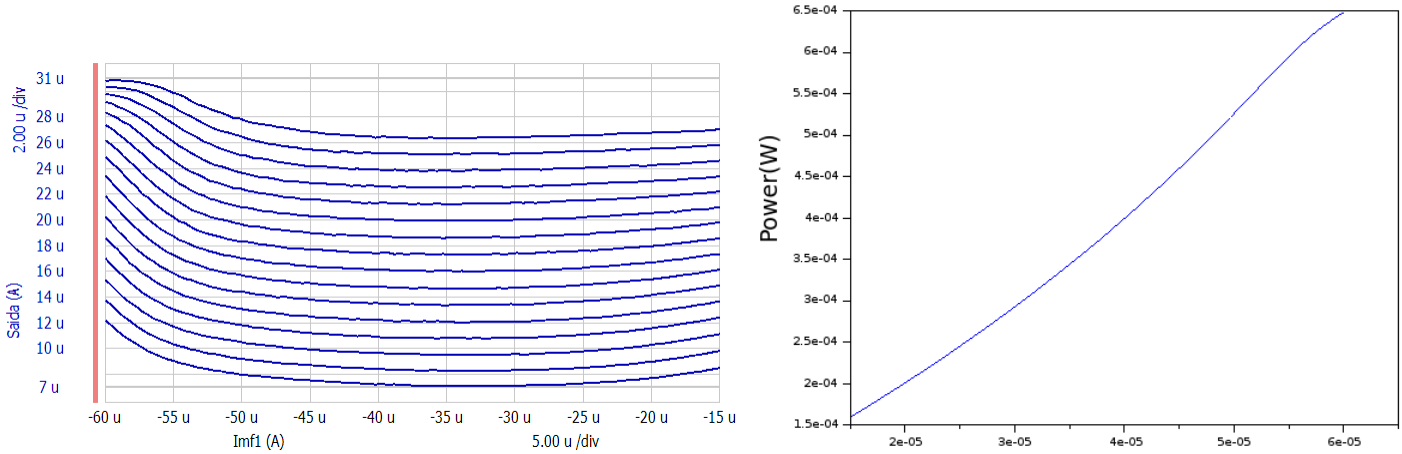


Figure 3: (a) Defuzzification Output for the NT Method; and (b) Power Consumption for the NT Method Circuit

H. Main challenges and difficulties encountered during design, submission, importing process and measurements of the circuit.

The main challenge faced during the layout design was the integration with the PAD structure. The PAD library provides only the phantom view of the layout. Therefore, it created some confusion on how to import and to use it in our design. With the assistance of Prof. Jacobus Swart and Mr. Tobias Vanderhenst, we were able to understand how the phantom view should be used, but eventually opted for using a different PAD structure, kindly provided by Prof. Salvador Gimenez and his team (FEI – SP).

I. Resulting publications (submitted, accepted or published) and degrees earned by students.

IV Congresso Brasileiro de Sistemas Fuzzy (CBSF). November 16th to 18th 2016. Campinas- SP, Brazil. Download in www.ime.unicamp.br/~cbsf4

1. "Fuzificador Analógico baseado em Lógica Fuzzy Tipo-2 Intervalar utilizando "current steering". - Published
2. "Implementação em hardware analógico de um módulo de processamento de saída de controlador Fuzzy tipo-2 intervalar segundo o método Nie-Tan". – Published

XVIII Simpósio de Aplicações Operacionais em Áreas de Defesa (SIGE). September, 28th to 30th, 2016. São José dos Campos- SP, Brazil. Download in www.sige.ita.br.

3. "Projeto e Layout de um Circuito Analógico Gerador de Funções de Pertinência Fuzzy tipo-2". - Published
4. "Desenvolvimento e Implementação em Hardware com Componentes Discretos de um Processo de Saída de Controlador Fuzzy tipo-2 Intervalar". Published

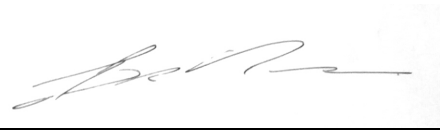
IEEE Transactions on Circuits and Systems for Video Technology

5. "A novel Analog Interval Type-2 Fuzzifier Architecture for Dedicated Real-Time Pattern Recognition Systems". - Submitted

I. Gabriel Antonio Fanelli de Souza has already earned his Master's degree, in February, 2017; and

II. Rodrigo Bispo dos Santos is already pursuing his Master's degree. He Will be presenting his Thesis up to July, 2017.

March, 24th, 2017



Lester de Abreu Faria - Prof. Dr.
Advisor