**IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology**

Title of the Circuit: Fully Integrated Class J Power Amplifier for IEEE 802.11g/n

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Institution (University/Faculty): Universidade Federal do Rio Grande do Sul/ PGMicro

Type of Circuit Design: ( ) Digital; ( ) mixed signal; ( ) analog; (X) RF

Date of the circuit tape-out of the run: 23/03/2016

Date of receiving the chips at your institution: 03/09/2016

Date of the report and/or of later update: 23/08/2017

**Description**

The CMOS PA market has been steadily growing motivated by the high integrability and low cost of the technology, but CMOS PA design is challenging and require several innovative techniques to achieve high output power and linearity required by modern communication standards, one of which is power combining.

This amplifier design was proposed by Gabriel Guimarães during his M.Sc. studies at UFRGS, he was assisted by Diogo Santana, a Ph.D. student that had previously worked with RFPAs. The objective of this design is to make the first fully integrated CMOS PA design at the group, and the first linear PA. The design is focused on 802.11g standard.

The block-level diagram of the proposed amplifier is shown in Fig. 1. In this circuit two differential active cores are combined in a series combining transformer (SCT) to produce a single-ended output signal. Both VDD and the ground signals are supplied through AC grounds to make the circuit more insensitive to bondwire parasitics. The center-tap of the SCT is used to create a 2nd-harmonic tuned bypass, the original objective was for the 2nd-harmonic network to enhance this harmonic and make a class-J PA as described in Steve Cripps RF Power Amplifiers for Wireless Communications, 2nd Edition. To the authors knowledge this was only achieved in discrete PAs so far and never in a fully integrated configuration. This class-J condition was not satisfactorily achieved in this first prototype, so a class-AB condition was restored for the active cores for tapeout.



Figure 1 - CMOS PA top-level schematics

**Results**

 The chip photograph can be seen in fig. 2. The circuit is intended to be measured in a chip-on-board (CoB) configuration where the bias pads are connected to a PCB and the RF signal is accessed through GSG RF microprobes, an alternative test configuration would have the RF signals connected to the board for the measurement of the impact of bondwire parasitics on signal path. A first PCB was manufactured and one chip was attached and bonded to it as can be seen in fig. 3, but the PCB contacts were high-resistivity contacts that made the measurements impossible. This was due to metallurgic problems with the gold wires being bonded to a common HASL surface finish. A second PCB with ENIG surface finish is being developed for the chip measurement. Nevertheless, circuit electromagnetic simulation results were published in the NEWCAS 2017 conference and are present in the master thesis of Gabriel Guimarães.



Figure 2 - chip photograph



Figure 3 - first PCB with CoB

**Why Europractice?**

Europractice through the mini@sic provide us with a unique opportunity for students such as the ones involved with this work to have access to fabrication in technologies such as 180nm CMOS, this makes works like this possible in a low-cost academic environment. Europractice offers timely support during the tapeout that is essential for the designers and reduce the necessary time for chip verification.

**Acknowledgement**

 We would like to thank the Federal University of Santa Catarina for access to wirebonding, ITT-Chip institute in Unisinos that helped with the debugging on the first CoB board, the CI-Brasil program for EDA support and also CNPq and CAPES for funding.

**Publications and Degrees**

GUIMARAES, G.; KLIMACH, H.; BAMPI, S.; "A Fully Integrated CMOS 2.4GHz and 24dBm Linear Power Amplifier." in 15th IEEE NEW CIRCUITS AND SYSTEMS CONFERENCE (NEWCAS), 2017, Strasbourg, France

Teófilo Neves Guimarães, Gabriel; Advisor: Advisor: Hamilton Klimach; Coadvisor: Eric Fabris. CMOS linear RF power amplifier with fully integrated power combining transformer. Master’s thesis, 2017.