**IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology**

**Title of the Circuit:** SUBCIRCUITS FOR BLUETOOTH LOW-ENERGY RECEIVER

**Adviser Professor(s)**
Prof. Wilhelmus Van Noije

**Students involved (names and aimed degrees)**
1 - Fellipe Sola - Master Student
2 - Roberto Rangel da Silva - Master Student
3 - Hugo Daniel Hernandez - Pos-doc
4 - Lucas Severo – PhD

**Institution (University/Faculty):**
Polytechnic School of the University of São Paulo - Electrical Engineering

**Type of Circuit Design: ( ) Digital; (X) mixed signal; (X) analog; (X) RF**

**Date of the circuit tape-out of the run:** 16/05/2017
**Date of receiving the chips at your institution:** 12/09/2017

**Short description of the circuit: (function, proposed innovation, number of transistors, passive components, screen shot of the chip layout, etc.)**
**Main results and representative performance data or curves, picture of the IC, does circuit function as expected, etc.**

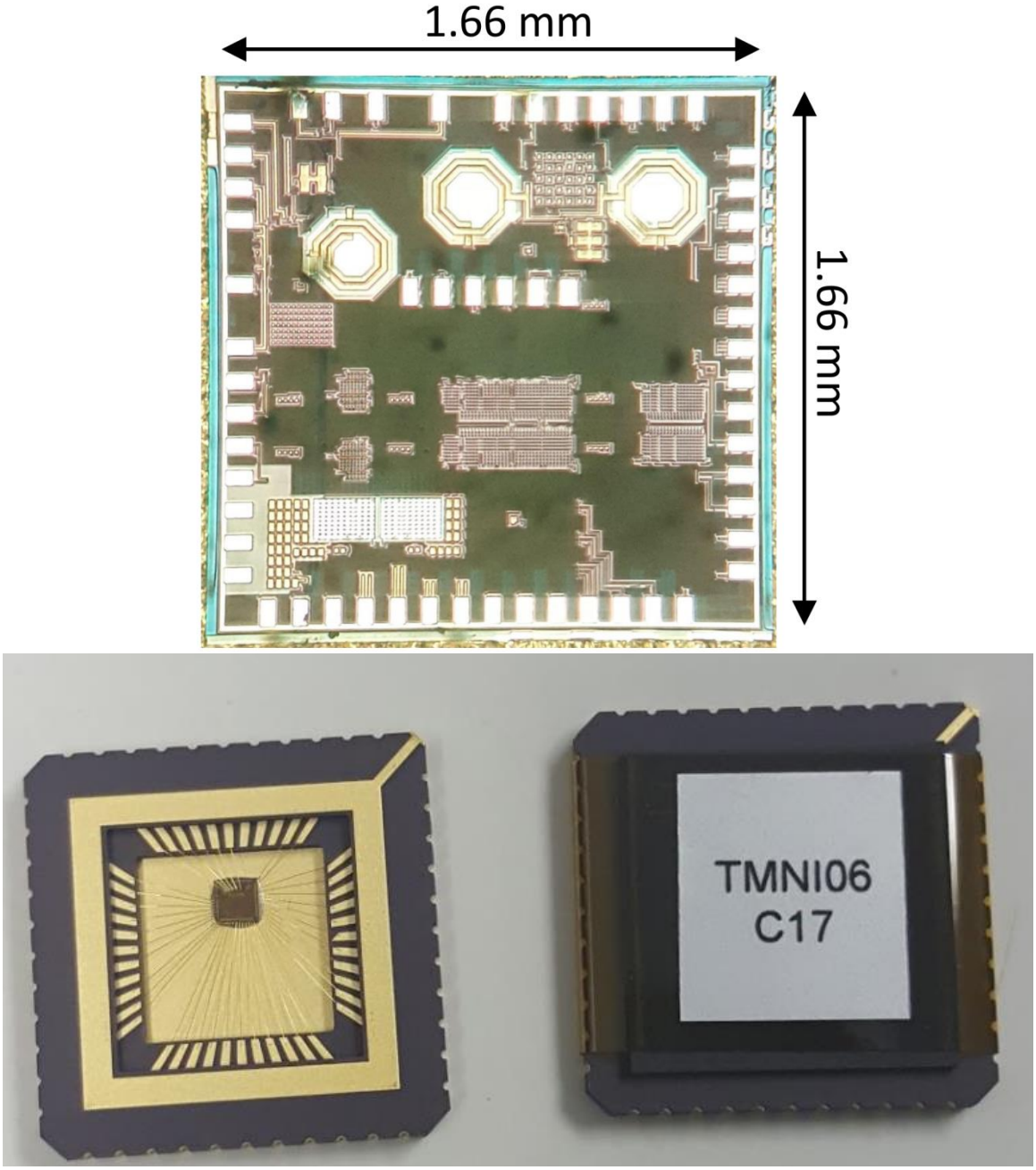


*Figure 1. Microphotograph of the manufactured chip*

### *A. 0.5V 2.4HGZ V Voltage Controlled Oscillator (VCO)*

This circuit is a voltage controlled oscillator based on the cross-coupled topology. The circuit uses two inductors, a bank of capacitors, two MOS-capacitor acting as varactors to tuning the oscillation frequency. Also it has 7 switches to control the current and capacitance of the bank to compensate PVT variations. The proposed innovation has been the circuit design for low power

applications, consuming using power supply voltage (VDD) of only 0.5V (a reduction of 72%) and bulk bias. The power consumption of the VCO is 2mW, and figures 2 and 3 present the transient response and the spectrum of the output signal, respectively. From these figures we can note that the center frequency is 2.45GHz.

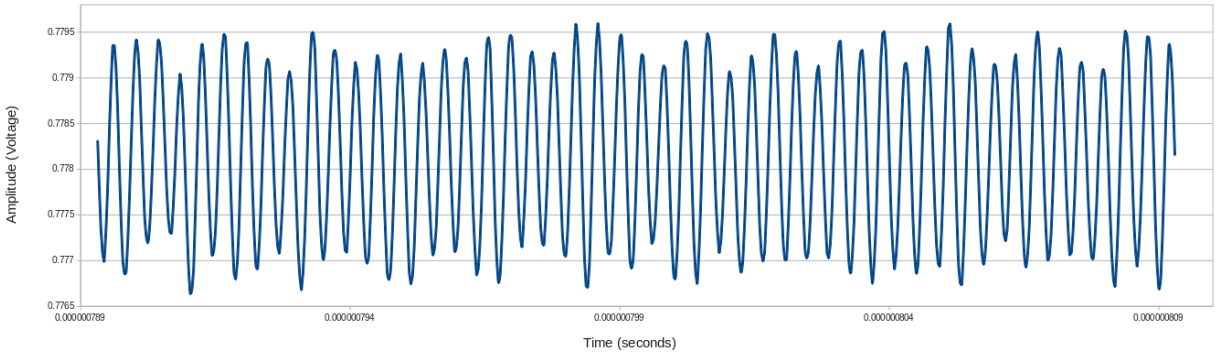


Figure 2. VCO output signal.

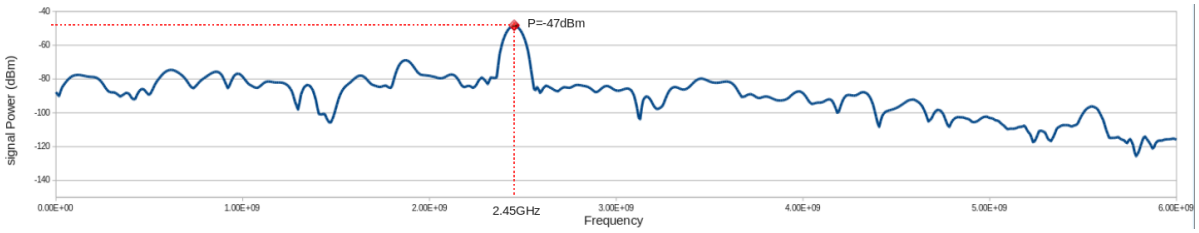


Figure 3. *Spectrum of the VCO output signal.*

### *B. Ultra-Low Voltage RF LNA for a Bluetooth Low-Energy Receiver*

Figure 4 presents the LNA schematics. The circuit uses a cascode topology, including forward bulk biasing for threshold voltage reduction, enabling the operation at 0.5V voltage levels using the present 180nm technology, whose original nominal supply voltage is 1.8V. Moreover, a varactor was added to the load to further calibrate the LNA output matching. The circuit is designed to operate at Bluetooth's frequency range, 2400 – 2483.5 MHz.

Figure 5 shows the test board designed for a Chip-on-board connection of the chip die, an additional off-chip matching network was included to fix PCB line impedance.

The input response has been tested through *S11* measurement using a Vector Network Analyzer (VNA) as shown in Figure 6. Measurements for the other performance factors are still been carried out.

The input reflection ratio (S11) shows a -9dB response inside the frequency band of interest. The static current consumption is 1.3 mA at 0.5V supply and 0.4V input bias, presenting 0.65mW power consumption.

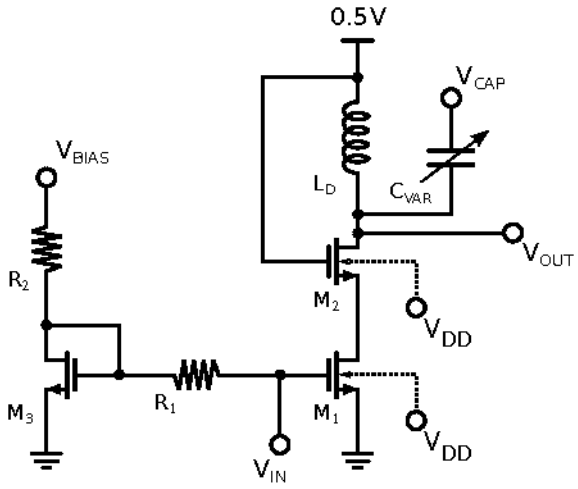


*Figure 4. LNA Schematic Capture*

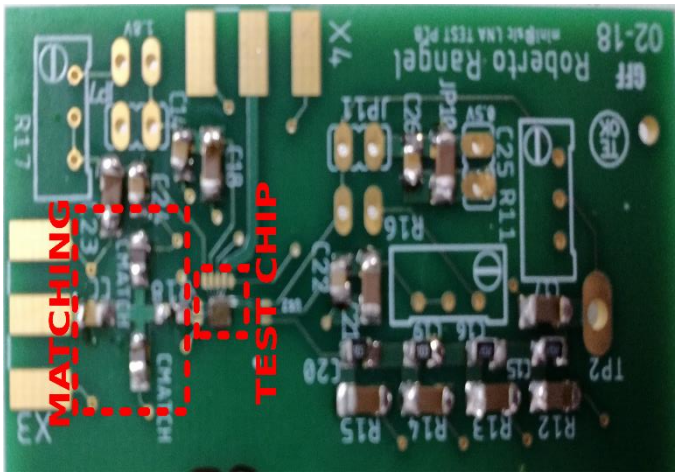


*Figure 5. VCO and LNAtestboard.*

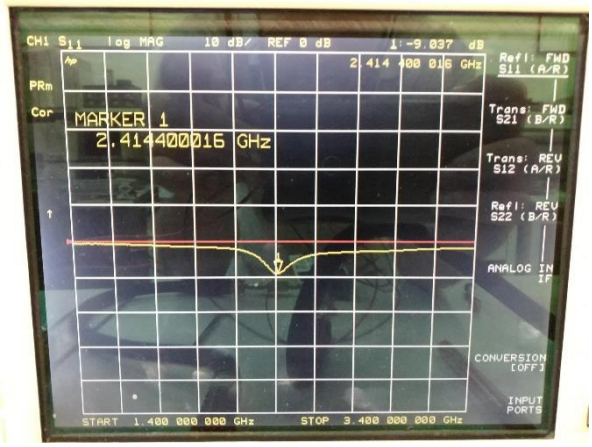


*Figure 6. S11 measurement result*

### *C. 0.5V 9bits 10MS/s SAR ADC*

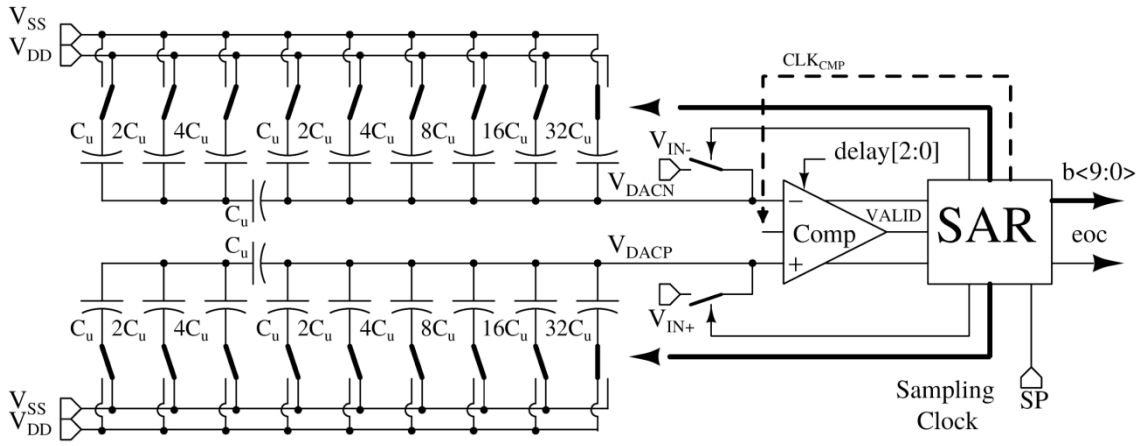


*Figure 7: Schematic of the 0.5V SAR ADC.*

A 9-bit 10MS/s asynchronous SAR ADC at 0.5V of supply voltage for BLE applications in 180nm CMOS technology was designed and experimentally validated in this work. The proposed comparator and bootstrapped circuits topologies demonstrated to be adequate for design with low-$V_t$ transistor and ultra-low voltage operations. The experimental results indicated that the manufactured chip consumes 48uW in normal operation at 10MS/s, with ENOB of 8.55 bits for 1MHz of input frequency. The measured peak of INL and DNL using code-density were 0.7/-0.85 LSB and 0.9/-0.5 LSB, respectively, as shown in Figure 8.

Figure 7 shows the block diagram of the designed ADC. It comprises a low-power dynamic latch comparator, a 9 bits' capacitive split-array DAC (6 MSB and 3 LSB), an asynchronous SAR digital logic and two bootstrapped switches. A differential architecture was used to have a good common mode noise rejection.

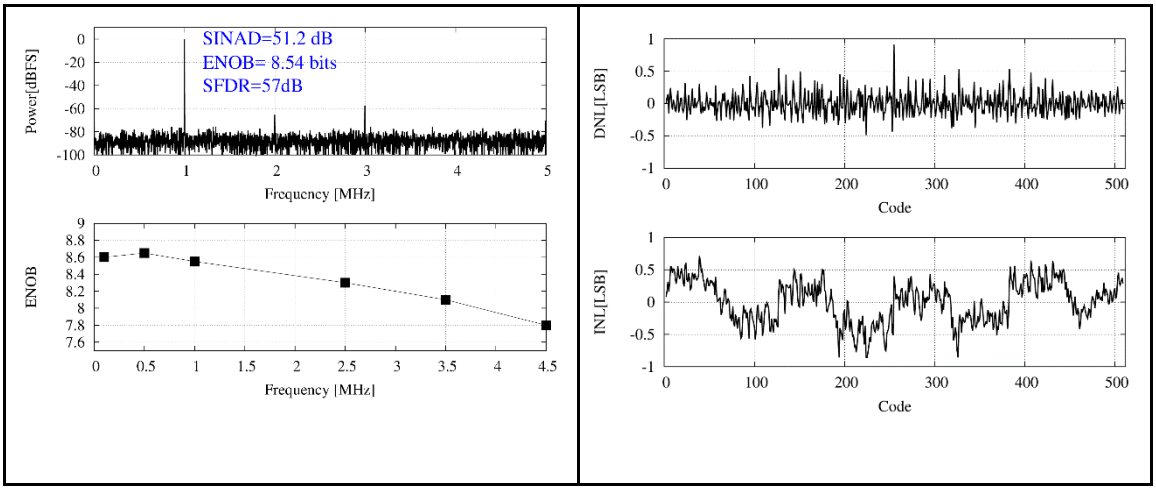


*Figure 8. Experimental results of the 0.5V SAR ADC.*

The ADC has two operation phases: (1) sampling phase, where the input differential signal is stored on the top plates of the capacitor array, and (2) decision phase, where the successive approximation algorithm is performed from MSB to LSB bits solution. The decision phase takes place after the falling edge of the sampling clock and the ADC takes 9 clock cycles to find the digital output word. After this time period, the ADC remains in the sampling-hold phase

until the next falling edges of the sampling clock. The end-of-conversion signal will be enabled (high) when the output data is ready and disabled (low) by the rising edge of the sampling clock.

The maximum sampling frequency of the ADC is 10 MS/s. During the sampling phase, the differential inputs are connected to the top-plates of the capacitor array and, simultaneously, the MSB is set to high and all other bits are reset to low. Next, the sampling switch is open and the input data is sampled on the capacitor array, then the comparator performs the first comparison with the positive edge of the CLK_CMP signal. If VDACP is higher than VDACN, the MSB stays high, otherwise it goes low. The decided bit is stored in the SAR register with the positive edge of the VALID signal.

### *D. Ultra-low voltage (ULV) and ultra-low power (ULP) active-RC Complex Bandpass Filter (CxBPF) and Programmable Gain Amplifier (PGA) for Bluetooth low energy receivers.*

Figure 9 shows the schematic of the proposed circuits. To reach the ULP operation we have used single-stage operational amplifier instead of using multiple stages to save the power waste in phase margin compensation. To compensate for the opamp reduced voltage gain and resistive loading we have proposed a novel strategy of using an input connected negative transconductor. The circuits were implemented using only two Low-VT stacked transistor and PMOS bulk forward bias to be able to operate with a power supply voltage down to 0.36V. The experimental results showed that both CxBPF and PGA present specification in according to the requirements of the Bluetooth Low Energy 5 standard. The CxBPF presented a power dissipation of only 10.9 uW/pole, 1 MHz bandwidth centered at 2 MHz, image rejection rate of 34 dB and 12.7 fJFoM. The measured performance showed comparable specifications, the best FoM and the smallest power dissipation among the works with measured results of CxBPF for BLE receivers presented in the literature. The PGA measured results at 0.36V showed a programmable voltage gain from 0.2 to 18.4 dB, 15.4 µW power dissipation and 0.98 MHz bandwidth.

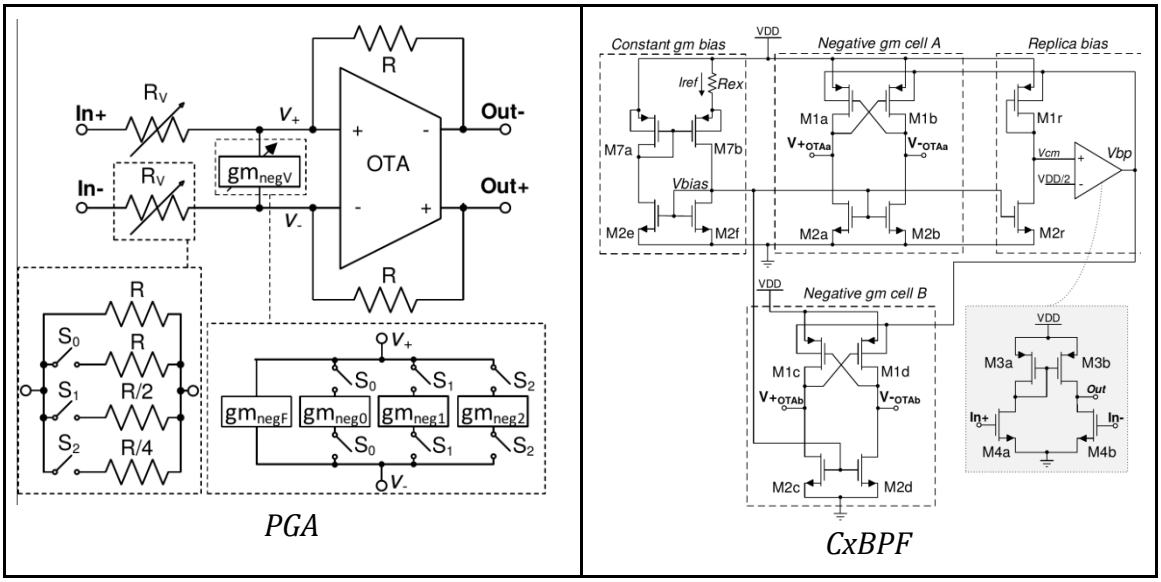


*Figure 9.* schematic of the proposed circuits

**Resulting publications (submitted, accepted or published) and degrees earned by students.**

1. SEVERO, L.; VAN NOIJE, W.: 0.36V PGA combining single-stage OTA and input negative transconductor for low energy RF receivers. ELECTRONICS LETTERS, v. 54, p. 319-320, 2018.

2. SEVERO, L. C.; NOIJE, W. A. M. V.: A 10.9uW/pole 0.4-V Active-RC Complex BPF for Bluetooth Low Energy RF Receivers. 9th IEEE Latin American Symposium on Circuit and Systems, 2018, Puerto Vallarta - Mexico;

3. HUGO HERNANDEZ; SEVERO, L.; VAN NOIJE, W.: 0.5V 10MS/s 9-bits asynchronous SAR ADC for BLE Receivers in 180nm CMOS technology. 31st international IEEE SoC (System-on-Chip) Conference (*SOCC 2018*).

4. SEVERO, L. C.; NOIJE, W. A. M. V.: the paper presented at 9th IEEE Latin American Symposium on Circuit and Systems, 2018, was considered as one of the best papers and the authors were invited to submit an extended paper to IEEE TCAS-1, which was sent out in June 2018.