IMEC FreeMini@sic Fabrication on TSMC 0.18 um Technology

Title of the Circuit: ***Chip_ITA_2017***

I. *Analog-to-Digital Converter (ADC), Level Crossing, resolution 5 bits*
II. *High dynamic range ROIC cell*
III. *High reliability finite-state machine*
IV. RadHard ROIC Unit Cell

Adviser Professor(s): *Prof. Dr. Lester de Abreu Faria*

Students involved (names and aimed degrees): *i. Gabriel Antonio Fanelli de Souza (Doctorade's degree),* ii. *Rodrigo Bispo dos Santos (Doctorade's degree);* iii. *Brunno Brendon Cortes de Oliveira (Master's degree);* iv. *Lucas M. Santana (Undergraduation's and Master's degrees);* v. *Nicholas Yukio Menezes Sugimoto (Undergraduation's and Master's degrees); vi. Fernando Ribeiro dos Santos (Undergraduation's and Master's degrees).*

Institution (University/Faculty): *Instituto Tecnológico de Aeronáutica - ITA*

Type of Circuit Design: ( ) Digital; ( ) mixed signal; (X) analog; ( ) RF

Date of the circuit tape-out of the run: *Aug, 29th, 2017*
Date of receiving the chips at your institution: *Jan, 22nd,2018*
Date of the report and/or of later update: *Aug, 16th, 2018*

Short description of the circuit: (function, proposed innovation, number of transistors, passive components, screen shot of the chip layout, etc.)

In this IC we have basically 4 circuits. Below one can find a short description of each one of them.

The first one is an Analog to Digital Converter (Fig.1) working in the level crossing topology that aims to take advantage of the sparse signals behavior of biomedical signals to decrease the power consumption. The main innovation behind this new circuit is that the slack time during the update of the DACs' moving window is being used to save power by the means of turning OFF the comparators which are the most power hungry parts of the circuit. This is controlled internally by an Asynchronous Finite State Machine and can be calibrated externally through a 2-phase handshake protocol.

The second one is a novel ROIC (Readout Integrated Circuit) cell with high dynamic range in terms of the photocurrent magnitude it is able to readout, which was achieved by means of a mixed (analogue and digital) circuit approach. The entire cell comprises 97 MOS transistors and one capacitor and its layout dimensions are 125.3 x 65.9 um. Figure 2 shows a block diagram of the circuit. It is based on a DI (Direct Injection) ROIC cell, which performs the readout task through integration of the input photocurrent in a capacitor. The other blocks shown in the diagram successively discharge the DI capacitor at the end of every charge so the capacitor can be charged again and the number of complete charges is routinely incremented in the counter.

The third one is a High reliability finite-state machine. The circuit is a combination of three Synchronous Finite-State Machines, which was designed with a different redundancy technique. The first is a simple machine, with no extra hardware. The second is designed with the TMR (Triple Modular Redundancy) technique. The last one is designed with a novel technique, which combines transistor duplication and logic redundancy for a better redundancy. The three machines are identical in functionality and differ only by the logic gate topology. The same inputs (2 variables and a clock) goes to each of them, and the outputs are separated.

The fourth one is a RadHard ROIC Unit Cell. It focus on the creation of a Radiation- Hardening (Rad-Hard) Unit Cell (Input Module) where, through the use of layout techniques (guard rings; P-MOSFETxN-MOSFET; channel-size variations; common-centroid layout; etc.), it is expected to achieve RadHard elements for ROICs.

Main results and representative performance data or curves, picture of the IC, does circuit function as expected, etc.

1 - For the Analog to Digital Converter, the main results are:

Measures: Power ON = 8uW, Power OFF = 0.2uW. Estimated average power (depends on what you are communicating with DAC): Gated Flip Flop: 5.66uW to 7.9uW depending on input frequency (sine wave) - 29% to 1.2%. DSP: ~ 3.3uW using first derivative estimation (sine wave) - 58%. DSP: ~ 1.76uW using first derivative estimation (triangular wave) - 78%. And Area: 0.04mm2 being 53%, by the 2 DACs

2 - For the high dynamic range ROIC Cell

An integrated voltage versus input photocurrent analysis was performed experimentally (Fig.3). In this analysis, each point corresponds to an input photocurrent and the integration time was 17.6 ms for all values of photocurrent. The plot presents the extended integrated voltage. The presented plot shows a highly linear readout output (extended integrated voltage) versus input (photocurrent) characteristic, which asserts the functionality of the designed circuit for conditioning current signals.

3 – For the high reliability finite –state machine

Results can be seen below, which are only simulated to this time.

Atraso	TMR	Complex
NAND	6,54	4,31
NOR	6,22	3,88
NOT	9,60	2,53
AND	—	5,88
OR	—	4,63

Potência	TMR	Complex
NAND	8,28	5,43
NOR	7,60	3,59
NOT	5,67	2,17
AND	—	4,45
OR	—	4,30

Área	TMR	Complex
NAND	9,8	4,0
NOR	9,8	4,0
NOT	13	1,6
AND	—	4,0
OR	—	4,0

4 – For the RadHard ROIC Unit Cell

Preliminary results were measured under normal conditions, where the performance of the circuit worked well. Results can be seen below. Now we are starting the radiation phase, where the IC is being radiating with Co60 in order to check its performance when compared to the ones that do not present the RadHard techniques.

5 – For the previous IC from IMEC Free Mini@sic 2016

Results are still being collected and are a source for our published papers in 2017. They serve as a basis for two PHD Students (Rodrigo and Gabriel), who will propose additional layouts in 2018, as a matter of upgrading actual results.

Main challenges and difficulties encountered during design, submission, import process and measurements of the circuit.

The main challenge encountered during this period was due to the import process. Although the IMEC did not charge anything, the Brazilian Government charged high import taxes, which hampered the process, as the students and the advisor had to pay with their own money.

Besides, we found some kind of lack of repeatability in the measurements, leading to a certain difference between ICs

Resulting publications (submitted, accepted or published) and degrees earned by students.

Journals:

1. *SOUZA, GABRIEL A.F. ; SANTOS, RODRIGO B. ; ROCHA RIZOL, PALOMA M.S. ; OLIVEIRA, DUARTE L. ; FARIA, LESTER A.. A novel fully-programmable analog fuzzifier architecture for interval type-2 fuzzy controllers using current steering mirrors. JOURNAL OF INTELLIGENT & FUZZY SYSTEMS, v. 34, p. 203-212, 2018.*
2. *FANELLI DE SOUZA, GABRIEL ANTONIO ; DOS SANTOS, RODRIGO BISPO ; DE FARIA, LESTER ABREU . Low-Power Current-Mode Interval Type-2 Fuzzy Inference Engine Circuit. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS JCR, v. 1, p. 1-12, 2019.*
3. *FANELLI DE SOUZA, GABRIEL ANTONIO ; DOS SANTOS, RODRIGO BISPO ; DE FARIA, LESTER ABREU . Low Power Membership Function Generator for Interval Type-2 Fuzzy System . Journal of Inteligen fuzzy systems, 2019.*

Symposiums:

4. *Yukio, N. ; FARIA, L. A.. CMOS Inverter Based Voltage Level Sensor. In: Simpósio de Aplicações Operacionais em Áreas de Defesa (SIGE), 2018, Sao José dos Campos. Anais do Simpósio de Aplicações Operacionais em Áreas de Defesa (SIGE), 2018.*
5. *SOUZA, GABRIEL A.F. ; FARIA, L. A.. Circuito CMOS de Máximo e Mínimo em Modo Corrente para Aplicações Fuzzy. In: Simpósio de Aplicações Operacionais em Áreas de Defesa (SIGE), 2018, Sao José dos Campos. Anais do Simpósio de Aplicações Operacionais em Áreas de Defesa (SIGE), 2018.*

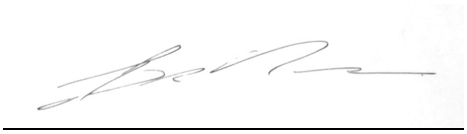
I. ***Rodrigo Bispo dos Santos*** *has already earned his Master's degree, in February, 2018; and has already started his PHD degree, in July, 2018.*
II. ***Gabriel Antonio Fanelli de Souza*** *is already pursuing his Doctorade's degree.*
III. ***Gabriel Antonio Fanelli de Souza*** *has already overcome the qualifying level forhis PHD Degree.*
IV. ***Brunno Brendon Cortes de Oliveira*** *is already pursuing his Master's degree.*
V. ***Lucas M. Santana*** *has already earned his UnderGraduation's degree, in December, 2017; and has already started his Master's degree, in January, 2018.*

VI. ***Lucas M. Santana*** *has already earned his Master's degree, in March, 2019.*

VII. ***Nicholas Yukio Menezes Sugimoto*** *has already earned his UnderGraduation's degree, in December, 2017; and has already started his Master's degree, in January, 2018.*

VIII. ***Fernando Ribeiro dos Santos*** *has already earned his UnderGraduation's degree, in December, 2017; and has already started his Master's degree, in January, 2018.*

IX. ***Tassio Cortes Cavalcante*** *has already earned his Master's degree, in November, 2018.*



Lester de Abreu Faria - Prof. Dr.
Advisor

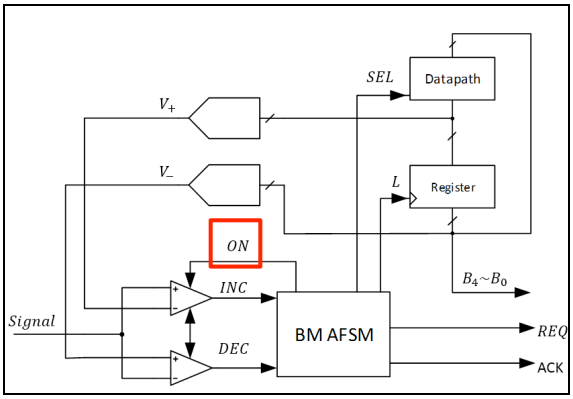


Fig 1

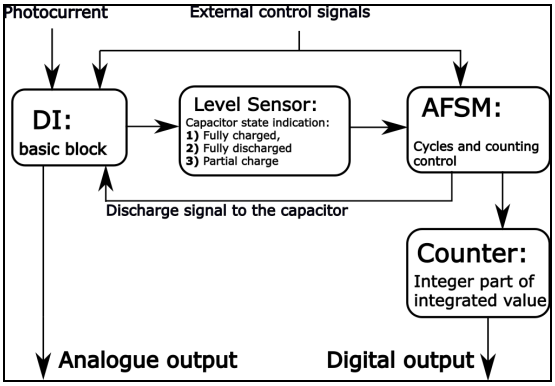


Fig 2

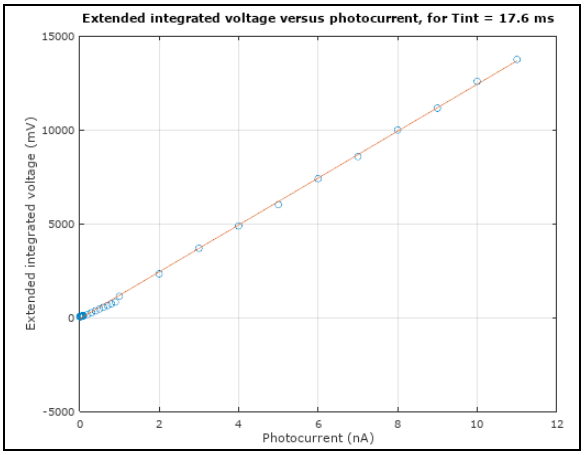


Fig 3

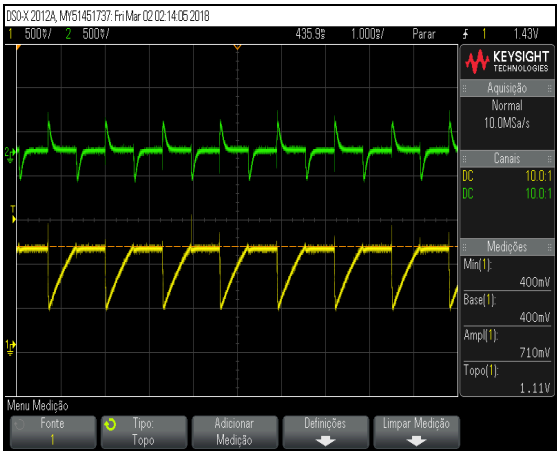


Fig 4