IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology

Title of the Circuit
RadHard digital library cells

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Type of Circuit Design: ( ) Digital; (x) mixed signal; ( ) analog; ( ) RF

Date of the circuit tape-out of the run: 2017/Mar
Date of receiving the chips at your institution: 2017/Sep
Date of the report and/or of later update: 2018/Aug/16

Short description of the circuit: (function, proposed innovation, number of transistors, passive components, screen shot of the chip layout, etc.)

In the context of design flow automation, necessary to synthesize complex digital circuits, there is a lack of reliable foundry-provided Radiation Hardening by Design (RHBD) cell libraries.

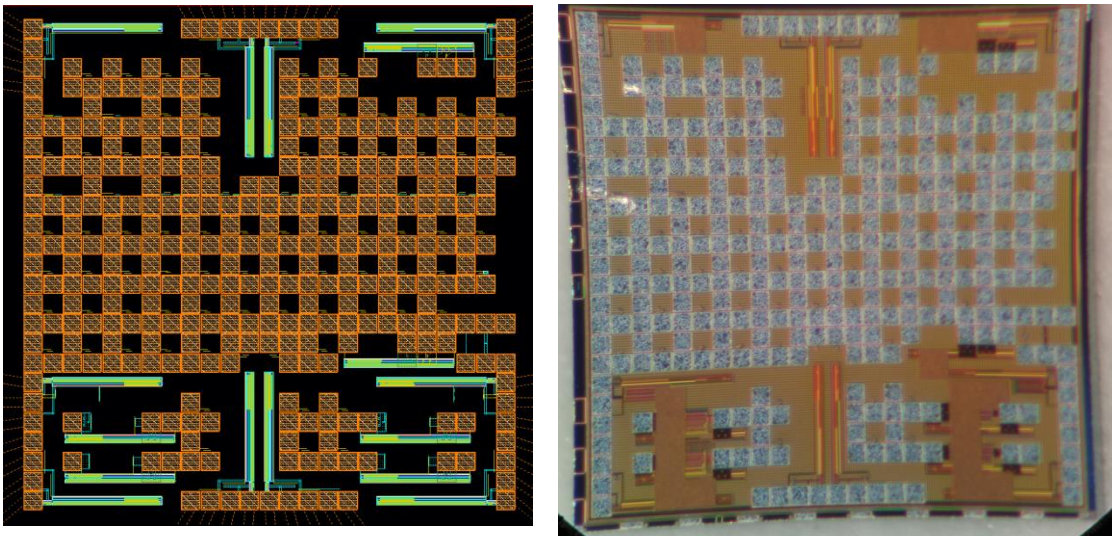
Thus, this PhD work entitled as *Design flow methodology for Radiation-Hardening by Design CMOS Enclosed-Layout-Transistor-based standard-cell library for aerospace applications aims to provide radiation-tolerant ICs, accounting for real-world constraints*. The focus of ASIC proposal it is to serve as practical measurements to validate the PhD proposed design flow.

This way, there is a group of cells, selected to characterize the basic building blocks of the RHBD library cells for TSMC 0.18um.

a) Individual enclosed transistors (n,pELT)
b) Individual standard transistors (n,pSTD)
c) n,pELT in series
d) n,pELT in parallel
e) Inverter-based Ring Oscillators
f) Output Buffers

The design and final test chip are shown in Figure 1 (a) and (b), respectively.

Figure 1: Test chip.

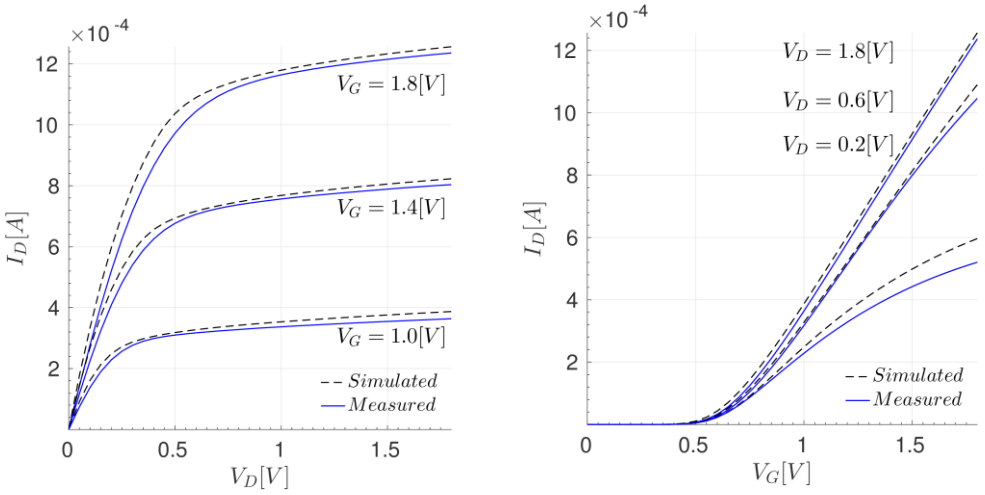


a) Designed test chip top view. (b) Laid-out test chip top view.

Main results and representative performance data or curves, picture of the IC, does circuit function as expected, etc.

Figure 2 shows a comparison of the output characteristic and transfer function between simulated versus measured values for a minimum nELT designed in 180nm. In these behaviors, the parametric voltages are VGS=1.8, 1.4, and 1.0; and VDS=1.8, 0.6, and 0.2, respectively.

Figure 2: Output characteristic and transfer function for nELT.



(a) ID x VD (b) ID x VG

Despite the use of the enclosed geometry, the SPICE simulated individual devices with different aspect ratios and lengths displayed good agreement to the measured data, as shown, for instance, in Fig. 2 (less than 5%). This is an important aspect for methodology validation; there was no need to fully characterize and model the ELTs in order to obtain adequate simulations. Simulation results were obtained using conventional commercial PDKs and CAD tools.

A complete characterization and device's parameter extraction are still being executed, nonetheless, these preliminary practical results shown that the methodology is fully compatible with the standard digital design flow and can be automatized into the flow to reduce costs. The methodology was validated through a comparison between SPICE simulation and electrical characterization of the proposed test structures fabricated in two different technology nodes.

Main challenges and difficulties encountered during design, submission, import process and measurements of the circuit.

During the entire phases of design (layout) and import phase, we have not had any difficulty and would like to thank the excellent support of both Prof. Jacobus W. Swart and Mr. Tobias Vanderhenst from IMEC.

Our research group would like to thank them for all support and attention during all processes steps.

Resulting publications (submitted, accepted or published) and degrees earned by students.

Today I am working on the final device's measurements and parameters extraction to qualify the accuracy of proposed methodology.

Submited work: Vaz, Pablo; Both Thiago; Vidor, Fabio; and wirth Gilson. "Design flow methodology for Radiation Hardened by Design CMOS enclosed-layout-transistor-based standard-cell library" Journal of Electronic Testing.