IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology

Title of the Circuit: Low Voltage Analog Circuits: A Low-Voltage Sigma-Delta Modulator with Inverter-Based OTAs, Inverter-Based OTA and Low-Pass Filter.

Adviser Professor(s): Alessandro G. Girardi, Lucas C. Severo and Paulo César C. de Aguirre.

Students involved (names and aimed degrees): Lucas C. Severo (Ph.D student at USP) and Paulo César C. de Aguirre (Ph.D student at UFRGS)

Institution (University/Faculty): Universidade Federal do Pampa (UNIPAMPA/Campus Tecnológico de Alegrete)

Type of Circuit Design: ( ) Digital; ( ) mixed signal; (X) analog; ( ) RF

Date of the circuit tape-out of the run: 12 September 2018, run 6375.
Date of receiving the chips at your institution: January 9th, 2019.
Date of the report and/or of later up-date: 05/08/2019 (later report)

Short Description of the circuit: (function, proposed innovation, number of transistors, passive components, screen-shot of the chip layout, etc)

The proposed chip was limited by the number of pins. Three circuits were fabricated. The low-voltage sigma-delta modulator with inverter-based operational transconductance amplifiers (OTAs) was measured and the results are shown hereafter. The low-voltage OTA was not measured yet since a short-circuit in the power rails was verified. The short-circuit was opened by an FIB provided by ST Microelectronics and the OTA will be measured in September 2019 (all 3 PCBs to test this OTA are ready). The low-voltage filter PCB is being finished and the circuit is expected to be measured at the beginning of September 2019.

The fabricated low-voltage continuous-time sigma-delta modulator (CT-SDM) main novelty is the loop-filter amplifier topology. This amplifier is a single-stage inverter-based OTA robust to process, voltage, and temperature (PVT) variations. The OTA topology biasing is provided by a bulk-based current mirror that significantly reduces the unity gain-bandwidth variation across PVT corners. Also, the proposed OTA presents a very stable DC gain around 40 dB. The amplifier has 32 transistors, 2 on-chip resistors, 2 off-chip resistors, and 4 on-chip capacitors. The amplifier topology was published in the IET Electronics Letters. This amplifier was used to design a low-voltage CT-SDM with the loop-filter amplifiers working in weak inversion. The proposed modulator also used a passive RC path to assist the amplifier of the first integrator to increase power efficiency. Also, a digitally tunable capacitive bank was used to

compensate RC variations. The proposed modulator was fabricated in the TSMC 180-nm CMOS process with a silicon area of 0.36 mm2. Figure 1 depicts the CT-SDM layout.

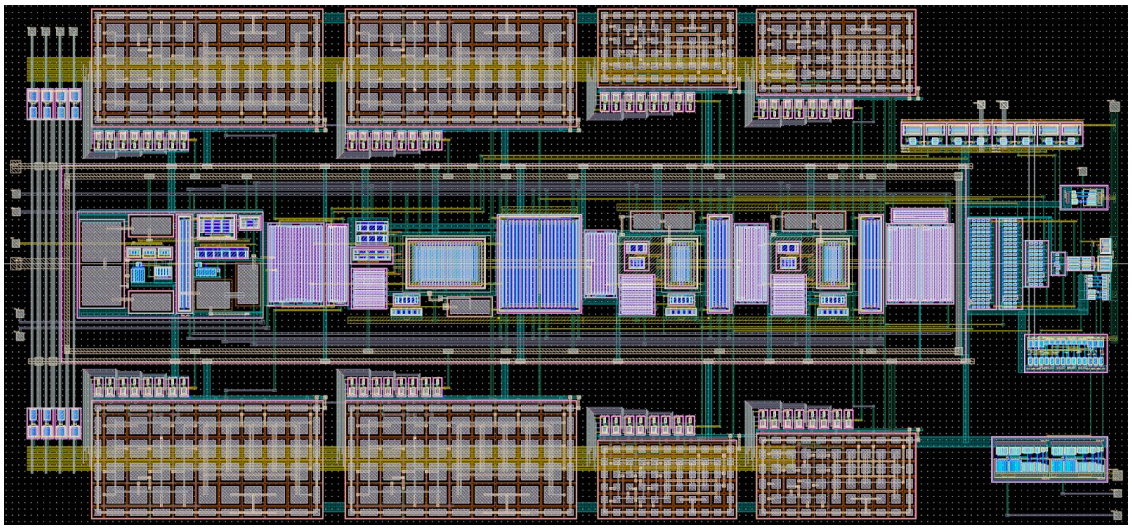

Figure 1 - Layout of the proposed CT-SDM. A full layout symmetry is observed.

Main results and representative performance data or curves, picture of the IC, does circuit function as expected, etc

The chip microphotograph, with the CT-SDM area highlighted, is shown in Figure 2. The modulator loop filter operates with an analog supply voltage of 0.45 V while the digital circuit operates at 0.6 V. The modulator total power consumption is 28.72 µW. For a 50-kHz signal bandwidth, the measured peak signal-to-noise ratio (SNR) is 71.24 and the signal-to-noise-and-distortion ratio (SNDR) is 70.64 dB. The achieved dynamic range (DR) is 78.3 dB, leading to a Schreier state-of-the-art figure of merit of 170.70 dB. Figure 3 depicts the measured output power spectrum density (PSD) for a 15-kHz 260-mV input signal. Figure 3 shows the modulator SNR/SNDR as a function of a 15-kHz input signal amplitude.

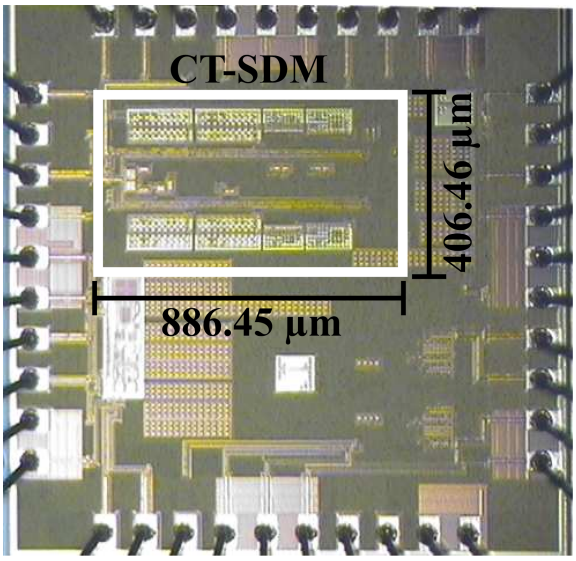

Figure 2 - Chip microphotograph.

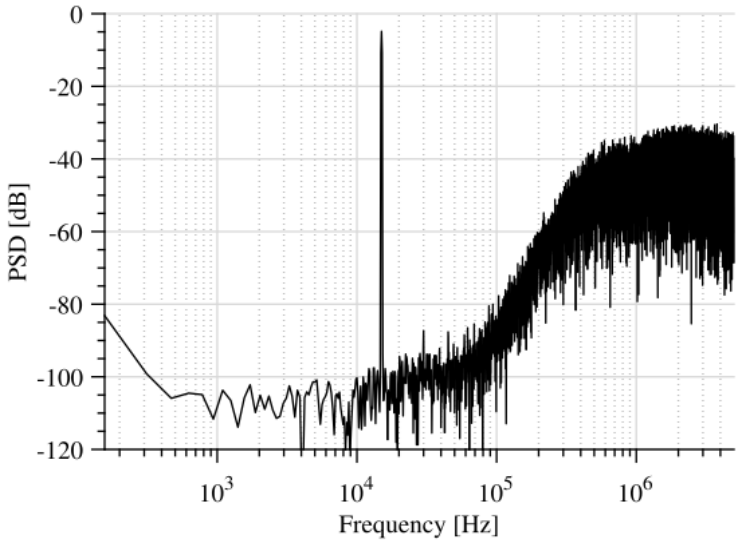

Figure 3 - Measured output power spectrum density (PSD) for a 15-kHz 260-mV input signal.

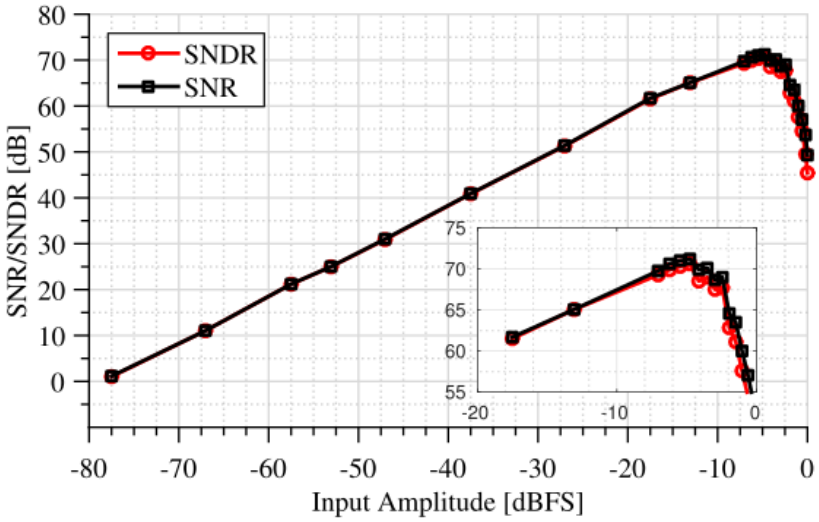

Figure 4 - SNR/SNDR as a function of the 15-kHz input signal amplitude.

Main challenges and difficulties encountered during design, submission, import process and measurements of the circuit.

The main challenge was the top-level circuit layout. We had fabricated an IC in the same technology in 2016 (also provided by the mini@sic program). However, we changed the IO-cells in this tape-out, and we had some IO-cells orientation problems. The IO-ring is designed using abstract cells only, without the layout view. It is not straightforward to handle since we do a top-level layout once a year in our Institution. In this run, we used an IO-cell with the open-cavity smaller than the standard one, and we paid and extra value. Our research group started the design and fabrication of analog and mixed-signal ICs in 2016. Thus, our design skills are growing after each tape-out.

The fabricated chip was measured during the stay of Prof. Paulo Aguirre at Pavia University (Pavia, Italy). It should be noted that our research group acquired more measurement equipment in 2019. Now, it is fully equipped to characterize low-power analog, mixed-signal, and RF chips. It was possible due to the increase in the number of high-quality publications, mainly originated by the access of IC fabrications as the one provided by the IMEC-mini@sic program.

Resulting publications (submitted, accepted or published) and degrees earned by students:

1) P. C. C. de Aguirre and A. A. Susin, “PVT compensated inverter-based OTA for low-voltage CT sigma-delta modulators,” Electronics Letters, vol. 54, no. 22, pp. 1264–1266, Nov. 2018.

2) A 170.7 dB FoM-DR 0.45/0.6-V Inverter-Based Continuous-Time Sigma-Delta Modulator" which was submitted to the IEEE Transactions on Circuits and Systems II: Express Briefs. Paper submitted and accepted with minor revisions (preparing revision).

3) Paulo César C. de Aguirre is finishing the thesis writing. The thesis presentation is expected to occur on October 2019.

Notes:

1) Publications should include acknowledgement to imec for the free fabrication on TSMC 180 nm technology.
2) The length of the report may be 2 to 3 pages.
3) The report is due at 6 months after receiving the chips (can be updated afterwards, with new publications and students completing degrees).
4) Any suggestion to improve the program can be sent separately to Jacobus Swart.