Impact of Gate Stack Layer Composition on Dynamic Threshold Voltage and Analog Parameters of Ge pMOSFETs

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ABSTRACT

One of the main challenging issues for germanium (Ge) devices is the gate stack engineering which determines the interface state density (N_{IT}) and the associated channel/oxide interface quality. This paper shows how this issue can play a role in p-channel Ge MOSFETs considering both the operation mode, i.e., comparing conventional, dynamic threshold voltage (DT, where $V_{BS} = V_{GS}$) and enhanced dynamic threshold voltage (eDT, where $V_{BS}=k*V_{GS}$) modes, and the main analog parameters like the Early voltage (V_{EA}) and intrinsic voltage gain (A_V). Moreover, the impact of different HfO_2/Al_2O_3 gate stack thicknesses is under evaluation. Although the thinnest Al_2O_3 layer degrades all evaluated parameters, specifically: lower V_{EA} and A_V, higher drain current hysteresis and subthreshold swing (SS) due to the higher N_{IT}, the dynamic threshold voltage showed to be an effective mode to strongly minimize the hysteresis effects and improves up to 60% in eDT (k = 2) mode compared to the conventional mode (k = 0), thanks to the dynamic threshold voltage reduction.

Index Terms: *Ge pMOSFET; Dynamic threshold voltage control; I-V Hysteresis; Gate stack layer; Intrinsic voltage gain.*

I. INTRODUCTION

Many efforts have been given to develop materials beyond silicon (Si) mainly for future high-performance and photonic applications. Considering high-performance, the prime characteristic of an alternative channel material compared to Si must be the carrier mobility. Promising candidates for n-channel devices are III/V materials, which present electron mobilities many times the one for silicon, while for p-FETs germanium (Ge) is the first choice, since the Ge hole mobility is four times higher than for Si [1].

At the same time, some intrinsic material parameters of Ge are not so favorable. First of all, as a consequence of the lower bandgap (EG) compared to Si, the leakage current and the diffusion current in Ge p–n junctions are significantly higher [1], since the intrinsic carrier concentration (ni) at room temperature is three orders of magnitude higher than in Si [2]. Next, the Drain-Induced Barrier Lowering (DIBL) (and related short channel effects) seems to be more pronounced, since the Ge dielectric constant (ε_{Ge}) is higher than for Si [1].

All in all, an optimization is required in order to obtain the best performance of a Ge transistor. One of the main

challenging issues that must be taking into account is the gate stack engineering, including surface passivation. The latter plays an important role in the interface state density (N_{IT}), which typically for Ge is quite high, resulting in an off-state region degradation [3]. Aiming to obtain the lower N_{IT} level, different interfacial passivation layers have been studied and reported in literature, such as SiO_x/Si [4], GeO_2 [5], GeON [6] and Ge_3N_4 [7].

Apart from the material properties [8], [9], [10], different operation concepts can be applied in order to improve the device performance, such as the dynamic control of the threshold voltage (DTMOS), which was introduced by Colinge [11]. In this configuration, the body and gate of an SOI MOSFET are tied together ($V_{BS} = V_{GS}$), resulting in both improved on-state and off-state performance [11]. Most of studies in the literature concerning the dynamic threshold voltage ($V_{BS} = V_{GS}$) operation mode are related with both Partially Depleted (PD) [11], [12] and Fully Depleted (FD) Ultra Thin Body and Buried oxide

(UTBB) Silicon-On-Insulator (SOI) MOSFETs [13], [14]. On the other hand, few studies have considered the enhanced dynamic threshold voltage (eDT) mode, where the V_{BS} is equal to a k-factor times V_{GS} (V_{BS} = k*V_{GS}) [14]. As in [15] the DT concept mode has also been applied to bulk p-type Si MOSFET.

This work for p-channel Ge planar devices is split in two main parts. The first focuses on the impact of the operation modes, taking into account the conventional, dynamic and enhanced-dynamic threshold voltage modes, in other words: it analyses the k-factor of the eDT influence on the threshold voltage, subthreshold swing and I-V hysteresis. The second part focuses on the evaluation of the analog parameters, where the transconductance over drain current ratio (gm/I_{DS}), Early voltage (V_{EA}) and intrinsic voltage gain (A_V) are considered. Besides that, different gate stack layers are taken into consideration. In the first part, two different gate stacks are compared, while the second part evaluates four splits. The gate stacks are composed of germanium oxide (GeO_x), aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) as high-κ material, where both the Al_2O_3 and HfO_2 film thicknesses are varied.

The gate stack study on planar Ge pMOSFETs is of interest, since this knowledge can be useful for future Ge device integration, mainly in FinFET structures, where the combination of both advantages from vertical structures and higher hole mobility can be employed [16].

II. DEVICE PROCESSING AND CHARACTERIZATION

The p-channel germanium MOSFET devices under evaluation in this work have been fabricated on 300 mm Si (100) wafers via the replacement metal gate high-κ last process at imec/Belgium. The main process flow can be seen in Fig. 1. Further details can be found in [17].

- Si recess in STI
- Ge epitaxial growth
- N-well formation and anneal
- Dummy gate definition
- Gate etching
- Boron implantation (extension)
- Spacer formation
- SiGe layer grown
- ILD0 (field oxide) formation + CMP
- Dummy gate removal and high-k/MG/W fill + CMP
- Sintering

Figure 1. Process flow description of the Ge pMOSFET studied in this work.

The gate deposition sequence is schematically presented in Fig. 2 and started right after the dummy gate removal and with the Ge surface passivated by an atomic layer deposition (ALD) of Al_2O_3 followed by plasma oxidation and either the HfO_2 or Al_2O_3 deposition by ALD. Table I presents the dielectric composition and thickness of the four different studied processes. Lastly, the process was concluded by the deposition of 4.5 nm TiN and 80 nm W on the contacts, followed by sintering for 20 min in H_2 at 400°C.

The planar device dimensions are a channel width (W) of 10 μm and a channel length (L) of 500 nm, 1 μm and 10 μm. The device structure is given in Fig. 3. The channel has a doping concentration of around 1×10^{17} cm^{-3}. Furthermore, four samples from the same wafer have been characterized electrically and all results presented are related to the mean value.

The work is based only on experimental data, which were obtained from measurements with the Agilent B1500A - Semiconductor Device Parameter

Table I. Gate dielectric composition

Evaluation Part	Plasma Power (W) for GeO_x	Al_2O_3 thickness (nm)	HfO_2 thickness (nm)
I and II		0.5	2
I and II	400	1	1
II		1	2
II	50	1 + 2	-

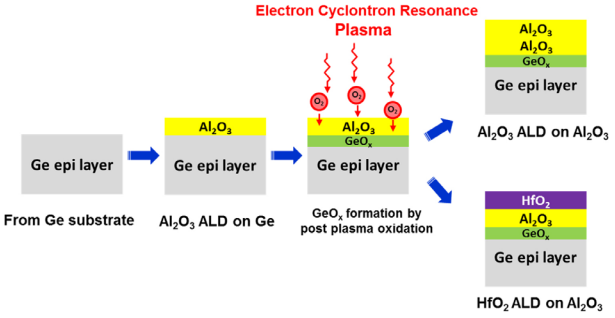

Figure 2. Basic schematic of gate stack fabrication.

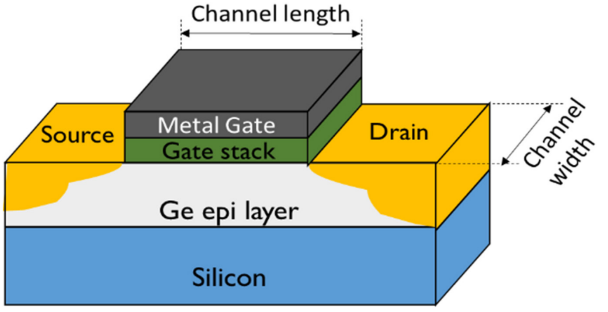

Figure 3. The Ge pMOSFET structure.

Analyzer. The hysteresis was extracted by measuring the drain current (I_{DS}) by a double sweep of the gate voltage (V_{GS}) at low drain-source voltage (V_{DS}) biasing (-50 mV) and a V_{GS} step of 10 mV. The magnitude of the hysteresis is the difference in the gate voltage between the forward and reverse curves measured at a constant drain current (2 μA) that is a reasonable value, allowing to observe and extract the hysteresis in all studied conditions, where the same trend as the maximum hysteresis values can be found. The threshold voltage has been extracted by the Ghibaudo method [18]. The latter presents the advantage of not being affected by the variations in carrier mobility owing to the transverse electric field [18]. Finally, the analog parameters were extracted from the same inversion condition, i.e., gate overdrive voltage (V_{GT}) of -0.25 V at V_{DS} of -0.8 V.

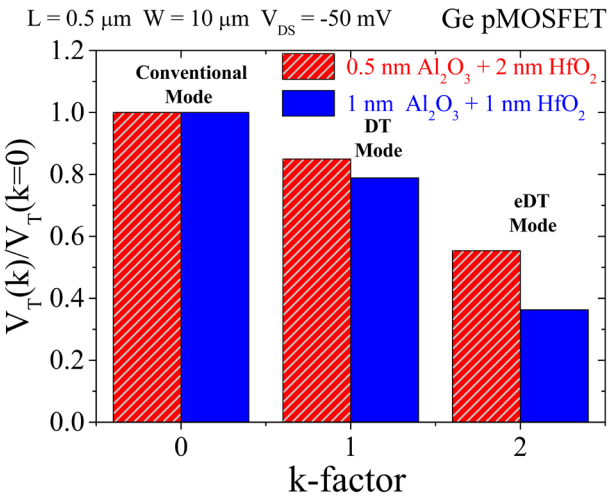

Figure 5. Threshold voltage as a function of k-factor, for two different gate dielectric compositions.

III. RESULTS AND ANALYSIS

Part I: Dynamic threshold voltage

Fig. 4 shows the drain current (I_{DS}) as a function of gate voltage (V_{GS}) for two Ge pMOSFETs with a different gate stack, consisting of 0.5 nm Al_2O_3 + 2 nm HfO_2 and 1 nm Al_2O_3 + 1 nm HfO_2, respectively, measured under different operation modes. First of all, one notices that for both devices the curves shift towards positive gate voltage (V_{GS}) as the operation mode is modified, i.e., for increasing k-factor. The latter plays a role in the threshold voltage (V_T) as discussed later on in Fig. 5. Second, comparing the performance of both devices in conventional operation (k=0), one notices that the device with the thicker Al_2O_3 presents a higher current level than the other one, thanks to the higher low-field carrier mobility and higher oxide capacitance density (C_{OX}) value. The latter is confirmed since the estimated Equivalent Oxide Thicknesses (EOT) are around 1.7 nm and 1.6 nm for the thinnest and the thickest Al_2O_3, respectively, resulting in a slightly lower C_{OX} value for the device with thinner Al_2O_3 layer. Third, as the forward substrate biasing increases, i.e., a k-factor different from zero, the depletion region decreases. In turn, the V_T dynamically reduces (on-state region) resulting in a higher I_{DS} level. On the other hand, when reverse substrate biasing is applied, the dynamic V_T presents the opposite behavior, resulting in an improvement of the subthreshold swing [14] as the k-factor increases (Fig. 6). Finally,

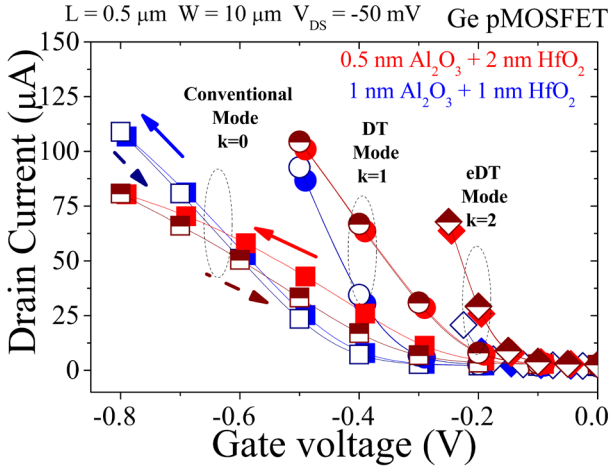

Figure 4. Drain current as a function of gate voltage for different k-factors and a gate dielectric composition of 0.5 nm Al_2O_3 + 2 nm HfO_2 and 1 nm Al_2O_3 + 1 nm HfO_2

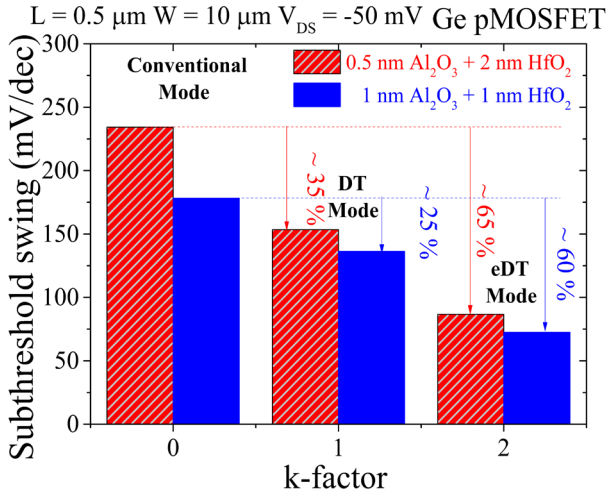

Figure 6. Subthreshold swing as a function of k-factor, for two different gate dielectric compositions

both devices present hysteresis for $|V_{GS}|$ above V_T, owing to the presence of border traps and further described in Fig. 7.

Fig. 5 depicts the normalized threshold voltage as a function of the k-factor. It shows that the V_T reduces towards a more positive value as the k-factor increases, owing to a reduction of the surface potential, when a forward substrate bias is applied. This effect is more pronounced as the k-factor increases.

The main difference in the normalized V_T between the two devices under investigation is related to the body effect coefficient, since the dynamic MOSFET V_T can be obtained from expression (1) [12]. One advantage of the small V_T in the on-state is that it leads to a large reduction in delay with respect to low voltage supply applications [15].

$$V_T = V_T(k=0) - \gamma\left(\sqrt{|-2\phi_F|} - \sqrt{|-2\phi_F| + V_{BS}}\right) \quad (1)$$

where V_T (k = 0) is the threshold voltage at zero substrate bias (conventional operation), γ is the body effect coefficient, $2\Phi_F$ is the surface potential at strong inversion and V_{BS} is the bulk-source voltage, which is k-factor times V_{GS} (k*V_{GS}). The negative sign of the body effect coefficient as in (1) is due to the forward biased bulk-source junction [12].

Fig. 6 clearly shows the effect of the k-factor on the subthreshold swing (SS). As the reverse substrate bias increases, the depletion region also increases, giving rise to a dynamic increase of V_T (off-state region), resulting in both leakage current and SS reduction.

As can be observed in Fig. 6 the SS improvement achieves around 60 % from conventional to eDT

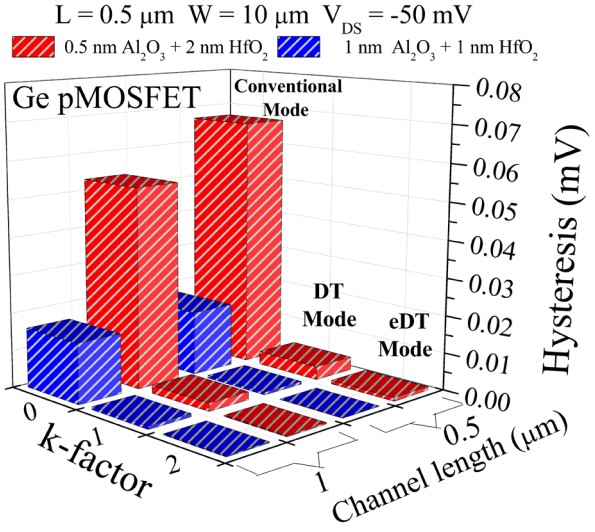

Figure 7. Hysteresis as a function of channel length and k-factor, for two different gate dielectric compositions.

modes for both devices. Also, it is worth to mention that worse SS values, for the thinnest Al_2O_3 device (k-factor equal to zero), is due to the higher interface trap density (N_{IT}) [19]. In addition, the SS improvement presented for both devices follows the same SS trend as observed in ultra thin body and buried oxide (UTBB) devices [14]. It confirms that the dynamic threshold technique can be applied not only for SOI but also for bulk planar devices**.**

Fig. 7 presents the hysteresis as a function of channel length (L) and k-factor, for two different gate dielectric compositions. At zero k-factor, there is a pronounce hysteresis dependence of Al_2O_3 layer thickness rather than the channel length dimension. On the other hand, a slight difference of the hysteresis for shorter devices might be associated to electrical characterization error, since the step value of the measured gate voltage was 10 mV, so that there is no significant hysteresis dependence of channel length. The latter is directly correlated to the channel/gate interface quality; one may have a strong impact of the interface charge density (N_{IT}) [19] and it is associated with the presence of border traps, i.e., hysteresis.

Similar as in [20] for Si devices, the hysteresis effect can be associated to border traps as a result of a V_{GS} sweep from weak to strong inversion, where interface states may capture holes from an inversion layer. Subsequently, the holes tunnel to the border traps. When the V_{GS} is backward swept, the holes tunnel back into the Ge channel [20]. As the border traps randomly communicate with the valence-band holes via the interface states [21], a higher interface state density results in higher hysteresis values.

The hysteresis for the thinnest HfO_2 layer presents almost no influence of the channel length, since it is the high-κ dielectric material, which plays a strong role in the effective oxide capacitance instead of the channel/gate interface quality. Furthermore, considering the contribution of the k-factor in the hysteresis in Fig. 7, one clearly observes that as the k-factor increases, the opposite behavior is found for the hysteresis. It indicates that the dynamic threshold voltage control is faster than the interaction between the interface and border traps, resulting clearly in a hysteresis drop. On top of that, the reduction of the transversal electric field at the surface under the DT and eDT modes also plays a role in suppressing the hysteresis, by reducing the tunneling probability.

Combining the I-V hysteresis behavior as a function of the k-factor and channel length in Fig. 7, one clearly observes that the thinnest Al_2O_3 layer presents a higher hysteresis compared with the other device, as long as the dynamic operation mode is not applied, i.e., both for DT and eDT. Otherwise, similar low hysteresis is obtained for both gate stacks with thin and thicker Al_2O_3.

Part II: Analog performance

Fig. 8 shows the gm over I_{DS} ratio as a function of the normalized drain current for four different gate stacks. One can notice that the lowest level in the strong inversion is achieved for the device with the thinnest Al_2O_3 layer. As discussed previously and in [19], this device presents a higher interface state density (N_{IT}), which degrades mainly the subthreshold swing, thereby compromising the low power/low voltage applications. On the other hand, the 1 nm Al_2O_3 splits show a similar behavior in weak inversion and some variation in strong inversion, where the dielectric on top of the first Al_2O_3 layer plays a more pronounced role.

The Al_2O_3 layer works as a protection layer for the channel (Ge)/oxide interface that controls the GeO_x layer growth during the oxygen plasma exposure [8]. This implies that the thinner the layer is, the more vulnerable to any damage during the fabrication processes it becomes. The latter is one of the challenging issues of the Ge MOSFET device, owing to the high level of interface trap density [1].

Fig. 9 depicts the Early voltage (V_{EA}) as a function of gate dielectric composition. As long as the Al_2O_3 layer thickness is 1 nm, there is no significant difference among the devices. On the other hand, like in Fig. 8 the thinnest Al_2O_3 layer also exhibits a more degraded parameter, which somehow facilitates the influence of the lateral electrical field in case of V_{EA} degradation.

Combining the gm/I_{DS} ratio and the Early voltage as shown in (2), one obtains the intrinsic voltage gain (A_V).

$$A_V = 20\log\left|\frac{gm}{g_D}\right| \approx 20\log\left|\frac{gm}{I_{DS}}V_{EA}\right| \quad (2)$$

Fig. 10 presents the intrinsic voltage gain (A_V) as a function of the gate stack. As a result of the degradation in both parameters (gm/I_{DS} and V_{EA}), the thinnest Al_2O_3 layer presents the lowest value of A_V. Apart from that, no significant A_V variation is observed among the other devices under investigation. It indicates that neither the plasma power (Table I) nor the HfO_2 thickness have a significant role in the A_V value. The HfO_2 layer is the high-κ dielectric material, and its thickness dictates the effective oxide capacitance and the drain current in Fig. 4, except for the thinnest Al_2O_3 layer.

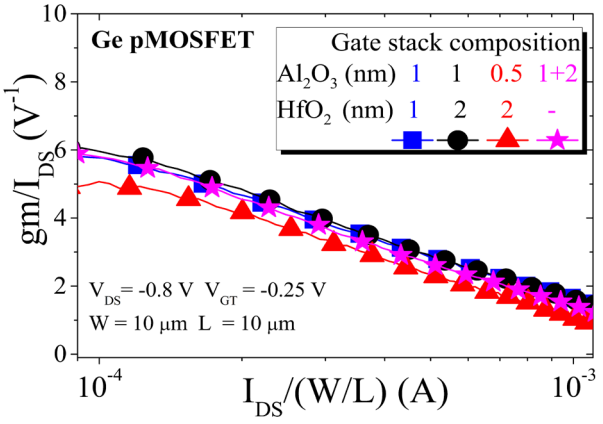

Figure 8. gm over I_{DS} ratio as a function of the normalized drain current for four different gate dielectric compositions.

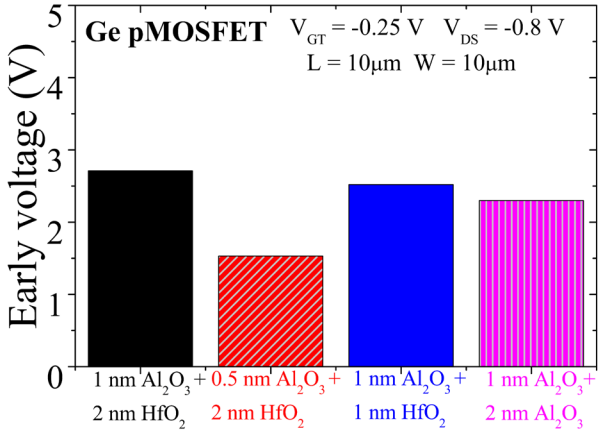

Figure 9. Early voltage for the four different gate dielectric compositions.

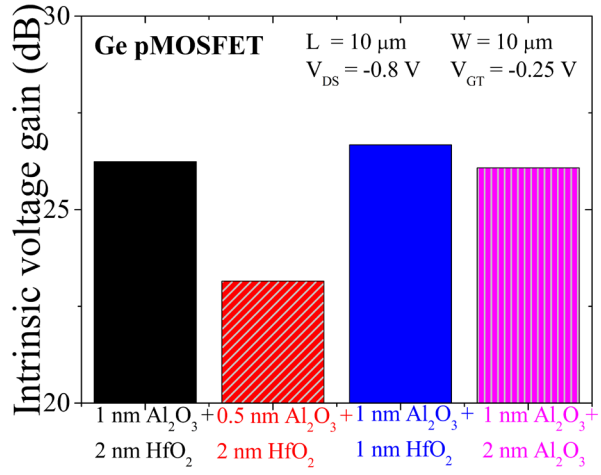

Figure 10. Intrinsic voltage gain for the four different gate dielectric compositions.

IV. CONCLUSIONS

The impact of the gate stack of planar Ge pMOSFETs on the analog parameters and the dynamic threshold voltage operation was evaluated. It is concluded that the gate stack layers can play a strong role

in the device performance, resulting in several effects, such as: a higher subthreshold swing, large I-V hysteresis values, Early voltage and intrinsic voltage gain. In other words, both digital and analog parameters are affected by the gate stack engineering, where the Al_2O_3 layer thickness is a critical parameter for the GeOx passivation and must be taken into account. Finally, apart from the expected benefits of the dynamic threshold voltage modes, i.e., a threshold voltage reduction, drive current boost, subthreshold swing improvement, in addition these techniques showed to be able to minimize effects such I-V hysteresis, since the transversal electric field at the surface is smaller.

Acknowledgements

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