An Analytical Study Of Temperature Dependence of Scaled CMOS Digital Circuits Using α-Power MOSFET Model

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ABSTRACT

Aggressive technological scaling continues to drive ultra-large-scale-integrated chips to higher clock speed. This causes large power consumption leading to considerable thermal generation and on-chip temperature gradient. Though much of the research has been focused on low power design, thermal issues still persist and need attention for enhanced integrated circuit reliability. The present paper outlines a methodology for a first hand estimating effect of temperature on basic CMOS building blocks at ultra deep submicron technology nodes utilizing modified α-power law based MOSFET model. The generalized α-power model is further applied for calculating Zero Temperature Coefficient (ZTC) point that provides temperature-independent operation of high performance and low power digital circuits without the use of conditioning circuits. The performance of basic digital circuits such as Inverter, NAND, NOR and XOR gate has been analyzed and results are compared with BSIM4 with respect to temperature up to 32nm technology node. The error lies within an acceptable range of 5-10%.

Index Terms: Short Channel MOSFET Model, Zero Temperature Coefficient Point, High Performance and Low Power Digital Circuits, Strong and Moderate Inversion Region of Operation, Velocity-Field (υ-E Model), Velocity Overshoot.

I. INTRODUCTION

Digital CMOS circuits are of two categories: high performance and low power logic [1]. In high performance logic circuits, the drive current is in strong inversion region. On the other hand, in low power logic circuits, the drive current is in the moderate inversion region. Process and environment variations affect device characteristics of MOSFETs, thereby varying the performance of integrated circuits [2]. One of the major challenges in robust and reliable circuit design lies in faithfully addressing analytically the effect of temperature variation [3]. Since the operational breakdown of microelectronic chip largely depends on localized operating temperature, generating hot spot, temperature related studies of MOSFET is emerging as an important motivating factor for addressing integrated-circuit (IC) reliability concerns [4][5]. Thus, a first order estimation of temperature effects is required not only for reliability checking but for added degree of freedom to improve circuit performance. Further, the temperature effect on MOSFET characteristics is the basic input for development of temperature related sensors[4].

In this paper an analytical study of α-power law based MOSFET model [6] has been undertaken to understand and accurately model the impact of temperature on MOSFET operation. Although BSIM3 and BSIM4 models for SPICE are widely used to precisely model temperature dependence of MOSFETs and related circuits, the technique is numerical and is not suitable for developing analytical temperature dependent circuit design methodology [7] [8]. An analytical circuit design methodology, optimization and characterization of digital circuits using nanoscale CMOS devices require compact. Such equations need to include first order short channel phenomena relevant to the nanoscale technology nodes. Many researchers have studied compact models to predict the temperature dependent ON-current, based primarily on temperature dependence of carrier mobility and threshold voltage [9] [10]. The temperature-dependent ON-current separating the temperature dependences of the mobility and the saturation velocity has been obtained in [3]. The study is however restricted to only strong inversion region. In the present paper, a physical alpha power model is proposed that includes following modifications:

- For both strong and moderate inversion regions of operation, the basic form of α-power equation originally proposed by Sakurai Newton has been [6].
- For strong inversion region of operation, the three defining parameters of α-power model namely, velocity saturation index α, transconductance parameter K1 and threshold voltage V_h are obtained in terms of physical device parameters.

• In the moderate inversion region since the transport mechanism consists of drift and diffusion of carriers, a compact expression for the three core parameters of α-power model which is physical and suitable for analytical purpose, is not feasible. We use interpolation method following EKV, to obtain expressions for α-power parameters for moderate inversion region which, however, is not completely physical [11].

• The low field mobility μ_0 is a strong function of temperature. The expression used for first order estimation of mobility as a function of temperature as given in the literature have been modified to take into account all three scattering mechanisms (coulomb, lattice, and surface-roughness) [13]. This is in contrast with the other approaches where only the temperature dependence of coulomb scattering is considered [3].

• It is well known that as the device dimensions are scaled down, channel related electric field increases and the saturation of the drain current occurs at a smaller value of the drain voltage as compared to the long-channel drain current-saturation due to the phenomenon of velocity saturation i.e. before the inversion charge pinches-off. Semi-empirical formulations that describe the dependence of surface mobility μ_{eff} on threshold voltage have been used for temperature analysis of carrier mobility.

• An important feature of revisited alpha-power model is to include the effect of velocity overshoot which plays an important part in ultradeep submicron technology node.

The paper is organized as follows: Section II briefly describes the MOSFET model derivation. Section III describes the temperature dependant parameters of MOSFET. Section IV highlights the temperature dependence of α-power based MOSFET model parameters for strong and moderate inversion region. Section V calculates the zero temperature coefficient (ZTC) point voltage utilizing modified α-power model. Section VI and VII applies the modified α-power model for dc and transient characterization of basic digital circuits such as Inverter, NAND, NOR, XOR etc.. Finally, section VIII highlights the important conclusions.

II. MODEL DERIVATION

The drain current at any point x along the length of the channel is given as:

$$I_{ds}=I(x)=WC_{ox}\left(VG-nV(x)\right)\upsilon(x) \tag{1}$$

Here, the factor n takes into account the variations in the bulk charge along the channel, $VG=V_{gs}-V_{th}$, W is the channel width, C_{ox} is the gate oxide capacitance per unit area, $V(x)$ is the potential difference between minority carrier quasi-Fermi potential and equilibrium Fermi potential in the bulk at point x and $\upsilon(x)$ is the carrier velocity at point x. The velocity versus electric field for electrons in the inversion layer is described as:

$$\upsilon(E)=\frac{\upsilon_{sat}\dfrac{E}{E_c}}{\left[1+\left(\dfrac{E}{E_c}\right)^{M}\right]^{\frac{1}{M}}} \tag{2}$$

where υ_{sat} is saturation velocity (m/s), E is the lateral electric field, M is a empirical constant and E_c is the critical field at which the carriers are velocity saturated. It is widely accepted in literature that M = 2 for electrons and M = 1 for holes. Since, the mathematics involved in deriving the drain current with M = 2 involved and tedious [12], following modified first order υ-E model with fitting constants a,b,c and m is proposed:

$$\upsilon(E)=\frac{\upsilon_{sat}a\dfrac{E}{E_c}}{\left[b+c\left(\dfrac{E}{E_c}\right)^{M}\right]^{\frac{1}{M}}} \tag{3}$$

Here,

$$E_c=\frac{m\upsilon_{sat}}{\mu_{eff}} \tag{4}$$

It may be mentioned that our model is an extension of that proposed by [14] that uses 3 constants a,b,c. It is accepted that M = 2 with a, b, c = 1 for electrons and M = 1 with a, b, c = 1 for holes. By introducing four fitting parameters (a,b,c,m), our first order hyperbolic function with four constants faithfully replicates second order hyperbolic function with M=2. The use of first order hyperbolic function enables analytical solution and model simplicity.

μ_{eff} is the effective mobility dependent on the gate voltage given by:

$$\mu_{eff}=\frac{\mu_0}{1+\theta\left(V_{gs}-V_{th}\right)} \tag{5}$$

where θ is the mobility degradation coefficient, μ_0 is the low field mobility, V_{gs} is the gate to source voltage and V_{th} is the threshold voltage. In the presence of parasitic resistance, θ can be expressed [15] as:

$$\theta_m = \theta + \beta_0 R_s \tag{6}$$

Here, β_0 is the value against maximum device transconductance.

The lateral electric field $E(x)$ can be expressed by putting equation 3 in equation 1 and rearranging:

$$E\left(x\right) = \frac{I_{ds} b}{W\mu_{eff} C_{ox} a\left(VG - nV\left(x\right)\right) - \frac{I_{ds} c}{E_c}} \tag{7}$$

By integrating equation 7 from x=0 to x=L (Here, L is effective channel length) and $V(x)$=0 to $V(x)=V_{ds}$, we get the current equation for linear region as:

$$I_{dlin} = \frac{Wa\mu_{eff} C_{ox}\left(VG - n\frac{V_{ds}}{2}\right)V_{ds}}{L\left(b + \frac{cV_{ds}}{E_c L}\right)} \tag{8}$$

Velocity saturation voltage corresponds to the drain bias at which the lateral electric field at the drain end of the channel becomes equal to the critical electric field E_c. Putting $E(x)=E_c$ in equation 7,

$$I_{dsat} = \frac{E_c W\mu_{eff} aC_{ox}\left(VG - nV_{dsat}\right)}{b + c} \tag{9}$$

Equating equation 8 and equation 9 for linear and saturation regions,

$$V_{dsat}^2 \frac{n\left(c-b\right)}{2} + V_{dsat} b\left(VG + nE_c L\right) - E_c VGLb = 0 \tag{10}$$

Physical meaningful root of equation 10 is:

$$V_{dsat} = -\frac{-b\left(VG+nE_c L\right) + \sqrt{\left(b\left(VG+nE_c L\right)\right)^2 - 2n\left(c-b\right)\left(E_c VGLb\right)}}{n\left(c-b\right)} \tag{11}$$

It may be noted that the above equation becomes computationally unstable for c=b. To overcome this problem, finitily small quantity ζ is added in the denominator. Equation 11 represents an improved expression of V_{dsat} proposed to analytically derive the drain current equation of the short channel MOSFETs. In the presence of parasitic source/drain resistance R_s, the expression of saturation drain current can be expressed as:

$$I_{dsat} = \frac{I_{dsat0}}{1 + \frac{R_s I_{dsat0}}{V_{gs} - V_{th}}} \tag{12}$$

where I_{dsat0} is the current when R_s=0. In sub-nanometer range, the parasitic resistance becomes significant and needs to be incorporated in the model equations for acceptable accuracy and prediction [16].

For short channel devices threshold voltage V_{th} becomes drain-substrate bias (V_{ds}) dependent due to the drain induced barrier lowering (DIBL) effect which leads to modification of threshold voltage given by:

$$V_{th}\left(V_{ds}\right) = V_{th} - \sigma V_{ds} = V_{th} - \delta V_{th} \tag{13}$$

where V_{th} is the threshold voltage measured at low V_{ds} (0.1V), called the nominal V_{th}, δV_{th} is the change in the threshold voltage measured at higher V_{ds} from its nominal value, and σ is the DIBL parameter.

Since, the α-power Law MOSFET Model is the most widely used short channel drain current model because of its simpler structure and high level of accuracy, the physical proposed model is thus connected to α-power model. The drain current expressions derived by Sakurai and Newton (SN) [6]:

$$I_{dsat} = \frac{W}{L} B\left(V_{gs} - V_{th}\right)^{\alpha}\left(1 + \lambda V_{ds}\right) \tag{14}$$

$$I_{dlin} = \frac{W}{L} B\left(V_{gs} - V_{th}\right)^{\alpha}\left(2 - \frac{V_{ds}}{V_{dsat}}\right)\frac{V_{ds}}{V_{dsat}} \tag{15}$$

$$V_{dsat} = V_{dsat1}\left(\frac{V_{gs} - V_{th}}{V_{dd} - V_{th}}\right)^{0.5\alpha} \tag{16}$$

$$V_{dsat1} = V_{dsat} \mid V_{gs} = V_{dd} \tag{17}$$

where α is the velocity saturation index, B is the transconductance parameter of SN Model, L is the effective channel length, V_{th} is the threshold voltage, V_{dd} is the supply voltage, λ is the channel length modulation factor, and V_{gs} and V_{ds} are the gate-source and drain-source voltages, respectively. The voltage V_{dsat} determines the boundary between linear and saturation regions. The excellent linearity of the logarithm plots confirms the validity of

$$I_{dsat} = B\left(V_{gs} - V_{th}\right)^{\alpha} \quad (18)$$

Following modification to the SN-model was proposed by [17] for the current equations in the two operating regions:

$$I_{dsat} = K1\left(V_{gs} - V_{th}\right)^{\alpha}\left(1 + \lambda V_{ds}\right) \quad (19)$$

$$I_{dlin} = K1\left(V_{gs} - V_{th}\right)^{\alpha}\left(2 - \frac{V_{ds}}{V_{dsat}}\right)\frac{V_{ds}}{V_{dsat}} \quad (20)$$

$$K1 = \beta_1 + \beta_2 W + \beta_3 W^2 \quad (21)$$

where β_1, β_2 and β_3 are fitting parameters.

Thus, neglecting λ in 19, the saturation drain current can be written as:

$$I_{dsat} = K1\left(V_{gs} - V_{th}\right)^{\alpha} \quad (22)$$

The value of K1 can be found by putting $log(V_{gs}-V_{th}) = 0$. Thus, putting $VG = 1$ in equation 9,

$$K1 = \frac{E_c W \mu_{eff} a C_{ox}\left(1 - nV_{dsat}\right)}{b + c} \quad (23)$$

The physical value of α can be obtained by equating I_{dsat} of α-power law model (equation 22) with proposed model (equation 9),

$$K1\left(V_{gs}-V_{th}\right)^{\alpha} = \frac{E_c W \mu_{eff} a C_{ox}\left(VG - nV_{dsat}\right)}{b + c} \quad (24$$

where V_{dsatn} is given by equation 11.Thus,

$$\alpha = \frac{ln\dfrac{E_c W \mu_{eff} a C_{ox}\left(VG - nV_{dsat}\right)}{b + c}}{ln\left(V_{gs} - V_{th}\right)} \quad (25)$$

As shown above, the model equations that are utilized for calculating the drain current are of strong inversion region. For ultra low power operation, the device current model must be accurate in moderate and weak inversion region to appropriately model delay. Based on the EKV formulas [11], the drain current equation can be expressed as:

$$i_{ds} = ln^2\left(1 + exp\frac{\left(v_{gs} - v_{th}\right)}{2}\right) \quad (26)$$

where

$i_{ds} = I_{ds} / I_{spec}$

$v_{th} = V_{th} / U_T$

U_T is the thermal voltage KT/q and $I_{spec} = 2n\mu C_{ox} U_T^2 W/L$.

Modification of the above model is further proposed to give the value of drain current in moderate inversion.

$$i_{ds} = ln^{\alpha}\left(1 + exp\frac{\left(v_{gs} - v_{th}\right)}{2}\right) \quad (27)$$

The value of α can be calculated by interpolating the strong and weak inversion equation as done by EKV. Figure 1 shows the verification of drain current of n-channel and p-channel MOSFET operating in both strong and moderate inversion with BSIM4.

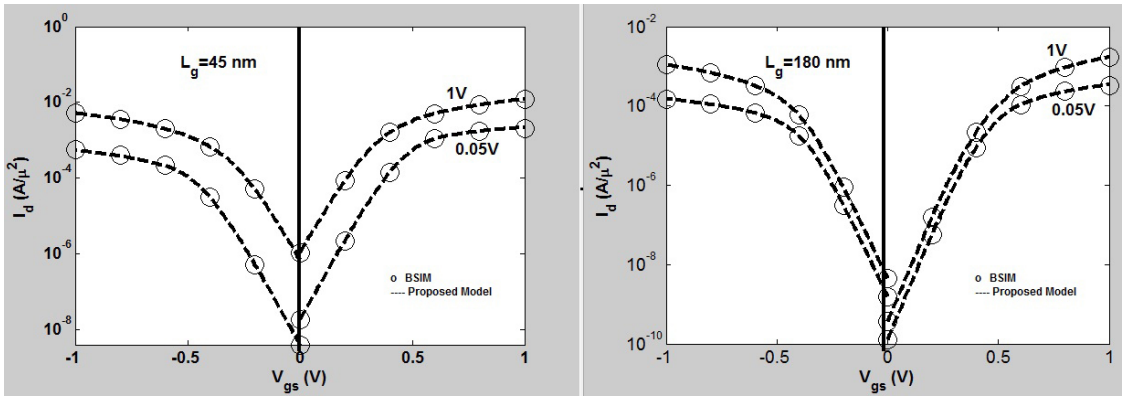

Figure 1. Proposed model verification of drain current of n-channel and p-channel MOSFET with BSIM4.

III. TEMPERATURE DEPENDENT PARAMETERS OF MOSFET

A. Carrier Inversion layer Mobility:

The carrier mobility in semiconductors is related directly to the mean-free time between collisions, which in turn is determined by various scattering mechanisms [18]. The three most important mechanisms are coulomb, lattice, and surface-roughness scatterings.

Coulomb (Impurity) scattering: Coulomb scattering results when a charge carrier travels past an ionized impurity. The effect of coulomb scattering at high temperature is small because the carriers are moving faster and, therefore, scatter less. When the temperature decreases, this mechanism becomes more appreciable because slower electrons are more susceptible to columbic scattering. The coulomb-scattering-limited mobility μ_c is represented as follows [19]:

$$\mu_c \propto \frac{T}{N_I} \tag{28}$$

where T is temperature and N_I is the charge density at the Si-SiO2 interface.

Lattice(Phonon)scattering: Lattice scattering results from thermal vibrations of the lattice atoms at any temperature above zero. These vibrations disturb lattice periodic potential and allow energy to be transferred between the carriers and the lattice. For intermediate inversion-layer concentrations Q_N/q = 0.5 ≈ 5 x 10^{12} cm^2 the channel mobility has been observed to have the following relationships with the effective transverse electric field [20]:

$$\mu_L \propto T^{-n} E_{eff}^{\frac{-1}{\gamma}} \tag{29}$$

where

$$E_{eff} = \frac{0.5Q_N + Q_D}{\varepsilon_{si}}$$

Q_D is the depletion charge density, depending on the crystallographic orientation and the strength of intervallic scattering.

Surface-roughness scattering: Surface-roughness scattering results from the asperities at the Si-Si02 interface at high electron concentrations. The dependence of the surface-roughness scattering-limited mobility μ_{SR} on $E_{e}f$ is given by [21] :

$$\mu_{SR} \propto E_{eff}^{-2} \tag{30}$$

Because the probability of a collision $1/\tau_c$ taking place in unit time is the sum of the probabilities of collisions due to various scattering mechanisms, it follows that:

$$\frac{1}{\tau_c} = \frac{1}{\tau_{c,c}} + \frac{1}{\tau_{c,L}} + \frac{1}{\tau_{c,SR}} \tag{31}$$

Or equivalently (Mathiessen's rule):

$$\frac{1}{\mu_n} = \frac{1}{\mu_c} + \frac{1}{\mu_L} + \frac{1}{\mu_{SR}} \tag{32}$$

The simple temperature-dependent mobility formula used in the SPICE Level 1 model is:

$$\mu_0(T) = \mu_0(300K) \times \left(\frac{T}{300K}\right)^{-1.5} \tag{33}$$

where lattice scattering is assumed to be the only factor that determines the carrier mobility. Because the on-chip temperature could rise upto 120°C and in scaled VLSI technologies, the simple mobility model in equation 33 may not be adequate to cover a wide range of temperatures. However, it is rather difficult to accurately formulate the channel carrier mobility because of the intricate quantum effects [22]. Although some empirical models such as BSIM3v3 uses eight fitting parameters to obtain a fairly good fit for the mobility of a fixed technology, the technology dependence and scaling properties are not well understood. Owing to above reasons, a physically based, semiempirical mobility model developed by [23] has been used to model mobility taking all the three scattering mechanisms:

$$U(T) = \mu_0^{-1}(T)$$

$$U(T) = A1\left[\left(\left(\frac{T}{300}\right)^{-1} - 1\right)\right] + A2\left[\left(\left(\frac{T}{300}\right)^{A3} - 1\right)\right] + A4 \tag{34}$$

The symbol $U(T)$, defined as the inverse of the mobility $\mu_0(T)$, is used for convenience. The A1, A2, A3 and A4 terms are fitting parameters, which are determined by using the nonlinear least-square fitting technique to match the extracted $\mu_0(T)$. Refer [fig. 2].

B. Threshold Voltage

Threshold voltage is another important parameter that increases as temperature decreases due

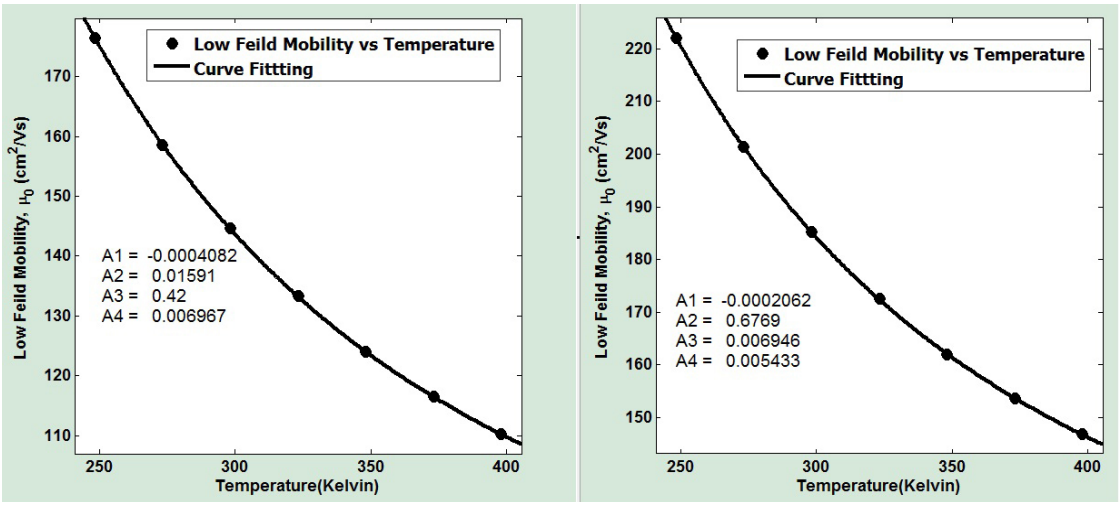

Figure 2. Fitted low field mobility μ_0 with extracted value [24] at a)180nm b)32nm

to the shift in Fermi level and band gap energy. The temperature dependence of threshold voltage given by BSIM3v3 [7] is:

$$V_{th}(T) = V_{th}(T_0) - \alpha_T \frac{T}{T_0} \tag{35}$$

Here $V_{th}(T_0)$ is the threshold voltage at room temperature. α_T is the temperature coefficient of threshold voltage.

C. Saturation Velocity

The saturation velocity dependence on temperature can be expressed as [7]:

$$v_{sat}(T) = v_{sat}0 - \eta(T - T_0) \tag{36}$$

Here $v_{sat}(T)$ is the threshold voltage at room temperature. $v_{sat}0$ is the temperature coefficient of threshold voltage.

As the technology scales, the effect of velocity overshoot becomes prominent and to account for this, following modification is adopted in estimating the saturation velocity V_{sat} [24]:-

$$V_{sat} = V_{sat0} + 0.13\mu_{eff}\sqrt{\tau\mu_{eff}\frac{kT}{q}\left(\frac{V_{ds}}{L^2}\right)} \tag{37}$$

where V_{sat0} corresponds to saturation velocity in the absence of velocity overshoot and τ is the transit time (which in turn depends on V_{sat}) of the carriers leaving the source and arriving at the drain. Due to the effect of velocity overshoot the saturation velocity V_{sat} becomes the linear function of drain saturation voltage.

It can be seen from the figure 3 that at lower technology nodes, the effect of velocity overshoot have to be considered for estimating the performance of MOSFET. Figure 4 shows the verification of temperature dependent drain current at 32nm technology node. It can be seen from the plot that as the temperature is increased, the drain current is decreased.

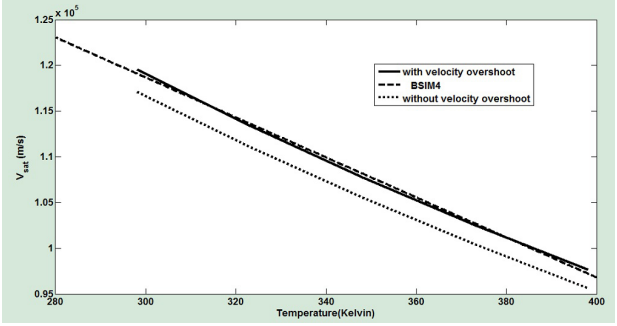

Figure 3. Plot of V_{sat} as a function of temperature at 22nm technology node.

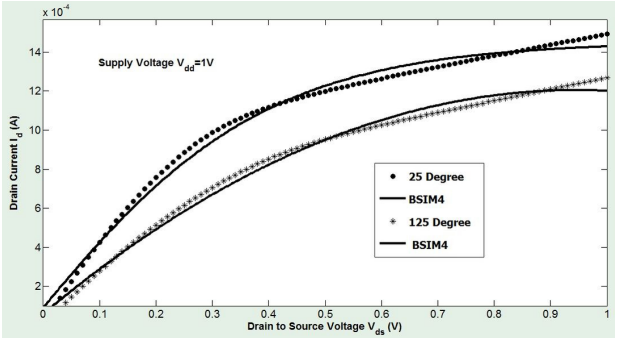

Figure 4. Drain current characteristics of nMOS for 32nm technology node

IV. TEMPERATURE DEPENDENCE OF PROPOSED PHYSICAL α-POWER MODEL PARAMETERS

A. Temperature dependence of α-power model parameters for strong inversion

The values of the three parameters of α-power model i.e. transconductance parameter K1, velocity saturation index α and threshold voltage V_{th} obtained in section 2 (equation 23 and equation 25) has been analyzed at different temperatures with the thermal variations as described in section 3. The temperature dependence of transconductance parameter K1, threshold voltage V_{th} and velocity saturation index α are calculated, plotted and curve fitted into a simpler expressions. Figure 5 shows the temperature dependence of velocity saturation index α within temperature range of 25 to 125 degrees curve fitted to simple quadratic expression and verified through BSIM4.

The variation of α with respect to temperature can be best described using the following expression:

$$\alpha(T) = A(T)^{B} + C \tag{38}$$

Here the parameters A,B,C are the fitting parameters whose values can be found using Levenberg-Marquart algorithm. Similarly, the modification of the value of K1 with respect to temperature calculated and best fitted can be best described using the following expression:

$$K1(T) = D(T)^{2} + E(T) + F \tag{39}$$

Here the parameters D,E,F are the fitting parameters whose values can be found using Levenberg-Marquart algorithm. Figure 6 shows the temperature dependence of transconductance parameter $K1$ within temperature range of 25 to 125 degrees curve fitted to simple quadratic expression and verified through BSIM4.

B. Temperature dependence of α-power model parameters for moderate inversion

The temperature dependent parameters for MOSFET operating in moderate inversion as described by equation 27 are I_{spec} , V_{th}, U_T and α. Thus, rewriting equation 27 in terms of temperature considering the variations of temperature as described in section 3,

$$I_{ds}(T) = I_{spec}(T) \ln^{\alpha(T)}\left(1 + exp\frac{\left(V_{gs} - V_{th}(T)\right)}{2U_T(T)}\right) \tag{40}$$

The figure 7 shows the variation of the specific current I_{spec} with temperature for 32nm n-channel

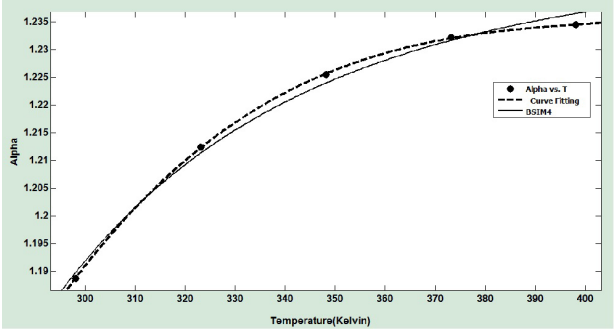

Figure 5. Velocity Saturation Index α dependence on temperature (25-125 Degrees) for 32nm technology node

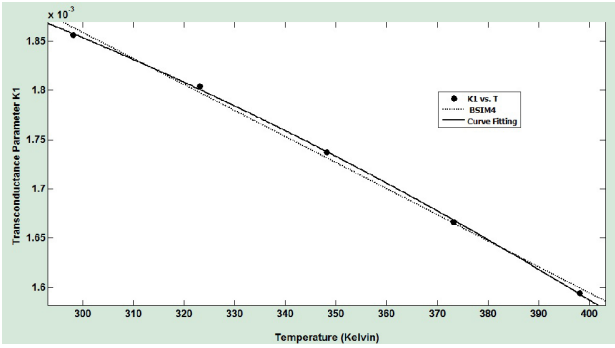

Figure 6. Transconductance parameter (K1) dependence on temperature (25-125 Degrees) for 32nm technology node

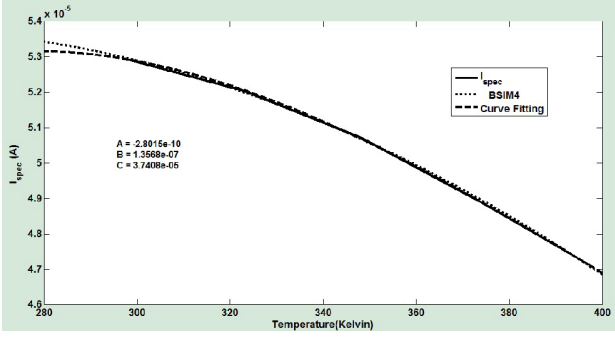

Figure 7. Variation of the specific current I_{spec} with temperature for 32nm n-channel MOSFET.

MOSFET operating in moderate inversion, curve fitted to simple quadratic relationship and its verification with BSIM4. The plot have been curve fitted to the quadratic relationship given in equation 41.

The temperature dependence of specific current I_{spec} is expressed as:

$$I_{spec}(T) = A(T)^{2} + B(T) + C \tag{41}$$

Similarly, The temperature dependence of α for the MOSFET operating in moderate inversion can be calculated through interpolation and is expressed in equation 41. Figure 8 shows the variation of velocity

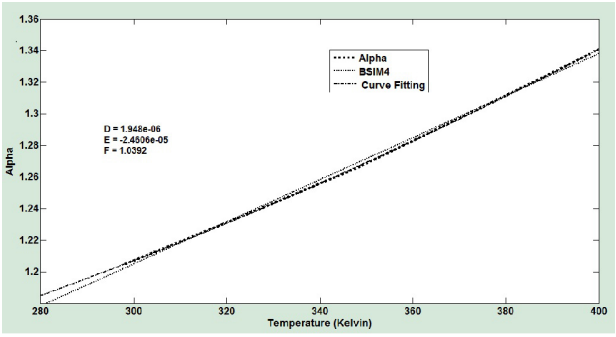

Figure 8. Variation of velocity saturation index α with temperature for 32nm n-channel MOSFET.

saturation index α with temperature for 32nm n-channel MOSFET.

The plot has been curve fitted to the quadratic relationship given in equation 42.

$$\alpha(T) = D(T)^2 + E(T) + F \tag{42}$$

V. DETERMINATION OF ZERO TEMPERATURE COEFFICIENT (ZTC) POINT VOLTAGE

Temperature independent biasing is always required while designing digital or analog circuits and the most popular technique used is the MOSFET operating near its Zero Temperature Coefficient (ZTC) point voltage [25]. Carrier mobility and threshold voltage are two parameters that have major temperature dependence [9] [10]. As the temperature increases, both these quantities decrease. But, the drain current decrease with decrease in mobility while it increase with decrease in threshold voltage. The ZTC point is defined as that bias point at which there occurs a mutual compensation between these two parameters (mobility and the threshold voltage) [26]. Thus, transistor biased near its ZTC point has minimum deviation in its saturation current with temperature. The ZTC point through experimentally plotting the transconductance characteristics at various temperatures have been reported in the literature. The standard method of determining the ZTC point has been to use long channel MOSFET operating in strong inversion region. Such an approach is based on the implicit assumption that ZTC point always pertains to strong inversion region of operation [26][27] [28][29]. In our approach we make use of a general MOSFET alpha-power equation incorporating interpolation method of EKV which provides continuous equation valid both in moderate and strong inversion [11]. Our results show that the ZTC point lies in the moderate inversion region which is verified with BSIM simulations. This result is in contrast to the general perception prevailing in literature that the ZTC point belongs to strong inversion region [26].

A. ZTC utilizing α-power law based on unified drain current model

The continous drain current equation of MOSFET is given by equation 27. Putting the temperature variations of specific current, threshold voltage and velocity saturation index in 27 :

$$I_{ds}(T) = \left(A(T)^2 + B(T) + C\right) * \ln^{\left(D(T)^2 + E(T) + F\right)} \left(1 + exp \frac{\left(V_{gs} - \left(V_{th}(T_0) + \alpha_T\left(T - T_0\right)\right)\right)}{2U_T(T)}\right) \tag{43}$$

For a diode connected MOSFET, in order to get minimum thermal sensitivity, $\frac{dI_{ds}}{dT} = 0$ and then finding the value of V_{gs}.

$$\alpha(T) = D(T)^2 + E(T) + F \tag{42}$$

V_{gs} .

$$\left(AT^2 + BT + C\right) \ln^{DT^2 + ET + F} \left(e^{-\frac{gT - V_{gs} + h}{2tT + 2y}} + 1\right) * \left(\left(2DT + E\right) \ln\left(\ln\left(e^{-\frac{gT - V_{gs} + h}{2tT + 2y}} + 1\right)\right) + \frac{\left(DT^2 + ET + F\right)\left(\frac{2t\left(gT - V_{gs} + h\right)}{\left(2tT + 2y\right)^2} - \frac{g}{2tT + 2y}\right) e^{-\frac{gT - V_{gs} + h}{2tT + 2y}}}{\left(e^{-\frac{gT - V_{gs} + h}{2tT + 2y}} + 1\right) \ln\left(e^{-\frac{gT - V_{gs} + h}{2tT + 2y}} + 1\right)}\right) + \left(2AT + B\right) \ln^{DT^2 + ET + F} \left(e^{-\frac{gT - V_{gs} + h}{2tT + 2y}} + 1\right) = 0 \tag{44}$$

Here, g and h represents the linear coefficient of temperature variation of threshold voltage. x and y represents the linear coefficient of temperature variation of thermal voltage. The value of ZTC point voltage for various technology nodes is given in table 1.

Table 1

Technology (μ)	$V_T(T0)$ (V)	ZTC (BSIM) (V)	ZTC (Analytical) (V)	% Error
0.032	0.242	0.344	0.3330	3.3
0.045	0.257	0.372	0.3639	2.2
0.065	0.258	0.388	0.3815	1.7
0.09	0.263	0.391	0.3856	1.4
0.130	0.265	0.394	0.3898	1.07

VI. TEMPERATURE DEPENDENT DC ANALYSIS OF CMOS INVERTER

A. Unity gain points

The analytical values α-power model parameters i.e α, K1 and V_{th} for strong inversion and its variation with temperature are utilized to calculate the dc and transient characteristics of minimum size CMOS inverter and the results are verified using BSIM.

Maximum input voltage which can be interpreted as logic '0': V_{IL}:

The slope of voltage transfer characteristics i.e. $\frac{dV_{out}}{dV_{in}}$ -1 when the input voltage $V_{in} = V_L$. At that time NMOS operates in saturation and PMOS operates in linear region.

$$K1_n(T)\left(V_{in} - V_{thn}(T)\right)^{\alpha(T)} = K1_p(T)\left(V_{in} - V_{dd} - V_{thp}(T)\right)^{\alpha(T)}\left(2 - \frac{V_{out} - V_{dd}}{v_{dsatp}(T)}\right)\frac{V_{out} - V_{dd}}{v_{dsatp}(T)} \quad (45)$$

The value of V_{IL} at 180nm and 32nm is calculated through proposed model and verified through BSIM by differentiating equation 45 with respect to V_{in} and putting $\frac{dV_{out}}{dV_{in}} = -1$ as shown in the table 2.

Minimum input voltage that can be interpreted as logic '1': V_{IH}:

The slope of voltage transfer characteristics i.e. $\frac{dV_{out}}{dV_{in}} = -1$ when the input voltage $V_{in} = V_H$. At that time nMOS operates in linear and pMOS operates in saturation region.

$$K1_p(T)\left(V_{in} - V_{dd} - V_{thp}(T)\right)^{\alpha(T)} = K1_n(T)\left(V_{in} - V_{thn}(T)\right)^{\alpha(T)}\left(2 - \frac{V_{out}}{V_{dsatn}(T)}\right)\frac{V_{out}}{V_{dsatn}(T)} \quad (46)$$

The value of V_{IH} at 180nm and 32nm is calculated through proposed model and verified through BSIM by differentiating equation 46 with respect to V_{in} and putting $\frac{dV_{out}}{dV_{in}} = -1$ as shown in the table 3.

Table 2: Comparison of minimum size CMOS inverter unity gain point at supply voltage $V_{dd} = 1V : V_{IL}$

Technology	*VIL* (BSIM) (V)	*VIL* (Proposed Model) (V)	% Error
180nm (T=298.15K)	0.429	0.4262	0.65
180nm (T=398.15K)	0.357	0.3532	1.04
32nm (T=298.15K)	0.297	0.301	1.34
32nm (T=398.15K)	0.243	0.24	1.23

Table 3: Comparison of minimum size CMOS inverter unity gain point at supply voltage $V_{dd} = 1V : V_{IH}$

Technology	*VIH* (BSIM) (V)	*VIH* (Proposed Model) (V)	% Error
180nm (T=298.15K)	0.542	0.5379	0.75
180nm (T=398.15K)	0.503	0.4977	1.04
32nm (T=298.15K)	0.539	0.5330	1.11
32nm (T=398.15K)	0.533	0.5283	0.87

B. Switching point V_{sp}

The inverter switching point is defined as $V_{sp} = V_{in} = V_{out}$. Both transistors are operating in saturation region.

$$K1_n(T)\left(V_{in} - V_{thn}(T)\right)^{\alpha(T)} = K1_p(T)\left(V_{in} - V_{dd} - V_{thp}(T)\right)^{\alpha(T)} \quad (47)$$

$$V_{sp}(T) = \frac{V_{thn(T)} + \alpha(T)\sqrt{\frac{K1_p(T)}{K1_n(T)}}\left(V_{dd} + V_{thp}(T)\right)}{1 + \alpha(T)\sqrt{\frac{K1_p(T)}{K1_n}(T)}} \quad (48)$$

It can be seen from the figure 9 that the unity gain point voltage V_{IL} and the switching point voltage V_{sp} decreases as the temperature is increased while V_{IH} is almost independent to change in temperature. The value of V_{sp} at 180nm and 32nm is calculated through proposed model and verified through BSIM by as shown in the table 4.

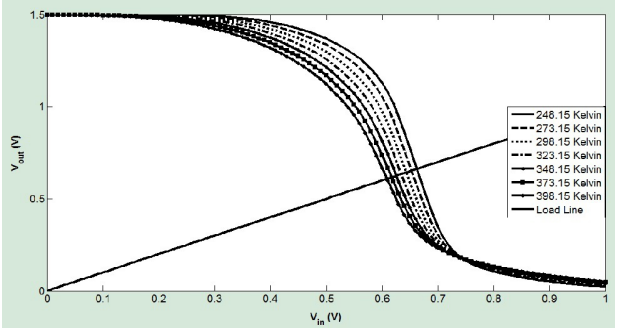

Figure 9. Temperature dependant DC characterization of minimum size CMOS inverter for supply voltage V_{dd} =1.5V at 22nm technology node

Table 4: Comparison of minimum size CMOS inverter switching point voltage V_{th}

Technology	*Vsp* (BSIM) (V)	*Vsp* (Proposed Model) (V)	% Error
180nm (T=298.15K)	0.493	0.4895	0.69
180nm (T=398.15K)	0.452	0.4486	0.74
32nm (T=298.15K)	0.455	0.4526	0.52
32nm (T=398.15K)	0.438	0.4341	0.88

VII. TEMPERATURE DEPENDENT TRANSIENT ANALYSIS OF CMOS INVERTER

The temperature analysis of quarter micrometer MOSFET based digital circuits was performed by [29]. During high-to-low transition, when nMOS transistor starts conducting, it initially operates in the saturation region (from t0 to t1).

When the output voltage falls below V_{dsatn}, the nMOS transistor starts to conduct in linear region (t1 to t2). First let us consider nMOS transistor operating in saturation region. The α-power equation of I_{dsat} for a nMOS such that $V_{dsatn} < V_{out} \leq V_{OH}$ is given by equation 22. The differential equation describing the discharge event is:

$$C_L \frac{dV_{out}}{dt} = -I_d \tag{49}$$

Since the saturation current is practically independent of the output voltage (neglecting channel length modulation), the temperature dependent solution of equation 49 between the time interval t0 to t1 is for output voltage $V_{out} = V_{OH} = V_{dd}$ to $V_{out} = V_{dsatn}$ is:

$$t_1 - t_0 = \frac{C_L}{K1_n(T)\left(V_{dsatn}(T)\right)^{\alpha(T)}}(V_{dd} - V_{dsatn} \tag{50}$$

At t=t1, the output voltage will be equal to V_{dsatn} and the transistor will be at the saturation-linear region boundary.

Now, let us consider the transistor operating in linear region. The equation described below for linear region.

$$I_{dn}(T) = K1_n(T)\left(V_{in} - V_{thn}(T)\right)^{\alpha(T)} * \left(\frac{2V_{out}(T)}{V_{dsatn}(T)} - \frac{V_{out}(T)^2}{\left(V_{dsatn}(T)\right)^2}\right) \tag{51}$$

The solution of equation 51 in the time interval from t_1 to t_2 for $V_{out} = V_{dsatn}$ to $V_{out} = V_{50\%}$ and $V_{in} = V_{dd}$ is:

$$t_2 - t_1 = \frac{2C_L V_{dsatn}(T)}{K1_n(T)(V_{dd} - V_{thn}(T))^{\alpha(T)}} ln \frac{2V_{dsatn}(T) - V_{50\%}}{V_{50\%}} \tag{52}$$

The propagation delay for high-to-low output transition τ_{PHL} can be calculated by adding the results obtained in equation 50 and equation 52:

$$\tau_{PHL}(T) = \frac{C_L}{K1_n(T)\left(V_{dsatn}(T)\right)^{\alpha(T)}}(V_{dd} - V_{dsatn}(T)) + \frac{2C_L V_{dsatn}(T)}{K1_n(T)(V_{dd} - V_{thn}(T))^{\alpha(T)}} ln \frac{2V_{dsatn}(T) - V_{50\%}}{V_{50\%}} \tag{53}$$

Table 5 shows the variation of propagation delay of minimum size basic digital gates driving the FO4 load with temperature and supply voltage.

Table 6 shows the comparison of propagation delay for a minimum size CMOS inverter for V_{dd} =1V with BSIM4.

Figure 10 shows the variation of propagation delay with respect to supply voltage and temperature

Table 5: Temperature variation of propagation delay(s) of CMOS based basic digital circuits at 180nm and 32nm technology node

*180nm CMOS Technology	Temp.(K)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2
	298.15	2.54E-11	9.11E-11	1.38E-10	1.29E-10	2.80E-10	6.92E-11
	398.15	3.01E-11	1.10E-10	1.54E-10	1.47E-10	2.51E-10	6.29E-11
% Variation		18.5	20.7	11.6	14	10.3	9.1
		Supply=0.9V					
*180nm CMOS Technology	Temp.(K)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2
	298.15	5.66E-11	4.05E-10	5.78E-10	3.04E-10	6.51E-10	1.62E-10
	398.15	5.69E-11	4.03E-10	5.80E-10	3.01E-10	6.52E-10	1.61E-10
% Variation		0.53	0.49	0.34	0.98	0.15	0.61
		Supply=0.9V					
*32nm CMOS Technology	Temp.(K)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2
	298.15	1.56E-12	5.34E-12	8.63E-12	6.66E-12	1.38E-11	2.12E-12
	398.15	1.014E-12	2.56E-12	4.07E-12	3.17E-12	0.66E-11	1.14E-12
% Variation		35.0	52.0	52.8	52.4	52.1	46.1
		Supply=0.36V					
*32nm CMOS Technology	Temp.(K)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2
	298.15	1.82E-12	9.54E-12	1.11E-11	2.55E-11	4.33E-11	6.66E-12
	398.15	1.81E-12	9.47E-12	1.10E-11	2.53E-11	4.28E-11	6.63E-12
% Variation		0.41	0.71	0.90	0.77	0.94	0.33

Table 6: Comparison of propagation delay for a minimum size CMOS inverter for $V_{dd} = 1V$

Technology	τ_{phl} (BSIM)	τ_{phl} (Proposed Model)	% Error
180nm (T=298.15K)	6.8701E-12s	6.648E-12s	3.23
180nm (T=398.15K)	7.5833E-12s	7.3805E-12s	2.67
32nm (T=298.15K)	1.1304E-12s	1.096E-12s	2.98
32nm (T=398.15K)	1.2545E-12s	1.2308E-12s	1.85

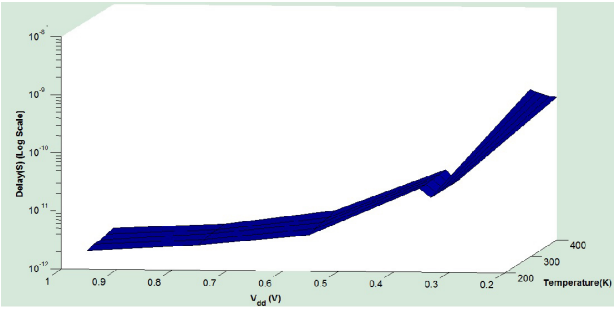

Figure 10. Variation of propagation delay with respect to supply voltage and temperature for 32nm minimum size CMOS inverter

for 32nm minimum size CMOS inverter. It can be seen from the figure that at a particular supply voltage, the temperature dependence of CMOS inverter is negligible (known as temperature inversion voltage (TIV)). After TIV, the delay characteristics with respect to supply voltage are reversed. Thus, following observations are made:

1. Propagation delay increases with increase in temperature and decrease in supply voltage V_{dd}.
2. There is an optimum supply voltage where the propagation delay becomes independent of the change in temperature. This voltage is known as temperature inversion point voltage (TIV). After TIV, the propagation delay increases with increase in supply voltage as shown in figure 10.
3. Thus, any circuit biased at TIV will have minimum deviation in delay with respect to temperature.
4. TIV depends on the length of the channel.

VIII. CONCLUSION

Following points are concluded:

• An α-power law based simple, physical and analytical model is presented that is related to primary short channel phenomenon for scaled bulk MOSFET devices. The model is compact and suitable for analytical study of temperature dependence of MOSFET circuits.

• Temperature dependence of carrier inversion layer mobility has been modified to include all the three scattering mechanisms.

• Temperature dependence of saturation velocity has been upgraded to include the secondary effect of velocity overshoot.

• Temperature dependence of three parameters of α-power model (velocity saturation index α, transconductance parameter K_1 and Threshold voltage V_{th0}) has been calculated and presented with a curve fitted expression.

• Zero temperature coefficient point voltage has been calculated utilizing modified α-power law based model for MOSFET operating in strong inversion and unified α-power based model for MOSFET operating in moderate inversion region. The results have been compared with BSIM4 and the error lies within the acceptable range of 2-4 %.

• An important finding of the investigation is that ZTC point belongs to the moderate inversion region of operation of MOSFET device. This result was obtained because of the fact we use a continuous expression for alpha power law valid both for strong and moderate inversion region. This was overlooked in earlier investigations because the ZTC point was obtained using strong inversion equation.

• For unified α-power based model, the temperature dependant parameters like specific current I_{spec}, velocity saturation index α and threshold voltage is calculated and presented with a curve fitted expression.

• CMOS inverter DC characteristics have been analyzed to calculate noise margins and switching threshold point. It has been found that the unity gain point V_{IH} voltage is almost independent of temperature change.

• The temperature dependent transient behavior of basic CMOS based digital gates is analyzed and tabulated in table 5.

• It is shown analytically that alpha power law predicts an optimum supply voltage where the propagation delay becomes independent of the change in temperature for scaled CMOS devices. This voltage is known as Temperature Inversion Point voltage (TIV).

• The capability of alpha power model can be extended to faithfully predict circuit performance of MOSFET based temperature sensor

• The revisited alpha-power model is capable of predicting temperature dependent behavior of CMOS digital circuits with process variation.

ACKNOWLEDGEMENT

Authors would like to thank Mentor Graphics (MG) for their partial financial support.

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