A Physics-Oriented Parameter Extraction Method for MOSFET Libraries Generation

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ABSTRACT

A novel method for MOSFET parameter extraction based on EKV 2.6 model is presented. The proposed method improves and updates the previous ones found in literature, since it describes setups and equations for the extraction of intrinsic DC parameters, not requiring any fitting procedures or optimization steps, as demanded by the previous ones. The physical approach used in the analysis allowed the achievement of these features, leading to the generation of libraries valid in all operating regions. Due to this approach, the method can be applied to new technologies or to harsh environments (such as cryogenic temperatures), where commercial libraries are not yet available. Validations of the method were done with data extracted from BSIM3v3 simulated curves, at room temperatures, and with experimental curves of an AMS 0.35µm transistor at 77K. In both cases, the EKV 2.6 generated libraries were able to reproduce the transistors behavior with errors less than 6%.

Index Terms: Semiconductor device modeling, Field Effect Transistors, parameter extraction

I. INTRODUCTION

THE EKV model is a scalable and compact simulation model built on the physical properties of the MOS structure. This model is dedicated to the design and simulation of low-voltage, low-current, analog or mixed-signal circuits using submicron CMOS technologies. It is formulated as a "single expression", which preserves the continuity of first and higher-order derivatives with respect to any terminal voltage in the entire range of the model. EKV 2.6 model provides very good simulation results for analog circuits, requiring only eighteen DC parameters. The physical approach of this model and the low number of parameters make parameter extraction more comprehensible [1-4] and useful for specific applications where MOSFET libraries are unknown. Even being an old model, and currently being overcome by some others with higher accuracy, EKV 2.6 already shows to be a good option for a first approach of analog projects, which are designed with transistors that do not suffer with most of the more complex short-channel effects. Technology nodes bigger than 0.18μm are perfect for this kind of project and presents a good trade-off for using EKV 2.6. When compared to BSIM3v3 model, currently the most used simulation model, it presents a much lower number of parameters and a better accuracy. While BSIM3v3 shows errors near 40% [1] in moderate inversion, EKV prediction is close to the ideal one.

Although existing for about 20 years, a complete method for extracting all parameters of EKV 2.6, based only on physical features was not found in literature. Most methods and extraction tools, like IC-CAP (Keysight) and UTMOST (Silvaco) [5-8], use some kind of fitting, presenting a number of optimization steps and searching for the best parameters that could minimize the differences between simulated and experimental curves. These existing methods usually find good mathematical solutions but sometimes loose the relationship with the physical mean of parameters. At room temperatures and vicinities, where the model is well described, this fitting approach is not a problem, but when migrating to harsh environments, such as cryogenic temperatures (lower than 200K), where the model is not valid anymore, the lack of a relationship with physical parameters may lead to errors, due to many additional effects [9-13].

In this context, it is desirable to develop a method to overcome the previous drawbacks and to generate libraries for specific applications, achieving accuracy and a quick turnaround time in projects.

This paper presents a novel method for EKV 2.6 intrinsic DC parameters extraction. It is based on the physical properties of the devices and on the equations of the model, requiring only four experimental setups, even when short-channel effects are considered.

It allows a quick and accurate generation of transistor libraries, allowing circuit simulations in all conditions.

This paper is organized as follows. In Section II, some existing extraction methods and the proposed one are presented and detailed. In Section III our method is validated through two different examples and finally, Section IV presents some concluding remarks concerning to the results.

II. EKV 2.6 PARAMETER EXTRACTION METHODS

Before describing the existing methods and the proposed one, it is worth to show a brief description of each one of the parameters that compose EKV2.6 model libraries, focusing on a better understanding of the methods. In this sense, Table 1 summarizes all eighteen parameters, depicting their physical meaning and the used setup for their extraction in the proposed method (to be shown in subsection B). It is important to highlight that the first four parameters (*COX*, *XJ*, *DW* and *DL*) are "process related parameters", and are not extracted, but accessed from the node technology specifications. The next eleven parameters (*VT0*, *GAMMA*, *PHI*, *KP*, *E0*, *LAMBDA*, *UCRIT, LETA*, *WETA*, *Q0* and *LK*; and even the I_s that is a normalization factor for currents and voltages) are described in the present work, composing our full approach for the physical method. Finally, the last three parameters (*IBA*, *IBB* and *IBN*) are proposed to be used as default values (such as *IBA* = 0, *IBB* = 3E9 and *IBN* = 1), once no simple method was developed to the time of submission of this paper, and that, considering the variability in CMOS processes and the difference between different runs of the same foundries, they show to be of minor importance to the accuracy of the model, once the substrate current (*IB*) (influenced by these parameters) reach only a few pA (PMOS) and nA (NMOS), even at 77K.

Table 1. Description of the main parameters of the EKV 2.6 Model

Parameter	Description
L	**Channel Length.** It depends on the design. It is not extracted but a specification, composing the geometry of the device
W	**Channel Width.** It depends on the design. It is not extracted but a specification, composing the geometry of the device
1 - COX	**Gate Oxide Capacitance per unit area.** It is a "process related parameter". It is defined as a function of the *TOX* (gate oxide thickness) - $COX=\varepsilon ox/TOX$.
2 - XJ	**Junction Depth**. It is a "process related parameter". It is the depth (measured from the surface) of the plane in p-n junction at which concentration of acceptors is equal to the concentration of donors. It can be achieved from the technology parameters.
3 - DW	**Channel Width Correction**. It is a "process related parameter". It is usually a negative value and refers to the overlap between the field oxide and the gate.
4 - DL	**Channel Length Correction**. It is a "process related parameter". It is usually a negative value and refers to the overlap between the source (or drain) and the gate.
5 - VT0	**Setup #2 (diode connection and a current source - *IS* in the Source terminal)** **Long-channel threshold voltage**. It is a "basic intrinsec model parameter". It is referred to the bulk and it can be defined as the gate voltage (VG) at which the channel is in equilibrium (V_{ch}=0) and the inverted charges (greater than $2\varphi_F$) equal zero.
6 - GAMMA	**Setup #2 (diode connection and a current source - *IS* in the Source terminal)** **Body Effect Parameter**. It is a "basic intrinsec model parameter". It is the effect in which a voltage difference between the substrate and the source modifies the width of the depletion layer of the p-n junction, implying a change in voltage across the oxide.
7 - PHI	**Setup #2 (diode connection and a current source - IS in the Source terminal)** **Bulk Fermi potential**. It is a "basic intrinsec model parameter". It represents an approximation of the surface potential (ψ_S) in strong inversion.
8 - KP	**Setup #3** **Transconductance parameter**. It is a "basic intrinsec model parameter". It is It is proportional to the relationship between the variation of the drain current and the variation of the gate voltage.
9 - E0	**Setup #3** **Mobility reduction coefficient**. It is a "basic intrinsec model parameter". It is the sensitivity to the vertical electric field to which occurs the reduction of mobility.

10 - LAMBDA	**Setup #4** **Depletion length coefficient (channel length modulation)**. It refers to an increase of the depletion layer between D and G as the drain voltage is increased.
11 - UCRIT	**Setup #4** **Longitudinal critical Field**. It is a "basic intrinsec model parameter". It is the relationship between the saturation of carrier drift velocity and the carrier mobility.
12 - LETA	**Setup #2 (diode connection and a current source - IS in the Source terminal)** **Short-channel effect coefficient**. It refers directly to changes imposed on the transistor body effect parameter (GAMMA) caused by short gate length
13 - WETA	**Setup #2 (diode connection and a current source - IS in the Source terminal)** **Narrow-channel effect coefficient**. . It refers directly to changes imposed on the transistor body effect parameter (GAMMA) caused by short gate width.
14 - Q0	**Setup #2 (diode connection and a current source - IS in the Source terminal)** **Reverse short channel effect peak charge density**. It refers to a phenomenon occurred in regions close to the drain and source due to non-uniform doping influenced by the concentration of doping. May be due to the pile-up phenomenon or to the existence of "pocket implants" and to "Low doped Drain", in order to control the threshold voltage of the transistors in order to avoid channel effect short reverse, RSCE.
15 - LK	**Setup #2 (diode connection and a current source - IS in the Source terminal)** **Reverse short channel effect characteristic length**. It refers to a phenomenon occurred in regions close to the drain and source due to non-uniform doping influenced by the characteristic length of doping. May be due to the pile-up phenomenon or to the existence of "pocket implants" and to "Low doped Drain", in order to control the threshold voltage of the transistors in order to avoid channel effect short reverse, RSCE.
16 - IBA	**First impact ionization coefficient**. It refers to a typical non-equilibrium process that requires a large longitudinal electric field. An electron in the conduction band has its energy increased by applying external longitudinal electric fields. This energy can be as high as the electron is able to create an "electron-hole" after colliding with an electron in the valence band, exciting it to the conduction band. It is used directly to calculate the substrate current (I_{DB}), being a fitting parameter.
17 - IBB	**Second impact ionization coefficient**. It refers to a typical non-equilibrium process that requires a large longitudinal electric field. An electron in the conduction band has its energy increased by applying external longitudinal electric fields. This energy can be as high as the electron is able to create an "electron-hole" after colliding with an electron in the valence band, exciting it to the conduction band. It is used directly to calculate the substrate current (I_{DB}) , being a fitting parameter.
18 - IBN	**Saturation voltage factor for impact ionization**. It refers to a typical non-equilibrium process that requires a large longitudinal electric field. An electron in the conduction band has its energy increased by applying external longitudinal electric fields. This energy can be as high as the electron is able to create an "electron-hole" after colliding with an electron in the valence band, exciting it to the conduction band. It shows to be a correction factor for the drain-source voltage (VDS).

A. Existing Parameter Extraction Methods

Literature provides some methods for extracting DC EKV parameters of MOSFET transistors. Each one of them presents advantages and disadvantages, depending on the proposed application, but all analyzed methods seem to use some kind of fitting approach [14-27].

The BSIM2EKV [15] is a software/method that converts/optimizes parameters from BSIM3v3 to generate EKV libraries. However, it requires a pre-existing valid library (that will be converted) and a commercial simulation software (to optimize the initial set of parameters, until the results achieve the desired accuracy). Thus, it cannot be used in prospecting technologies or in harsh environments, where libraries are unknown.

Another method was previously proposed by Bucher, Lallement and Enz [14,23]. It describes the extraction of two basic parameters: the pinch-off voltage and the specific current *(VP* and I_s*)*. No explanations about the other parameters of the model are given, leading to the conclusion that they should be extracted by fitting the experimental data. Besides that, the provided setups and equations do not refer to the short-channel parameters extraction, such as for *LK*, *Q0* and *E0*. It seems to be mostly a parameter optimization than a physical parameter extraction, what lead to the previous explained drawbacks.

Regarding to [18-22], all articles refer to EKV2.6 model. They suggest how the transistor should be biased (region of operation), but do not describe experimental setups or an extraction method itself. Disregarding the parameters *VP* and I_s, which were previously described in [14,23], the other parameters of the model (*LETA*, *WETA*, mobility, *UCRIT*, *LAMBDA*, *LK* and *Q0*) are not detailed, suggesting a fitting procedure for their extraction.

There is an additional method [16,17] that focuses on a parameter extraction for the EKV3.0 model. It presents the regions of operation where the transistor should be biased, but do not present the roadmap to the parameters extraction, suggesting, as well, a fitting of parameters of the equations to achieve the experimental curves (database). The complexity of this model, the high number of covered effects (generally more complex short-channel effects) and, consequently, the high number of intrinsic parameters avoid an easy and self-explanatory extraction, not showing to be a good option for a quick and easy first approach of a project where the technology is already unknown.

Software packages, such as IC-CAP (Keysight) and UTMOST (Silvaco) [5-8] provide an automated parameter extraction, performing it on a set of pre-defined equations of the model. However, in situations where the equations are no longer valid, like at cryogenic or high temperatures, these options seem to be ineffective due to different effects.

B. Proposed Method

The proposed extraction method is based on four different measurements. In this section, transistor biasing are shown, as an example, to the AMS 0.35μm technology node, but all setups can be dimensioned to any other technology, as specified.

The first measurement focuses on the Specific Current extraction, I_s. Both the experimental setup and the physical equations are well described in [14,23]. Therefore this work does not rely on it. The Specific current, I_s, is a normalization factor of the currents and voltages in EKV2.6 Model, being also used for biasing the transistor on the pinch-off voltage - *VP*, extraction.

The second measurement focuses on the pinch-off voltage, *VP*, of the transistor. This parameter corresponds to the potential of the channel to which the inverted charges become zero in a non-equilibrium situation [14]. Most of the other parameters will be extracted based on this setup, such as: *VT0, GAMMA, PHI, LETA, Q0* and *LK*. Although the experimental setup is well-described in [14,23], the procedures to extract most of the related parameters are not clear. Below, it is proposed a reasonable and improved roadmap for all parameter extractions, which will be summarized at the end of this section.

Based on the second setup [14,23] applied to long and wide transistors (where long and wide refer to transistors with gate dimensions bigger than 10λ, for any node technology), and on a typical *VP vs.VG* curve (shown in Fig.1), it is possible to verify *VP* to gate voltage variations, *VG*. In EKV model, by definition, the threshold voltage – *VT0* corresponds to the gate voltage at which channel inversion charges are equal to zero in equilibrium, i.e., when the pinch-off voltage is zero [14]. Therefore, *VT0* can be extracted directly, and corresponds to the gate voltage where *VP* is equal to zero (see Fig.1).

By determining two points in the linear part of the *VP vs.VG* curve, it is possible to extract *GAMMA* and *PHI*, based on the system of equations (1), where V_G' is the effective gate voltage and γ' is the body effect including short- and narrow-channel effects, as shown in (2).

The parameter *GAMMA* addresses the body effect for large devices, where large devices are considered those ones that present both the length and width of the channel bigger than 10λ. Once this extraction concerns for large devices, parameters related to Short-Channel Effects, like *LETA* and *WETA*, are considered equal to zero, what is not true as channel geometry shrinks. *LETA* and *WETA* will be focused on the next step of this extraction Method. The point P2 (higher *VG,* in Fig.1) is located in a region where this effect is quite pronounced (*VP=VS>>VB,* where *VS* is the Source Voltage and *VB* is the Bulk Voltage). The other point (P1, in Fig.1), chosen in a lower *VG,* but already in the linear part of the *VP vs.VG* curve, completes the system with two variables (*GAMMA* and *PHI*) and two equations, shown in (1) [28].

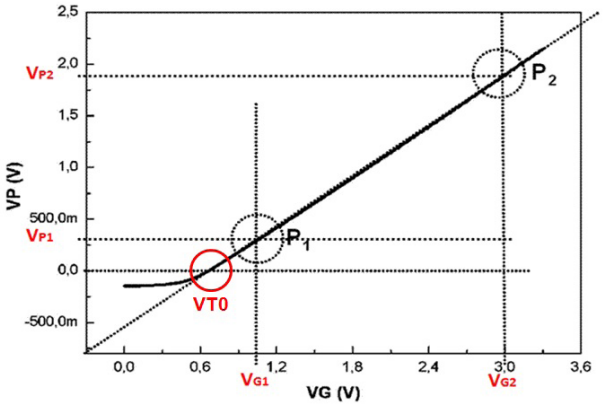

Figure 1. Typical characterization *VP vs. VG* for extracting *VT0*, *GAMMA* and *PHI* (long and wide transistors).

$$\begin{cases} V_{P1} = V_{G1}' - PHI - \gamma' \cdot \left[\sqrt{V_{G1}' + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2} \right] \\ V_{G1}' = V_{G1} - V_{T01} + PHI + GAMMA.\sqrt{PHI} \\ V_{P2} = V_{G2}' - PHI - \gamma' \cdot \left[\sqrt{V_{G2}' + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2} \right] \\ V_{G2}' = V_{G2} - V_{T02} + PHI + GAMMA.\sqrt{PHI} \end{cases} \quad (1)$$

$$\gamma' = GAMMA - \frac{\varepsilon_s}{COX} \cdot \left(\frac{LETA}{L + DL} \cdot \sqrt{PHI + VD} + \left(\frac{LETA}{L + DL} - \frac{3.WETA}{W + DW} \right) \cdot \sqrt{PHI + VS} \right) \quad (2)$$

It is also possible to use the same setup of *VP vs.VG* [14,23] to extract *LETA* and *WETA* (short- and narrow-channel effects coefficients), which are related to the body effect, and consequently to the *VT0*. By characterizing short-channel devices (close to the minimum gate length of the technology) and making *WETA*=0 in (2), before applying it on (1), it is possible to calculate *LETA*, once the other parameters were already extracted. It is easily done with the aid of the symbolic mathematic. The same applies for *WETA* extraction, but this time making *LETA*=0, characterizing a narrow-channel device (close to the minimum gate width of the technology) and using the same procedure previously explained. Thus, it is necessary to characterize two different devices for *LETA* and *WETA* extraction: a short channel and a narrow-channel device.

The extraction of *Q0* (reverse short-channel effect peak charge density) and *LK* (Reverse short-channel effect characteristic length) can also be achieved by using the setup of *VP vs.VG* [14,23]. A set of short-channel devices may be used (preferable such as: 1.0, 1.2, 1.4, 1.6, 1.8 and 2.0 L_{min}). The main impact of these two parameters relies on the threshold voltage - *VTH* of short-channel devices, which may be extracted exactly in the same way of *VT0* extraction (*VT0* is defined as the *VTH* of a big transistor). A mapping of *VTH (VT0) versus* L_{eff} for this set of transistors (as seen in Fig.2) must be done. In Fig.2, the Reverse Short-Channel effect (RSCE) can be clearly perceived, once *VTH* increases as channel decreases, instead of decreasing, as it would be expected based only on Short-Channel Effects. RSCE is a direct result of non-uniform channel doping, known as halo doping, developed to avoid drain-induced barrier lowering (DIBL). In this case, channels are more doped near the source and drain to minimize the size of the depletion region in these junctions. If the channel length is short, both halo overlap each other, increasing the channel doping and increasing the threshold voltage, as depicted in Fig.2. This effect is minimized if channel length increases, once halos do not overlap any more, leading to a constant *VTH*.

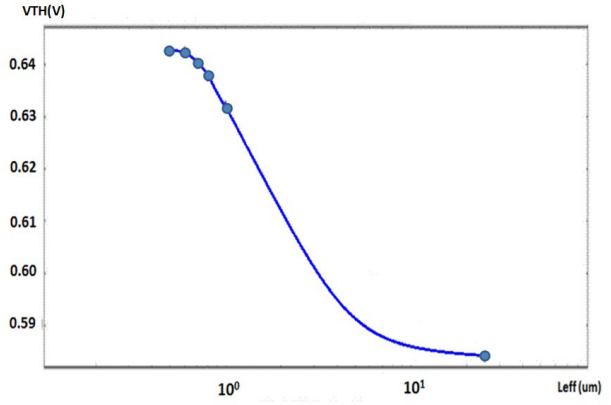

Figure 2. Mapping of *VTH vs.* L_{eff} for short-channel devices

In this case, two points must be chosen, preferable in the linear part of the graph, and applied on (3) and (4), considering *VG=VD=VTH* and *VB=VS=0,* where *VS* is the Source Voltage, *VB* is the Bulk Voltage and *VD* is the Drain Voltage. In (3), *VT0* shall be considered the one previously extracted from large devices (long and wide) [28].

$$V_{TH} = V_{T0} + \Delta V_{RSCE} + \gamma' \sqrt{V_S'} - GAMMA\sqrt{PHI} \quad (3)$$

$$V_S' = \frac{1}{2} \cdot \left[V_S + PHI + \sqrt{(V_S + PHI)^2 + (4V_t)^2} \right] \quad (4)$$

By using (3), (4) and choosing two transistors (points of the *VTH vs.* L_{eff} curve, in Fig.2), it is possible to find, firstly, ΔV_{RSCE}. This value is a function of the two parameters of interest (ΔV_{RSCE} = f(*LK*, *Q0*)) [24]. Therefore, by solving the system of equation (5) for these two ΔV_{RSCE}, with the aid of symbolic mathematic, it is possible to extract both variable, *LK* and *Q0*; where C_A=0.028 and C_ξ=0.001936 are both constants [28].

$$\begin{cases} L_{eff} = L + DL \\ \xi = C_A \cdot \left(10. \frac{L_{eff}}{LK} - 1 \right) \\ \Delta V_{RSCE} = \frac{2Q0}{COX} \cdot \frac{1}{\left[1 + \frac{1}{2} \left(\xi + \sqrt{\xi^2 + C_\xi} \right) \right]^2} \end{cases} \quad (5)$$

The third measurement is a novel approach for the EKV model parameter extraction, being based on big (long and wide) devices biased in the linear region of operation. The curve *ID vs.VG,* and its derivative, shall be measured. To extract the parameters transconductance - *KP* and Vertical Characteristic Field for

Mobility Reduction - *E0*, the transistor must be biased with *VD*=0.05V, *VG* varying from 0 to VDD (3.3V, in 0.35μm technology) and *VB*=*VS*=0=GND. Figure 3 depicts a typical characterization curve used for the extraction of these parameters.

In Fig.3, the blue line relates to the drain current (*ID* or I_D) of the device, while the red line relates to its derivative. I_D can be approached by [28]:

$$KP = \mu.COX = \frac{I_D}{\frac{W}{L}.V_D.(V_G - V_{T0})} \quad (6)$$

for a long and wide transistor operating in the linear region, and considering a low *VD* [24]. In this equation all parameters are known, except *KP*. It is defined that *KP* will be calculated for the *VG* to which the maximum derivative point of the curve is achieved, once at this point we have the minimum influence of the vertical field (from the gate to the bulk), and thus, the maximum transconductance.

Using the same experimental curve, it is possible to extract the parameter *E0*. First, a Mobility Reduction Coefficient, which is based on the derivative of the Drain Current Curve, shall be calculated. Considering (6), it is possible to write:

$$\mu = \frac{I_D.L}{COX.W.V_D(V_G - V_{T0})} = \frac{L}{COX.W.V_D}.g_m \quad (7)$$

where *gm* is the transconductance of the transistor. This equation shows a linear relation between μ and *gm*. Considering that *VD* is small, and the transistor is operating in the linear region of the curve, the mobility will be independent of the horizontal and vertical electric fields [25]. The maximum mobility value is determined at the point of maximum transconductance. From that point on, the transconductance and the mobility decrease in a quite-constant rate. This rate is defined as the Mobility Reduction Coefficient – θ, and can be modeled by the left hand of (8), where the maximum derivative point is proportional to μ_0 and the following ones are proportional to μ. Then it is possible to approximate *E0*, as:

$$\frac{\mu_0}{\mu} = 1 + \theta.(V_G - V_{T0}) \Rightarrow E0 = \frac{0.2}{\theta.tox} \quad (8)$$

The setup proposed for LAMBDA (channel-length modulation) and UCRIT (Longitudinal Critical Field) extractions is also a novel one, being based on short and wide devices biased in strong inversion and in saturation region. Transistors must be biased with *VG* close to VDD (*VG*=3.2V, in 0.35μm technology), *VB*=*VS*=0=GND and *VD* varying from 0 to VDD (3.3V, in 0.35μm technology).

For extracting UCRIT, one must define (or measure) the drain voltage *VD* corresponding to the saturation voltage (*VDsat*), as shown in Fig.4, "Point 1".

Once *VDsat* is the point where we have the transition from the linear to saturation regions, for short and wide devices, the saturation region will present an almost constant derivative (and close to zero), while the linear region presents high variation. Therefore, if the model extraction shows to be a very preliminary one, it can be done through a visual inspection, only by determining the *VD* where the *ID* curve tends to a constant derivative. But, for more accurate models, we suggest using a method based on the second derivative, where the *VDsat* is determined after extracting the second derivative of the *IDxVD* curve and checking a steep transition to "zero". This point will be an

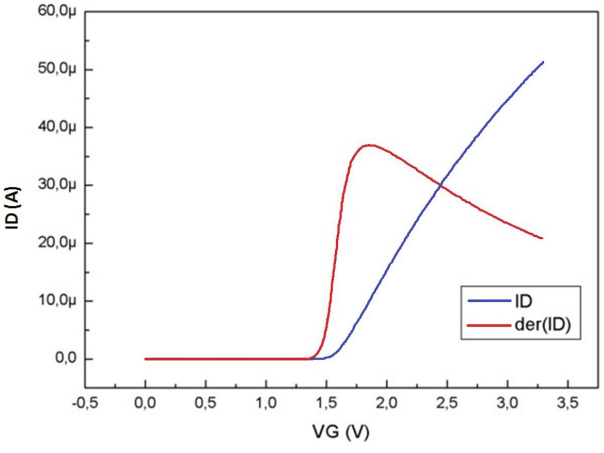

Figure 3. Typical characterization for KP and E0 extraction (long and wide transistor)

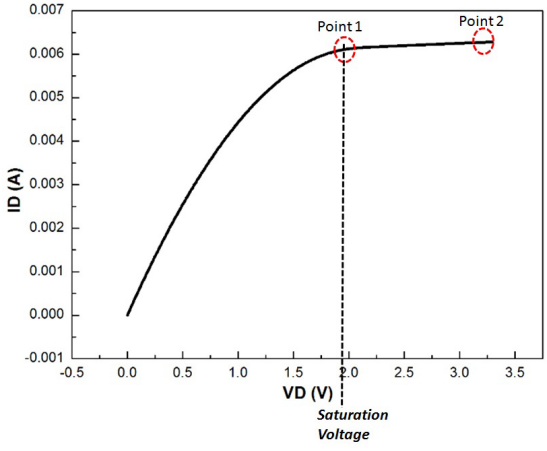

Figure 4. Typical characterization for UCRIT and LAMBDA extraction (short and wide transistor)

approximation of the *VDsat*, as demanded (circle and dash line in blue, in Fig. 5).

Then, the system of equations (9) allows calculating UCRIT with less than 5% of error; where *Vt* is the thermal voltage, *i_f* is the normalized direct current, *VDsat* corresponds to half the saturation voltage and *VP* is defined by (10) [28].

$$\begin{cases} VD_{sat} = UCRIT.L\left(\sqrt{0.25+\dfrac{Vt}{UCRIT.L}\sqrt{i\_f}}-0.5\right) \\ i\_f = \left(\log\left(1+\exp\left(\dfrac{VP-VS/Vt}{2}\right)\right)\right)^2 \end{cases} \quad (9)$$

$$\begin{cases} V_P = V_G{}' - PHI - \gamma'\left[\sqrt{V_G{}'+\left(\dfrac{\gamma'}{2}\right)^2}-\dfrac{\gamma'}{2}\right] \\ V_G{}' = V_G - V_{T0} + PHI + GAMMA.\sqrt{PHI} \end{cases} \quad (10)$$

Insofar, as the transistor presents short-channel effects, *VG'* should include the reverse short channel effect (RSCE), being replaced in (10) by [28]

$$VG' = VG - VT0 - \Delta V_{RSCE} + PHI + GAMMA\sqrt{PHI} \quad (11)$$

LAMBDA parameter can be extracted based on the same curve of Fig.4, requiring, however, the choice of a second point, "Point 2", with *VD* close to VDD (*VD* = 3.2V, in 0.35μm technology). Equation (12) allows calculating the variation of the channel length (ΔL) caused by an increase of the depletion layer [10, 28]:

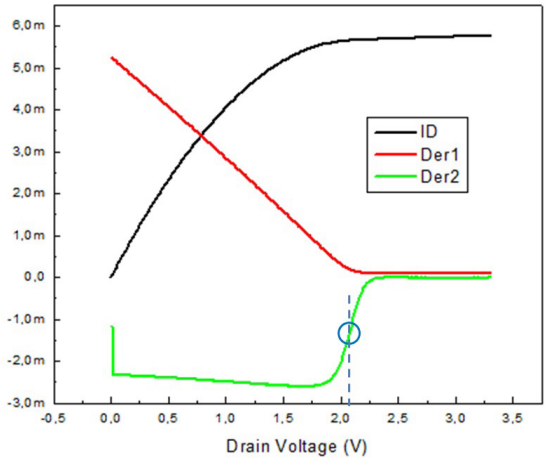

Figure 5. Second Derivative Method for extracting *VDsat* (Drain Current, in black, first derivative, in red, and second derivative, in green)

$$\Delta L = L\left(1-\frac{IDS_{sat}}{IDS}\right) \quad (12)$$

where IDS_{sat} refers to the saturation current, measured in VD_{sat} (Point 1), and *IDS* is the current measured in "Point 2". The Δ*L* value allows calculating *LAMBDA* with (13). *VDS* is the drain-source voltage, *i_f* is the normalized direct current, Δ*V* is a voltage correction variable regarding the channel modulation effect and V_{IP} is the effective saturation voltage for the MOSFET device [28].

$$\begin{cases} \Delta L = LAMBDA.\sqrt{\dfrac{\varepsilon_{Si}.\varepsilon_0}{COX}XJ}.\ln\left(1+\dfrac{VDS/2-V_{ip}}{\sqrt{\dfrac{\varepsilon_{Si}.\varepsilon_0}{COX}XJ.UCRIT}}\right) \\ V_{ip} = \sqrt{VD_{sat}^2+\Delta V^2}-\sqrt{\left(VDS/2-VD_{sat}\right)^2+\Delta V^2} \\ \Delta V = 4.V_t.\sqrt{LAMBDA.\left(\sqrt{i\_f}-\dfrac{VD_{sat}}{V_t}\right)+\dfrac{1}{64}} \end{cases} \quad (13)$$

Finally, Table 2 summarizes all procedures concerning to the proposed method. For all of them, details of the setup, polarization, region of operation, geometries of the samples and some additional remarks are presented.

III. VALIDATION OF THE METHOD

A computational tool called PExPy was developed, in PYTHON environment [26], to implement the proposed method. Embedded in PExPy, there is a simulation module called SimulPy [27] that allows the simulation of the transistors without interfaces with any other commercial tool. PExPy presents some check-points (pauses), to allow the user to choose the best values of the characterization curves for the calculus. This feature avoids eventual spurious data from noisy curves to interfere in the calculus, what could lead to a wrong set of extracted parameters. Both PExPy and SimulPy are open-source and free software, allowing further improvements in calculus and equations, if desired. PExPy is a self-contained program that comprises the full functionalities for parameter extraction issues, optimizing the time for libraries generation.

The proposed method was evaluated in two different cases: using, as data sources, the curves generated by a well-known BSIM3v3 model at room temperature; and using experimental data of AMS 0.35μm transistors, at 77K. The reason for choosing 77K is related to the fact that it is the Liquid Nitrogen Boiling temperature, used in the cooling of infrared sensors.

Table 2. Summary of the configurations for the proposed extraction method

Parameter	Setup/Polarization	Region of Operation	Transistor Geometry	Remarks
I_s	**Setup #1** VD = VDD VG > 0.7 VDD VS = 0V to VDD VB = 0V	- Strong Inversion - Saturation	- All	- Normalization Factor for Currents and Voltages - Graph: $d\left(\sqrt{I_D}\right)$ *vs.* VS - Previously presented in literature [14,23]
VT0 ***GAMMA PHI***	**Setup #2 (diode conection and a current source - IS in the Source terminal)** VD = VG = 0 to VDD IS = I_s/2 VB = 0V	- Moderate Inversion - Saturation	- Big (Long and wide)	- Graph: VP *vs.*VG - Setup and VT0 previously presented in literature [14,23]. - GAMMA and PHI extractions improved and detailed in this paper.
KP	**Setup #3** VD = 0.5V VG = 0V a VDD VS = VB = 0V	- Strong Inversion - Triode (Linear)	- Big (Long and wide)	- Graph: ID *vs.*VG - Novel approach
E0	**Setup #3** VD = 0.5V VG = 0V to VDD VS = VB = 0V	- Strong Inversion - Triode (Linear)	- Big (Long and wide)	- Graph: (derivative of ID) *vs.*VG - Novel approach
LAMBDA ***UCRIT***	**Setup #4** VD = 0V to VDD VG ≈ VDD VS = VB = 0V	- Strong Inversion - Saturation	- Short and Wide	- Graph: ID *vs.*VD - Novel approach
LETA ***WETA***	**Setup #2 (diode conection and a current source - IS in the Source terminal)** VD = VG = 0 to VDD IS = I_s/2 VB = 0V	- Moderate Inversion - Saturation	- WETA (Narrow and Long) - LETA (Wide and short)	- Graph: VP *vs.*VG - LETA and WETA extractions improved and detailed in this paper
Q0 ***LK***	**Setup #2 (diode conection and a current source - IS in the Source terminal)** VD=VG: 0 a VDD IS: I_s/2 VB: 0V	- Moderate Inversion - Saturation	- Set of Wide and Short transistors with $L_{min} < L_{eff} < 2L_{min}$	- Graph: VP *vs.*VG - Graph: VT0 *vs.* L - Novel approach

In the first case, a library (BSIM3v3 Model) from AMS 0.35μm technology generated the curves that were used as data base for the parameter extraction. Once there is no correspondence between the constitutive parameters of BSIM3v3 and EKV2.6, this approach allows us to demonstrate the efficiency of the method, without the need of characterizing a device. This option was chosen in a first approach in order to avoid experimental errors or noise, what could lead to mistakes and to wrong conclusions. The curves were generated for two different geometries of transistors (*W/L*): a long and wide transistor (25x25μm^2); and a short and wide transistor (25x0.35μm^2). After applying the proposed method, the EKV library was generated and simulated. The curves *ID* vs. *VD* and *ID* vs. *VG* were compared to the original data (from BSIM3v3 model) and the deviations between them were calculated. Figures 6, 7, 8 and 9 show the comparison between the curves generated by the BSIM3v3 model and the ones generated by our EKV model extracted library.

Analyzing Fig. 6, 7, 8 and 9, it is possible to ensure that, although based on a few numbers of parameters, EKV model was able to reproduce the behavior of the transistors in a wide range of dimensions, once the previous figures refer to channels lengths from 25μm to 0.35μm. For Fig. 6 and 7 (*ID*

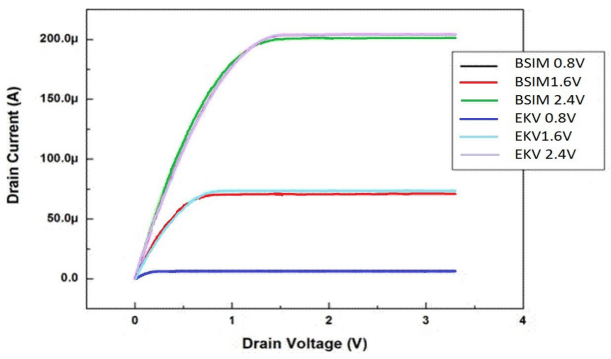

Figure 6. Comparison between the BSIM3v3 and the EKV curves for a long and wide transistor (three different *VG*).

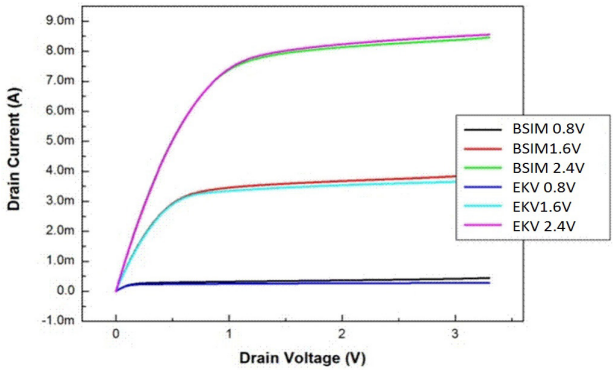

Figure 7. Comparison between the BSIM3v3 and the EKV curves for a short and wide transistor (three different *VG*).

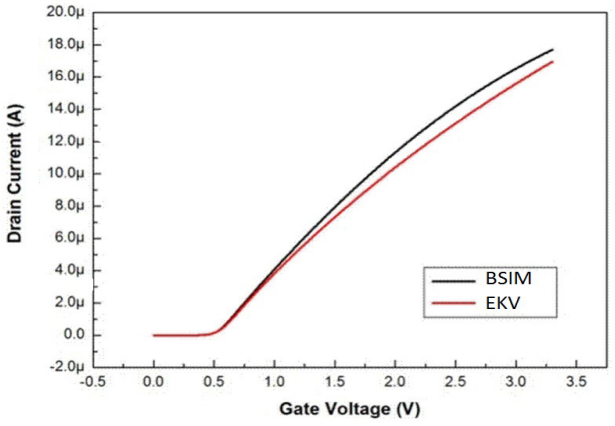

Figure 8. Comparison between the BSIM3v3 and the EKV curves for a long and wide transistor.

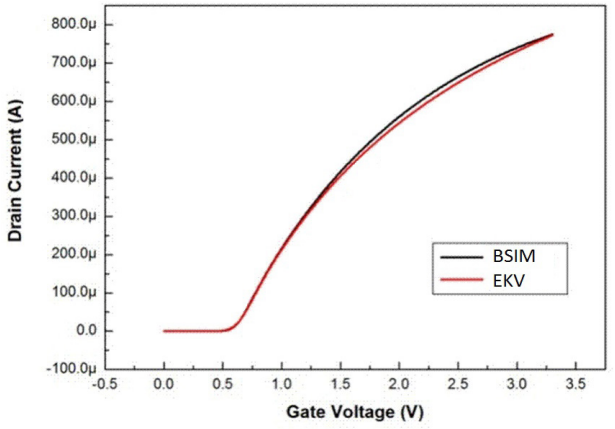

Figure 9. Comparison between the BSIM3v3 and the EKV curves for a short and wide transistor.

vs. *VD* curves) and Fig. 8 and 9 (*ID* vs. *VG* curves), the error was below 1.2% and 6%, respectively. For *ID* vs. *VG* curves the mean error value was below 2%, when considering all points of the curves. It assures the accuracy of the proposed method and of the generated library. An important detail must be highlighted: the presented results were achieved in only one step, without any kind of interaction or optimization steps, as required by other tools.

As a second validation of the method, it was applied to experimental curves of a transistor at 77K. This approach was implemented since there is no 77K library for this kind of project, becoming a challenge for the scientific community. The curves were extracted with a Keysight B-1500 – Semiconductor Parameter Analyzer for a transistor from AMS 0.35μm, with 20x2μm^2. Figures 10 and 11 show the comparison between the experimental curves and the EKV curves generated by the proposed method. A good agreement between the experimental and the EKV generated libraries/models for both curves was achieved, with mean errors below 5%.

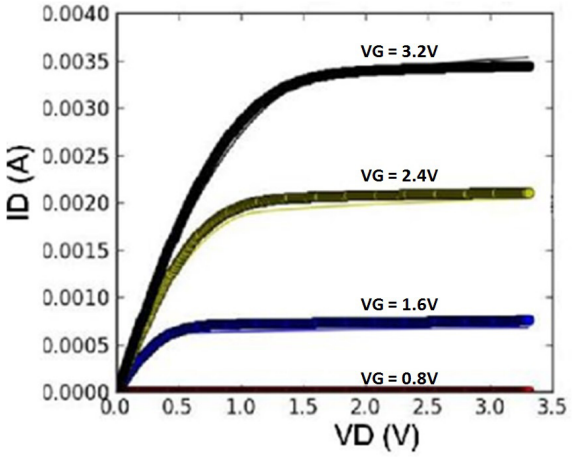

Figure 10. Comparison between the Experimental *ID*×*VD* Curves of AMS 20x2µm^2 Transistors (circles) and the ones generated from the EKV model (continuous lines), for four different Gate Voltages.

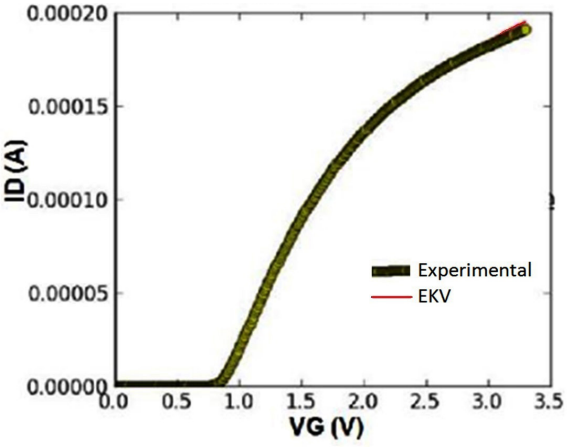

Figure 11. Comparison between the Experimental *ID*×*VG* Curves of AMS 20x2µm^2 transistors (circles) and the ones generated from the EKV model (continuous line).

IV. CONCLUDING REMARKS

This paper presented a novel MOSFET parameter extraction method. Based exclusively on EKV2.6 physical concepts, a full set of experimental arrangements and equations were proposed, in order to generate reliable and accurate simulation libraries, without the need of optimization steps.

The proposed method improves and updates the previous ones found in literature, once describes arrangements and physical equations for intrinsic DC EKV parameters, allowing the generation of MOSFET libraries, even in harsh environments, as 77K.

In the case of a full library, including short-channel effects, at least three transistors with different *W/L* should be measured. On the other hand, libraries focusing only on large devices, where short-channel effects are not representative, demand only one transistor geometry, even under harsh environment. In both cases, four setups are necessary to achieve all data base for the generation of reliable libraries.

Validations of the method were provided by the use of BSIM3v3 simulated curves, at room temperature, and by the experimental curves of an AMS 0.35μm transistor, at 77K. In both cases, it was possible to generate EKV libraries able to reproduce their behavior with low errors, without any kind of optimization (fitting) procedure. These results confirm the great potential of this method to be used in a first approach of practical projects, even in harsh environments and prospecting technologies.

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