Bio-Amplifier based on MOS bipolar Pseudo-Resistors: A New Approach using its non-linear characteristic

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ABSTRACT

This paper proposes a new and refined bio-amplifier design, which associates DC offset cancellation, adequate frequency response and buffered outputs to a significant reduction of the signal recovery time. A MOS-Bipolar pseudo-resistor integrated to the feedback network of a single-stage Operational Transconductance Amplifier and the source-follower buffers give to the new topology its main advantages. This architecture makes use of the high resistance values of these pseudo-resistors to eliminate the offset DC level input preserving the low cut-off frequency, without the need of high capacitances, thereby significantly reducing the active die area, which enables its use as a front-end pre-amplifier assembled directly on the acquisition probes. The recovery time after an input voltage transitory of high-amplitude is an important characteristic of the bio-potential amplifiers due to their very low cut-off frequency. The proposed bio-amplifier utilizes the non-linear characteristics of the pseudo-resistor in the recovery time reduction. This time was evaluated and the topology presented a significant contribution in this aspect, assuming values 90% lower when compared with the same topology using a constant resistance. The new amplifier allows voltage gain of 30dB from 0.6 Hz to 2 kHz, and Total Harmonic Distortion (THD) of 0.19% for an input signal of 10Hz. This work also provides a behavioral spice model for MOS-Bipolar pseudo-resistor, which allows an accurate simulation of the linear and nonlinear pseudo-resistor characteristics, obtained through an experimental method of indirect characterization. This method is based on the transitory response from a first order RC low pass filter. The experimental characterization method is of fundamental importance, due to the absence of appropriate SPICE models that describe with precision the pseudo-resistance behavior. The circuits were manufactured by MOSIS on 8HP SiGe BiCmos Global Foundries 0.13µm technology.

Index Terms: Bio-potential amplifier, MOS bipolar pseudo-resistor, Micro-power analog circuits.

I. INTRODUCTION

Bio-potential measurements, used to assist medical diagnoses, are obtained by non-invasive procedures with electrodes placed on the skin surface. Therefore, the bioelectric signal acquisition has been a challenge to electronic designers [1], due to the low-level electric signals acquired by the electrode transducers, in the order of millivolts or less. This low-level signal still has associated an intrinsic DC offset, created by the electrode-electrolyte association, and other undesired transitory signals. Such signals are frequently greater than the signal to be measured and, without the adequate attenuation, easily saturate the input-stage amplifiers. The applicable ANSI standard on medical equipment [2] establishes that the amplifiers must operate in the presence of up to ±300 mV offset DC added to the input signal, in addition to: preserving the bio-signal integrity, input impedance above 10 MΩ [2], suitable gain, limited bandwidth in order to improve the signal-to-noise ratio, low intrinsic noise, offset DC voltage cancellation and low harmonic distortion.

Some of the bio-amplifier challenges can be addressed through new circuit topologies, which can also allow the implementation in a single integrated circuit that could be placed directly in the electrode. It is worth noting that some improvement in the signal-to-noise ratio can be obtained simply from elimination of the cables and connections between the electrodes and the input amplifier. Due to the very low frequency of most of the bio-signals, the elimination of the DC and DC steps in the circuits are not easily achieved. In discrete implementations, DC offset cancellation may be obtained by decoupling capacitors or by topology amplifier implementation. In both solutions, large time constants are required, implying in large capacitors and/or large resistors, which cannot be implemented in CMOS standard technologies. Solutions to this problem include nonlinear devices, like the MOS-Bipolar "pseudo-resistor" [3-11], which can reach higher resistance values ($>10^{13}\,\Omega$) for low-level signals and lower resistance for high-level signals [6]. Due to the high resistance value reached by such devices, small capacitors may be implemented on the integrated circuit, leading

to acceptable footprints for the integrated-circuit design. However, the pseudo-resistor is a MOS transistor connected in a special configuration that biases the device in a quite unusual operational condition, and the available numerical models do not provide accurate outputs, when compared to experimental results. Moreover, the high resistance values of these devices cannot be measured directly [3].

Another important characteristic of the bio-potential amplifiers is the output recovery time after an input transitory voltage step [2, 6]. Once the frequency cut-off of these circuits is very low, the long transient recovery time causes the bio-amplifier saturation, which can last until hundreds of seconds [1,4,9], what could be unacceptable for many applications.

In this work, a new bio-potential amplifier topology, which makes use of MOS-bipolar pseudo-resistor, is proposed. The new design presents DC input cancellation without coupling capacitances, making it appropriate to be used as a front-end pre-amplifier, to be assembled directly on the acquisition electrodes. Beyond the offset DC cancellation, this new design utilizes the non-linear characteristics of the pseudo-resistor for the reduction of the recovery time and presents outputs for connection to differential inputs.

Additionally, this work presents an experimental characterization method for pseudo-resistors, and the procedure for the inclusion of a reliable model into SPICE simulation.

The paper is organized as follows. In Section II, the new bio-potential amplifier topology is proposed with its modeling. An experimental characterization method and its inclusion into SPICE simulation is discussed in Section III. The conclusions are given in Section IV.

II. BIO-AMPLIFIER TOPOLOGY

A simplified schematic diagram of the proposed topology is shown in Fig 1. It is composed of a source follower buffers associated to a single stage Operational Transconductance Amplifier (OTA). The OTA is implemented with composite-transistor structures [12] to increase the OTA output impedance. Due to the low lower cutoff frequency of the bio amplifier, a high time constant is needed. This architecture uses the higher resistance values MOS-bipolar pseudo-resistor, to allow reduction of the capacitor values on the RC feedback network, reducing also the active die area. The low impedance (around 1600 Ω) between output buffers minimizes the path effects (cables and electrical connections) preserving the shape and signal integrity. The absence of active devices in the feedback network makes this solution very stable without the need of compensations.

Bio-Amplifier Modeling

An analytical model has been developed from the proposed topology. It allows the gain estimation, and performance evaluation, including frequency response. The basic block diagram is shown in Fig. 2. It does not take into account the OTA high frequency effects, once the upper-frequency cut-off is about 2 KHz.

The voltage gain ($A_{V(j\omega)}$) in the analytical model, is given by equation (1).

$$Av_{(j\omega)} = \frac{V_{o(j\omega)}}{V_{i(j\omega)}} = G_{m1} \cdot \frac{Rds_1}{1+j\omega \cdot Rds_1 \cdot C_L} \qquad (1)$$

Where, G_{m1} is the OTA transconductance, C_L the load capacitance and Rds_1 the OTA output impedance. The passive feedback network ($H_{(j\omega)}$), represented in the Fig. 3, include the pseudo-resistor and the capacitor C. The pseudo-resistor is modeled only for small signals through linear resistor R_p and the capacitance C_p equalizes the frequency response curve.

The feedback network function, $H_{(j\omega)} = A_{(j\omega)}/Vo_{(j\omega)}$ can be represented by (2).

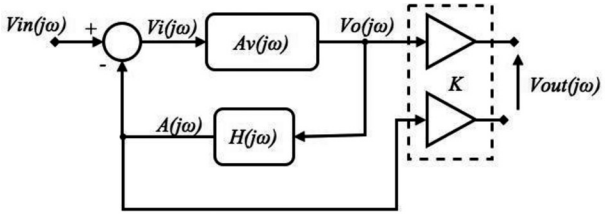

Figure 2. Pre-amplifier analytical model.

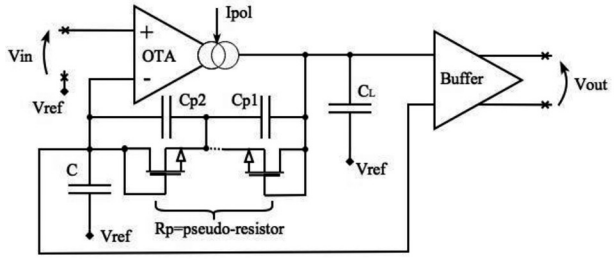

Figure 1. Functional block diagram of the Bio-amplifier proposed.

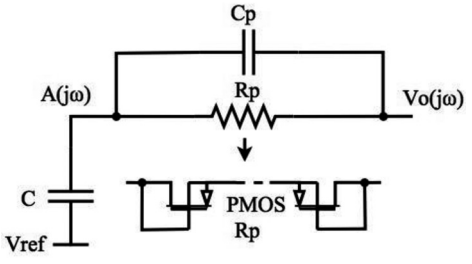

Figure 3. Passive feedback network model H(jω).

$$H_{(j\omega)} = \frac{\frac{1}{j\omega C}}{\left(\frac{1}{j\omega C_p}//R_p\right)+\frac{1}{j\omega C}} \quad (2)$$

The constant "K" represents the class AB output buffers gain using source follower, and it is lower than unity [13]. Equations (3), (4) and (5) show the complete bio-amplifier transfer function.

$$G_{(j\omega)} = \frac{Vo_{(j\omega)}}{Vin_{(j\omega)}} = \frac{Av_{(j\omega)}}{1+Av_{(j\omega)}\cdot H_{(j\omega)}} \quad (3)$$

$$A_{(j\omega)} = \frac{Av_{(j\omega)}\cdot H_{(j\omega)}}{1+Av_{(j\omega)}\cdot H_{(j\omega)}} \quad (4)$$

$$G_{total(j\omega)} = \frac{Vout_{(j\omega)}}{Vin_{(j\omega)}} = K\cdot\left[G_{(j\omega)} - A_{(j\omega)}\right] \quad (5)$$

It is worth noting that Rp is assumed to be constant in eq. 2- 5.

Bio-Amplifier Circuit Design

The design was based on inversion coefficient methodology (IC) for analog circuit designs [14, 15]. It uses operation regions of the MOS transistors, but with focus on main parameters for a bio-amplifier good design. Since the lower frequency cut-off is in mHz range, the flicker noise and non-linearity are very relevant aspects, so the design must minimize these undesirable effects. The schematic diagram of the proposed bio-amplifier is shown in Fig. 4. In this schematic the one-stage OTA, the source follower buffer [16] and the passive feedback network with the MOS-Bipolar pseudo-resistor are included. For low flicker noise, high transconductance and low DC mismatches, the amplifier transistors (M1, M2) must be designed to operate in weak inversion region, with very low drain current and very large dimensions [14], both transistors must be sub-threshold biased. Once we need very good linearity, all bias points and current mirrors were designed to operate in strong inversion region, with high Early voltage and low output current in the OTA, exception for M5c and M6c transistors, which operate in weak inversion region, due to bias of the composite transistors. High output impedance (R_{DS1}) was obtained with the use of composite transistors [11] (M5, M5c, M6, M6c, M7, M7c, M8, M8c), thereby reducing higher cutoff frequency (~2 KHz), for capacitive loads up to 10 pF.

The negative feedback minimizes the residual DC on the outputs, caused by implementation mismatches in the manufacturing process. The feedback network, composed by Rp and C, is connected between the output (Vo) and the inverting input (Vi-). The electrode probe is connected between the non-inverting input (Vi+) and the reference voltage (Vref), where the reference voltage establishes the suitable OTA's biasing. This circuit presents unitary gain for bio-signal DC levels, and it tolerates up to ±0.3 V_{DC} intrinsic added to the bio-signal, without decoupling capacitors. The range of input bio-signal is from 10 μVpeak to 5 mVpeak.

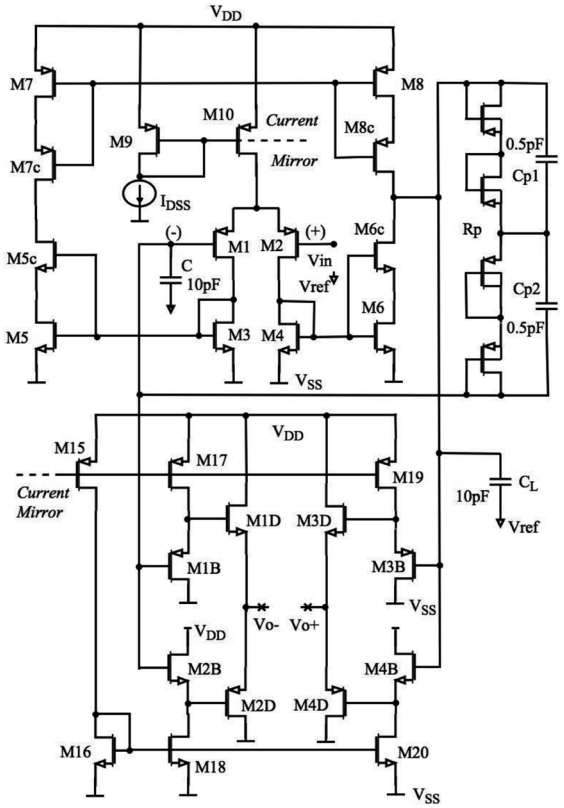

Figure 4. Detailed schematic of the Bio-amplifier proposed.

DC cancelation is achieved by connecting the circuit outputs (V_{o+} and V_{o-}, figure 4) to a differential input of the acquisition system, because V_{o+} contains both the DC and the AC components, while V_{o-} contains just the DC component. The residual DC expected by mismatching on the manufacturing process, should be minimal because its gain is below unity.

For the recovery time reduction, the architecture uses the pseudo-resistor resistance non-linear behavior with the voltage applied between its terminals. When the transient DC occurs in the signal input, the OTA output goes to saturation due to the increase of the differential input voltage, increasing the voltage between the pseudo resistor terminals. This fact, reduce its resistance and time constant RpC. The capacitor charge reduces the differential input voltage pulling out the OTA from saturation, and reducing the voltage between the pseudo-resistor terminals. This will increase the resistance again, so the output signal recovery time is reduced.

The driver's transistors (M1D, M3D, M2D and M4D) are designed to present high Gm values and thereby to obtain low output impedance, i.e. meaning high dimensions. Equation 6 gives the Buffer output impedance.

$$Zout = [(Gm_{1D} + Gm_{2D})//(Gm_{3D} + Gm_{4D})]^{-1} \quad (6)$$

The OTA Transconductance (Gm_1) was estimated using the equation 1 and the output impedance by equation 7:

$$R_{DS1}=1/((G_{DS}M8//G_{DS}M8c)+(G_{DS}M6//G_{DS}M6c)) \quad (7)$$

The Table 1 presents the transistors dimensions.

The new bio-potential amplifier design was implemented for 8HP 0.13 μm BiCMOS technology [17] and fabricated by MEP (Mosis Educational Program) [18], according to layout of Fig 5.

Table 1. MOS Transistors geometry and operating regions

DEVICES GEOMETRY AND OPERATING INVERSION REGION					
	OTA			BUFFER	
Devices	W/L (µm)	Operating Region	Devices	W/L (µm)	Operating Region
$M_{1,2}$	750.00/3.00	Weak	M_{15}	2.00/4.00	Strong
$M_{3,4}$	0.56/3.00	Strong	$M_{16,18,20}$	0.60/3.00	Strong
$M_{5,6}$	0.39/3.00	Strong	$M_{17,19}$	2.00/3.00	Strong
$M_{5C,6C}$	15.60/3.00	Weak	$M_{1B,3B}$	1.20/3.00	Strong
$M_{7,8}$	0.36/36.00	Strong	$M_{2B,4B}$	0.80/3.00	Strong
$M_{7C,8C}$	0.90/72.00	Strong	$M_{1D,3D}$	180.00/3.00	Strong
$M_{9,10}$	1.00/9.00	Strong	$M_{2D,4D}$	540.00/3.00	Strong

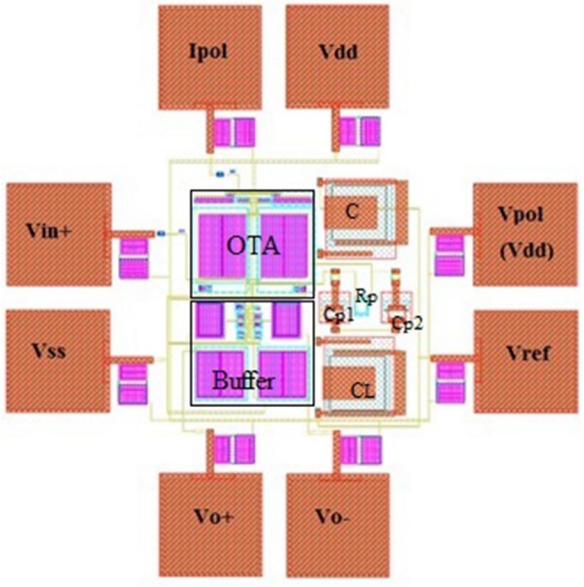

Figure 5. New bio-potential amplifiers design.

Performance Evaluation

The bio-amplifier performance can be either obtained by simulation or by experimental means. Fig. 6 presents the Bio-amplifier frequency response. These curves show the difference between the proposed experimental Rp model and the PMOS model BSIM3V3.1 [19]. This difference reaches almost two orders of magnitude in the low-frequency cut-off. The proposed circuit presented limited bandwidth in 2 KHz, THD of 0.19% and Total Input Noise 38.5 µV, according to Table 2.

The strategy for this amplifier design, using the Rp non-linearity to reduce the recovery time, after a transitory DC, presented on [6], was confirmed. Fig. 7 shows the transitory response for a 10 Hz input signal of 3 mV_{pp}, after a 300 mV_{DC} step, where it is possible to observe offset DC voltage cancellation. The circuit recovers the linear operation after about 3 seconds, a very

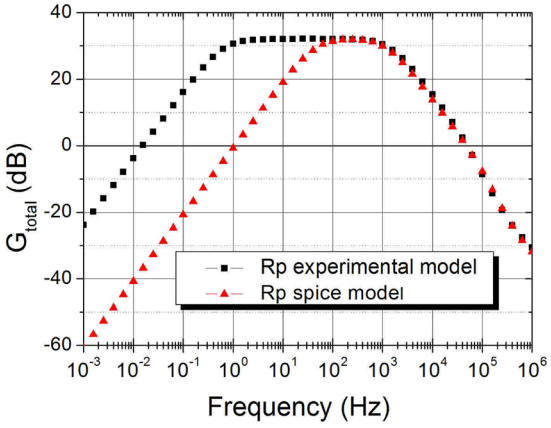

Figure 6. Bio-amplifier frequency response.

Table 2. Summary of electrical performance of the proposed Bio-Amplifier.

Summary of Electrical Performance	
V_{DD}	2.5 V
V_{ref}	1.0 V
I_{DSS}	0.5 µA
Gain (Av)	30 dB
DC rejection	< -30 dB
DC cancelation	±300 mV
Lowest frequency cut-off	300 mHz
Upper frequency cut-off	2 KHz
Phase Margin	90^0
THD	0.19%
Total Input Noise	38.5 µV
V_{out} (rail to rail)	±250 mV
Z_{out}	1600 Ω

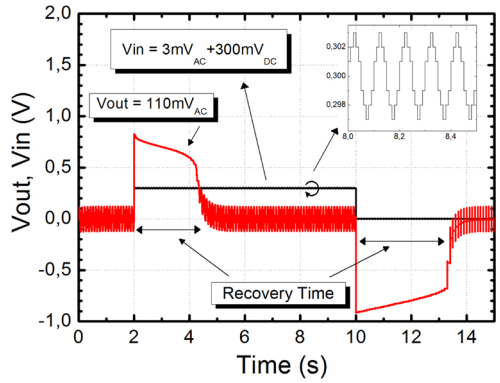

Figure 7. Bio-amplifier recovery response after the offset DC.

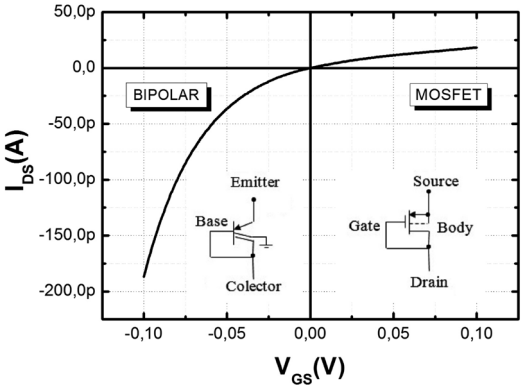

Figure 8. Pseudo-resistor behavior for positive or negative V_{GS} values.

short time for an amplifier with such a low frequency response (200 mHz of lower cut-off frequency).

Finally, Table 2 summarized the simulations performance of the bio-amplifier using the pseudo-resistor polynomial model, obtained by experimental data.

III. MOS-BIPOLAR PSEUDO-RESISTOR EXPERIMENTAL MODELING

The MOS-bipolar pseudo-resistor was introduced by T. Delbruck [20] as an "adaptive element". Delbruck explained that its effective resistance is huge for small signals and small for large signals. The pseudo-resistor uses MOS transistors body connected to the source and the gate connected to the drain, acting like a pMOS diode for positive V_{GS} and bipolar diode for negative V_{GS}. Fig. 8 exhibits the PMOS pseudo-resistor's behavior as a function of voltage bias.

Considering the back-to-back connection, a linear trend can be observed in the interval between ±100 mV [6]. References [4-6] use the pseudo-resistor like a high-value linear resistor, and limit the analysis to voltage drops (between terminals of pseudo-resistors) bellow 100 mV.

This work proposes one characterization method based in experimental measurements on the transitory time response from a low-pass RC filter. A low-pass RC filter and two source follower amplifiers compose the circuit, as shown in Fig.9a. The source followers provide functional isolation, avoiding direct connection of the high impedance circuit to the pads and external environment. The RC filter is composed by two back-to-back connected pseudo-resistors, a constructed capacitor (C), and the capacitance of M2 gate. Calibre™ PEX [21], adopting PSP103.1 SPICE model, can precisely extract this last capacitance from the layout. Fig. 9b shows the layout implemented using Global Foundries 8HP 0.13 µm BiCMOS technology and fabricated.

The measurement strategy consists in applying a step voltage (V_{step}) summed to the bias input voltage (V_{bias}) and evaluates the resistance by observing the capacitor charging function, through the output voltage (V_{O_Rp}). The expected output voltage (V_{O_Rp}), due R_pC time constant, can be expressed by equation (8).

$$V_{O\_Rp} = V_{step}\left(1 - e^{-\left(\frac{t}{RpC}\right)}\right) + V_{bias} \quad (8)$$

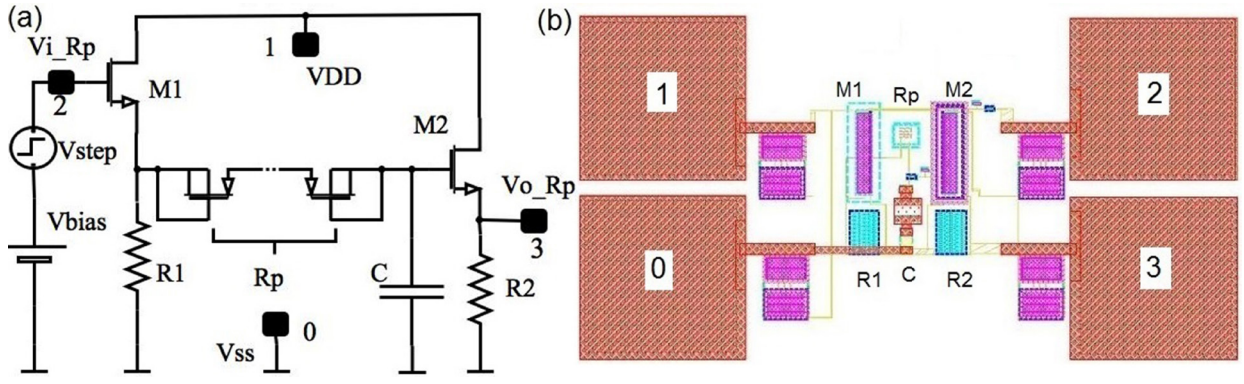

Figure 9. (a) Pseudo-resistor evaluation circuit, (b) Implemented layout.

Fig. 10 shows experimental curves of the output voltage dynamic behavior (V_{O_RP}) and the exponential fit with equation (8) to verify the I-V linearity.

The pseudo resistor implemented is composed by 4 transistors, connected in 2 back-to-back, and C=660 fF that was extracted by Calibre™ PEX [20]. For this analysis the hypothesis of ohmic resistance constant region in the interval between ±200 mV is confirmed. The curve fitted the experimental data with equation (8), and has presented Chi-square/degrees of freedom ratio of 8.75x10-8 and coefficient of determination of 0.99992. This confirms the high linearity of the I-V behavior of the pseudo-resistor for low bias. The resistance calculation has to be carried out using equation (9).

The values out the range of ±200 mV, that means non-linear region, were obtained using small intervals timing (Δt). For each interval (Δt), the resistance was assumed constant and can be calculated using the same equation 9.

$$Rp_i = \frac{\Delta t}{C \cdot \ln\left(\frac{V_{step}-\left(Vc_{i(t)}\right)}{V_{step}-\left(Vc_{i+1(t)}\right)}\right)} \; ; \text{ for I} = (0,1,2..n\text{ -}1) \qquad (9)$$

Where Vc_i is the output voltage at the beginning of the interval, and Vc_{i+1} is the voltage at the end, as represented in Fig. 11, which shows the output voltage dynamic behavior (V_{O_Rp}) of the circuit evaluation.

This evaluation method was applied to the characterization of several pseudo-resistor associations, with 1x, 2x and 3x back-to-back transistor circuits, and with different channel widths (W) and lengths (L). The pseudo resistance values obtained by SPICE simulations (BSIM3V3.1 or PSP103.1 models) did not reach the same magnitude of the experimental values. The pseudo-resistance values extracted experimentally and by SPICE simulations are exhibited on table 3.

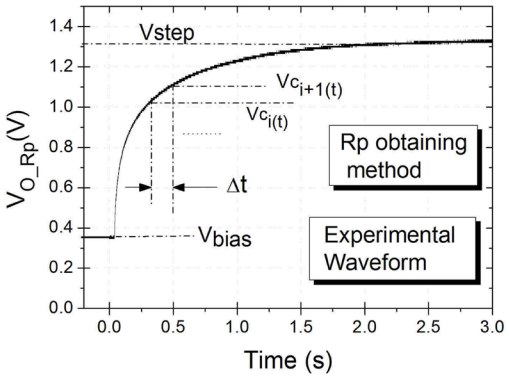

Figure 11. The experimental measurement of the output voltage (Vo), with the representation of the range used.

Table 3. Experimental pseudo-resistance values with geometry variation.

Back to back Transistors	W (µm)	L (µm)	Rp (TΩ) Measurement	Rp (GΩ) Simulation
1	0.36	0.24	0.56	13.30
2	0.36	0.24	1.30	25.80
3	0.36	0.24	2.41	38.32
1	0.72	0.48	0.27	3.50
2	0.72	0.48	0.60	6.61
3	0.72	0.48	1.08	9.53
1	1.08	0.72	0.19	2.00
2	1.08	0.72	0.42	3.55
3	1.08	0.72	0.61	5.20

Fig.12 presents the pseudo-resistance values as a function of the pseudo-resistor voltage. The pseudo-resistance values were calculated from equation 9, with the application of the proposed method in the experimental results and SPICE simulations, and compared with the Rp proposed polynomial model in the equation 10.

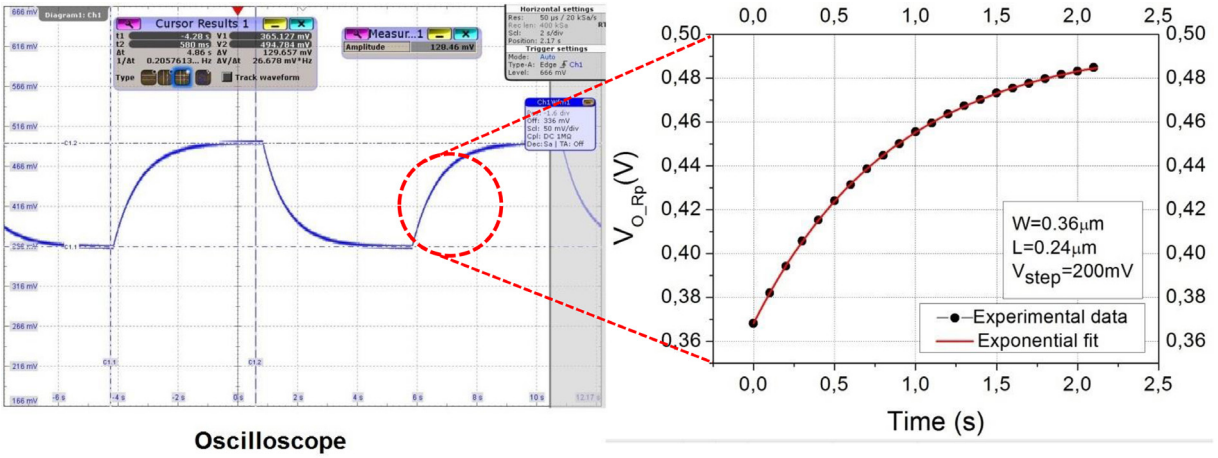

Figure 10. The experimental measurement of the output voltage dynamic behavior and exponential fit with the equation (8).

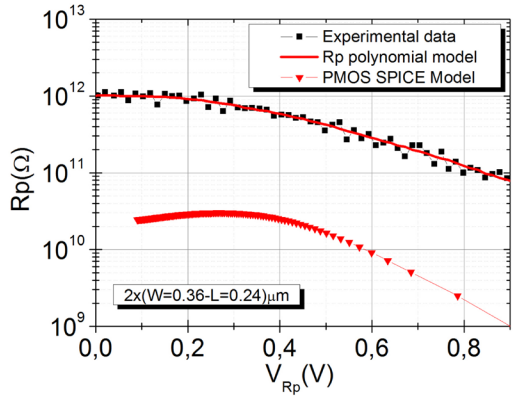

Figure 12. Pseudo-resistance values as a function of the V_{Rp}, of the experimental measures, SPICE simulations and the Rp polynomial model.

The pseudo-resistance increases as the voltage between its terminals is reduced, but close to 200 mV reaches a maximum constant value, as shown in Fig.12. The Spice simulation presents maximums from 40 GΩ to 200 GΩ and the experimental measurements, from 50 GΩ up to 1 TΩ. It suggests that the Spice model does not accurately represent the pseudo-resistor behavior in this technology [22]. To solve this problem of the SPICE simulation in the bio-amplifier, this work proposes a polynomial model that represents the pseudo-resistor experimental behavior as a function of the applied voltage (R_p/V_{Rp}). In the 8ª order polynomial curve fitted was obtained a coefficient of determination of 0.998, standard deviation of 0.00579 for number of points = 59. The equation (10) is the Rp polynomial model included in the SPICE file to run on the Eldo™ model BSIM3V3.1 [19] to take the place of MOS pseudo-resistor.

$$Rp = A_0 + \sum_{j=1}^{8} A_j \times V_{RP}^{j} \qquad (10)$$

IV. CONCLUSIONS

This work presented a new bio-amplifier topology that gathers the DC offset cancellation when connecting to differential inputs of data acquisition systems and significant reduction of the output signal recovery time. The DC offset cancellation was achieved by the use of MOS-Bipolar pseudo-resistor in the feedback network of the single stage Operational Transconductance Amplifier. This strategy allowed a significant reduction of the active die area, due to absence of decoupling capacitances. The recovery time reduction after an offset DC voltage step on the signal input was obtained by the non-linear characteristics of the pseudo-resistor. This time was evaluated and this topology presented 90% reduction when compared with the same topology without the use of the pseudo-resistor. Still, in this paper a new pseudo-resistor characterization method based in experimental measurements was proposed. The method can be applied to any MOS technology project using SPICE model for the MOS-bipolar pseudo-resistor. It allowed an accurate simulation of the pseudo-resistance behavior in any operation range and was validated through bio-amplifiers performance evaluation.

ACKNOWLEDGMENTS:

The authors would like to thank to MOSIS Educational Program (MEP) and the financial support provided by Brazilian research agency CNPq.

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