Origin of the Low-Frequency Noise in the Asymmetric Self-Cascode Structure Composed by Fully Depleted SOI nMOSFETs

Rafael Assalti[1], Rodrigo Trevisoli Doria[1], Denis Flandre[2] and Michelly de Souza[1]

[1] Department of Electrical Engineering, Centro Universitário FEI, São Bernardo do Campo, Brazil
[2] Department of Electrical Engineering (ELEN), ICTEAM Institute, Université catholique de Louvain, Louvain-la-Neuve, Belgium
rafael_22@fei.edu.br

Abstract—**In this paper the origin of low-frequency noise in the Asymmetric Self-Cascode (A-SC) structure composed by Fully Depleted SOI nMOSFETs is investigated through experimental results. It is shown that the predominant noise source of the A-SC structure is linked to carrier number fluctuations, being governed by the noise generated in the transistor near the source. Larger channel doping concentrations degrade the quality of the $Si\text{-}SiO_2$ interface and the gate oxide, which causes an increase of the normalized drain current noise spectral density, just as the reduction of the gate voltage overdrive, since there are few carriers in the channel. The A-SC structures have showed higher noise compared with single transistors. In saturation regime, the increase of the gate voltage overdrive has incremented the corner frequency, shifting the g-r noise to higher frequencies. Besides that, the normalized noise has been significantly increased when compared with the linear regime due to the rise of the drain current noise spectral density.**

Index Terms—Asymmetric Self-Cascode, Low-Frequency Noise, FD SOI nMOSFET, Trap Density.

I. Introduction

Silicon-on-Insulator (SOI) technology is characterized by the presence of a buried oxide layer between the active silicon film and the substrate. This feature allows for an intrinsic dielectric insulation between the transistors and the substrate, preventing most of the parasitic effects observed in the bulk technology [1]. When the body is fully depleted (FD), the advantages become more prominent such as lower subthreshold swing [2], increase on the carrier mobility [3] and lower short-channel effects [4]. These benefits strongly impact on the analog circuits, reducing the parasitic capacitances, promoting an increase of transconductance and also transconductance to drain current ratio (g_m/I_D) [5]. However, FD SOI transistors present reduced breakdown voltage in comparison with bulk MOSFETs, which is related to the activation of parasitic bipolar transistor inherent to the MOS structure due to the floating-body of SOI transistors [6].

The self-cascode SOI MOSFET configuration presented in Fig. 1(top), composed by two transistors in series association with short-circuited gates, is a widely recognized way of improving the analog characteristics of single MOS transistors [7]. Recently, the Asymmetric Self-Cascode (A-SC) structure, shown in Fig. 1(bottom), has been proposed, improving even more the analog parameters and minimizing the floating-body effects triggered by impact ionization of carriers. This structure is also composed by two transistors associated in series with shortened gates operating as a single device [8]. In Fig. 1(bottom), L_S and L_D correspond to the channel lengths of the individual transistors near the source and the drain, respectively. The total channel length (L) of the A-SC structure is equal to $L_S + L_D$. The transistor near the source (M_S) presents larger channel doping concentration, defining the threshold voltage (V_{TH}) of the A-SC structure, whereas the transistor near the drain (M_D) decreases the peak electric field at the channel/drain junction and, hence the impact ionization effect. Due to the reduced channel doping concentration, the M_D transistor reaches the inversion before the M_S transistor. Therefore, for gate voltages close to V_{TH} of the A-SC structure, the M_D transistor behaves as a drain extension, reducing the effective channel length to only L_S [8], incrementing I_D and g_m. Besides the minimization of impact ionization effects which increments the breakdown voltage, the asymmetric self-cascode structure promotes an improvement on the output characteristics in comparison with the uniformly doped transistor of same L, reducing the output conductance, becoming especially suitable for analog applications [8, 9, 10].

The A-SC structure has been successfully implemented in basic analog blocks, such as current mirrors (better mirroring precision), buffers (gain close to the unity) and common-source amplifiers (larger intrinsic voltage gain) [11]. In [12], the A-SC structure has exhibited higher intrinsic voltage gain compared with the single transistor of same L at liquid helium temperature. The asymmetric self-cascode has also been implemented with junctionless nanowire transistor (without PN junctions), incrementing the intrinsic voltage gain [13].

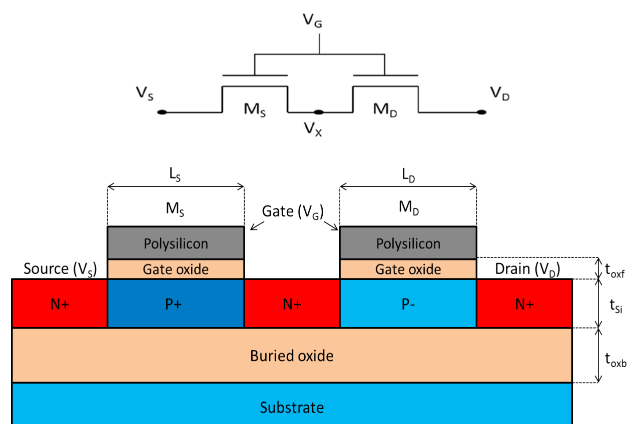

Fig.1 Schematic of the Asymmetric Self-Cascode structure composed by FD SOI nMOSFETs.

An important parameter for analog applications is the Low-Frequency Noise (LFN). The excess of noise above the known thermal and shot noises that arise at low frequencies is called low-frequency noise. This parameter defines the minimum limit above which an input signal can be detected, and significantly impacts the signal to noise ratio [14]. Besides that, the low-frequency noise is a nondestructive tool to characterize the trap density, since the carriers are confined to a narrow superficial channel under the gate oxide, being sensitive to traps located at the interfaces, in the silicon depletion layer and in the gate oxide [15].

The low-frequency noise is normally dominated by $1/f^{\gamma}$ noise (where f is the frequency), also named flicker noise, which results in random variations in the drain current caused by two physical mechanisms: fluctuations in the number of carriers [16] or/and in the mobility [17], which affect the device electrical conductivity. In case of flicker noise dominated by carrier number fluctuations, the frequency exponent (γ) varies from 0.7 to 1.3 [14]. If $\gamma = 1$ the trap density is uniform in the gate oxide depth, if $\gamma < 1$ the trap density is larger close to the Si-SiO_2 interface and if $\gamma > 1$ the trap density is higher in the gate oxide. On the other hand, if the flicker noise is dominated by mobility fluctuations, the frequency exponent is always equal to one [14].

At specific conditions, the generation-recombination noise (g-r) can become the dominant noise component, which is linked to the capture and emission of carriers between the channel and the traps, exhibiting a Lorentzian spectrum (plateau followed by $1/f^2$ roll-off). The g-r noise is significant when the Fermi level is close to the trap energy level since the carrier capture and emission time constants are almost equal [14].

This paper aims at analyzing the LFN in the asymmetric self-cascode composed by FD SOI nMOSFETs for different gate and drain voltages, and channel doping concentrations in the transistors near the source and the drain of the A-SC structure, comparing with single devices. The effective trap density (N_T) and its effective depth in the gate dielectric (x) are also extracted. In Section II, a brief description of the measurement setup and the device characteristics are presented. Section III and IV exhibit the DC and the LFN analysis of the A-SC structures, respectively. Finally, Section V presents the main conclusions of this work.

II. Device Characteristics and Measurement Setup

The studied transistors along the work have been fabricated in a 150nm FD SOI technology from OKI Semiconductors, presenting gate oxide thickness (t_{oxf}) of 2.5nm, silicon film thickness (t_{Si}) of 40nm and buried oxide thickness (t_{oxb}) of 145nm. The single transistors present channel width (W) of 10µm and channel length of 150nm. Three different channel doping concentrations have been evaluated, leading to threshold voltages of 0.02, 0.33 and 0.57V. The A-SC structures have been formed by the series association of the previously mentioned L = 150nm devices, maintaining the transistor with higher threshold voltage close to the source.

The experimental measurements were obtained with the Agilent 4156C Semiconductor Parameter Analyzer. To extract the low-frequency noise, the drain voltage was amplified by the SR560 low-noise amplifier. In sequence, this signal was inserted into an Agilent 4395 spectrum analyzer.

III. DC Analysis

Firstly, a DC study is performed as a way to evaluate the effects of different channel doping concentrations and the implementation of the asymmetric self-cascode on the input characteristics of this technology. Fig. 2 presents the drain current as a function of the gate voltage for single devices and A-SC structures varying the channel doping concentration. For single transistors, it is well known that the increment of the channel doping concentration increases V_{TH}. The same characteristic is obtained for the A-SC structures, since the larger the channel doping concentration of the M_S transistor, the higher the threshold voltage.

Also, we verify a reduction in the drain current level compared with the single transistors of same V_{TH}, which is related to the presence of M_D transistor in series, enlarging the resistance for the current flow. This can be better visualized by Fig. 3 by presenting the transconductance as a function of the gate voltage overdrive ($V_{GT} = V_{GS} - V_{TH}$). Although the A-SC structures present effective channel length similar to L_S around the threshold voltage, there is a reduction of g_m linked to the M_D transistor. As V_{GT} increases, the effective channel length tends to $L_S + L_D$ due to the closer electron concentrations in the M_S and M_D transistors [8], and the transconductance of the A-SC structure tends to half g_m of single transistors. Besides that, the larger the channel doping concentration of the M_S and M_D transistors, the lower g_m due to the reduction of carrier mobility.

IV. Low-Frequency Noise Analysis

In this section, the low-frequency noise will be assessed for single transistors and A-SC structures operating in linear (V_{DS} = 50mV) and saturation (V_{DS} = 0.7V) regimes. Also, the effective trap density will be extracted as well as its distribution along the gate oxide depth.

A. LFN – linear regime

Fig. 4 presents the drain voltage noise spectral density (S_{Vd}) as a function of the frequency for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) structure varying the gate voltage overdrive. The noise inherent of the measurement system (base-noise) is also indicated. One can see that the larger the gate voltage overdrive, the lower the drain voltage noise spectral density, incrementing the signal to noise ratio. Also, the drain voltage noise tends to the base-noise, whose spectrum is almost constant in all range of frequencies, becoming practically a white noise.

Based on simple equations, it is possible to convert S_{Vd} in drain current noise spectral density (S_{Id}), as presented in Fig.

5 for the same A-SC structure analyzed in Fig. 4. The 1/f and $1/f^2$ lines are also shown in order to identify the trends of the noise curves. We note that the A-SC structure can present either $1/f^{\gamma}$ or $1/f^2$ behavior depending on V_{GT} and frequency range. For $V_{GT} \geq 0V$, only 1/f noise component is observed. At $V_{GT} = -100mV$ and higher frequencies, $1/f^2$ noise is noticed, which is related to the presence of Lorentzians.

The lowest gate voltage overdrive presents the minimum drain current noise spectral density in the entire frequency spectrum, which is related to the operation in subthreshold regime, where the free carrier concentration in the channel is reduced. When $V_{GT} = 0V$, the formation of a superficial inversion layer increments S_{Id}. However, for $V_{GT} > 0V$, the overall noise does not increase, indicating that the carrier number fluctuations are the 1/f noise origin [14].

The thermal noise limit of the transistors ($S_{Id,thermal}$) can be obtained through (1), where k is the Boltzmann constant, T is the absolute temperature, which is equal to 300K, and γ' is a constant equals 1/2 and 2/3 in weak and strong inversions, respectively [18], and is different from the frequency exponent (γ) of noise. The thermal noise varies from $5\times10^{-25}A^2/Hz$ to $6\times10^{-24}A^2/Hz$ when the gate voltage overdrive is changed from –100mV to 200mV. As expected, the thermal noise is several orders of magnitude lower than the obtained 1/f and $1/f^2$ noise components.

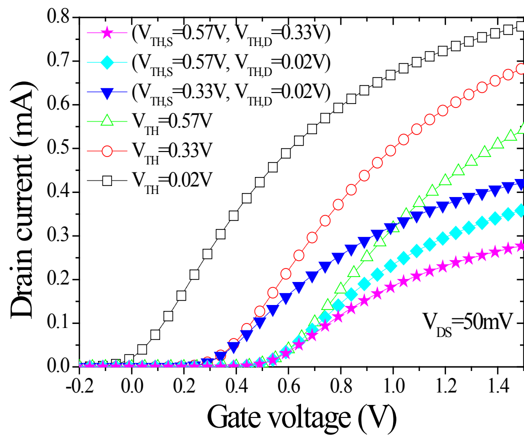

Fig.2 Drain current as a function of the gate voltage for single devices (open symbols) and A-SC structures (closed symbols) extracted at V_{DS} = 50mV.

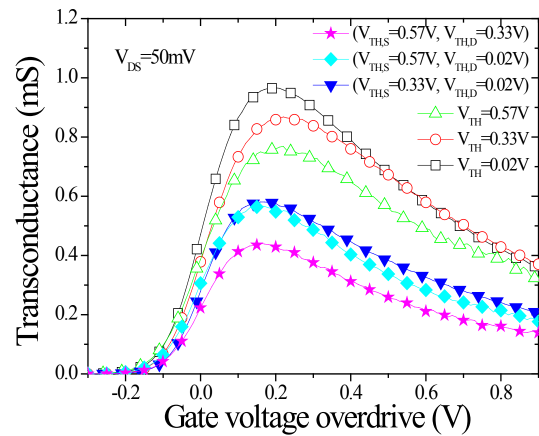

Fig.3 Transconductance as a function of the gate voltage overdrive for single devices (open symbols) and A-SC structures (closed symbols) extracted at V_{DS} = 50mV.

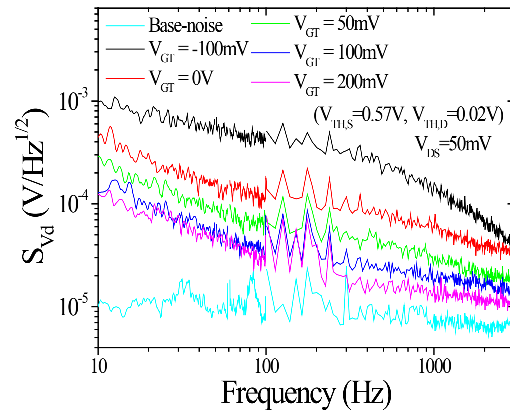

Fig.4 Drain voltage noise spectral density as a function of the frequency for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) structure varying V_{GT}.

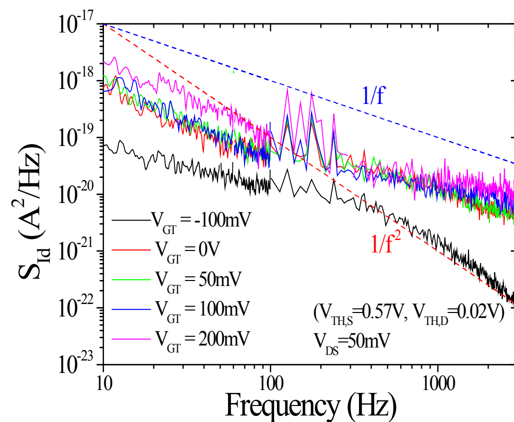

Fig.5 Drain current noise spectral density as a function of the frequency for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) structure extracted at different V_{GT}.

$$S_{Id,thermal} = 4.k.T.g_m.\gamma' \quad (1)$$

Normalizing the drain current noise by the square of the drain current (S_{Id}/I_D^2) in Fig. 6, it is possible to evaluate the LFN independently of I_D. One can see for $V_{GT} \geq 0V$ that the flicker noise changes from $1/f^{1.3}$ to $1/f^{0.7}$ as the frequency increases. Also, when V_{GT} is reduced, S_{Id}/I_D^2 increments, which is linked to the reduced free carrier concentration in the channel. Therefore, the traps activation and deactivation become more effective in causing fluctuations on I_D [14].

As a way to determine the origin of the LFN source, Fig. 7 exhibits S_{Id}/I_D^2 and $(g_m/I_D)^2$ characteristics as a function of the drain current extracted at frequency of 45Hz for single transistors (A) and A-SC structures (B). According to [19], if S_{Id}/I_D^2 is correlated to $(g_m/I_D)^2$ ratio, the noise is related to carrier number fluctuations, whereas the occurrence of other trends evidences an influence of the mobility fluctuations on the LFN. Fig. 7(A) shows close dependence between S_{Id}/I_D^2 and $(g_m/I_D)^2$ ratio, indicating that the carrier number fluctuations is the dominant noise source, which is linked to the carrier trapping and detrapping mechanisms at the Si-SiO_2 interface and in the gate oxide.

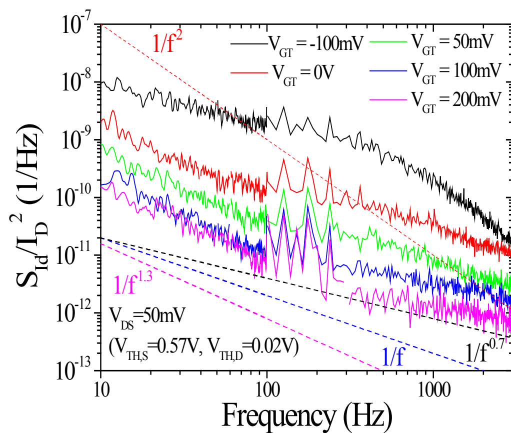

Fig.6 Normalized drain current noise spectral density as a function of the frequency for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) structure extracted at different V_{GT}.

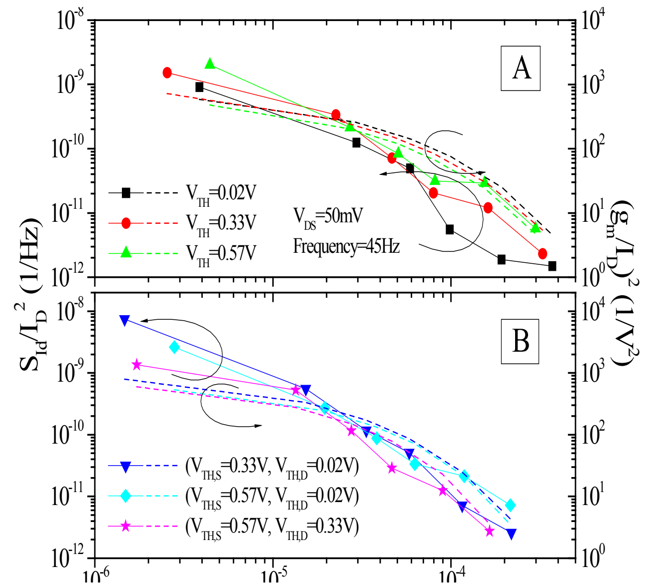

Fig.7 Normalized drain current noise spectral density (left axis, symbols) and $(g_m/I_D)^2$ ratio (right axis, lines) as a function of the drain current for single devices (A) and A-SC structures (B) at frequency of 45Hz.

However, for the single transistor with V_{TH} = 0.02V and larger I_D, the noise mechanism is changed to carrier number fluctuations with correlated mobility fluctuations. In this case, the carrier capture causes a mobility scattering. From Fig. 7(B), one can also notice a significant correlation between S_{Id}/I_D^2 and $(g_m/I_D)^2$ for all A-SC structures. Therefore, by associating single transistors in series, there is no change in the dominant noise source, which continues to be the carrier number fluctuations in this technology. Besides that, the resistance of the intermediate N+ diffusion region does not have significant importance on the noise origin, since there is no increase of S_{Id}/I_D^2 for larger I_D, which could indicate the series resistance as the main noise source [14].

The A-SC structure is characterized by the presence of two different gate voltage overdrives, one related to the M_D transistor and the other to the M_S transistor. In order to analyze the influence of each transistor in the noise of the A-SC structure, Fig. 8 shows S_{Id}/I_D^2 as a function of the frequency for A-SC structures and single transistors biased at same gate voltage as the A-SC structure (leading to different V_{GT} between M_S and M_D transistors). By analyzing the figure, it does not matter the gate voltage overdrive and the channel doping concentrations of the transistors which compose the A-SC structure, in all cases, the noise of the A-SC structure is dominated by the noise generated in the M_S transistor, since the M_D transistor is biased in higher V_{GT} for the same V_{GS}, reducing its noise. In Fig. 8(A), (B) and (C), the correct V_{GT} for the M_D transistors should be 240mV, 450mV and 210mV, respectively, instead of 200mV, 400mV and 200mV. If these gate voltage overdrives were used, the noise in the M_D transistor would be lower, which does not affect the performed analysis.

Fig. 9 shows the normalized noise as a function of the frequency extracted at V_{GT} of –100mV (A), 0V (B) and 100mV (C) for single devices and A-SC structures. In subthreshold regime, both 1/f and $1/f^2$ noises are verified for all single transistors and A-SC structures. With the increment of V_{GT}, only 1/f noise is present, as observed in Fig. 5.

For single transistors, the increase of the channel doping concentration worsens the normalized noise for all gate voltage overdrives due to the larger dose of ionic implantation, which degrades the quality of the gate oxide and the silicon interface, generating more traps. Besides that, the rise of the channel doping concentration diminishes the carrier mobility, reducing the drain current, making the drain current more susceptible to fluctuations due to the carrier trapping and detrapping mechanisms.

For A-SC structures, the presence of two transistors with same dimensions in series association doubles the gate area when compared to single transistors, incrementing the amount of traps in the gate oxide and the silicon interface, intensifying the normalized noise.

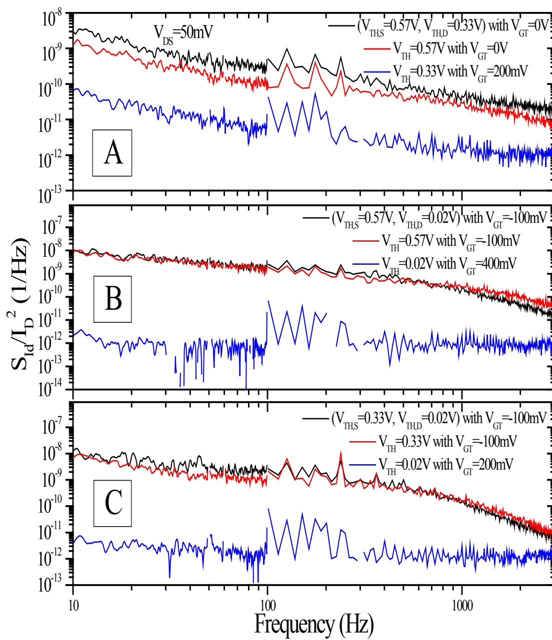

Fig.8 Normalized drain current noise spectral density as a function of the frequency for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.33V) (A), ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) (B) and ($V_{TH,S}$ = 0.33V, $V_{TH,D}$ = 0.02V) (C) structures.

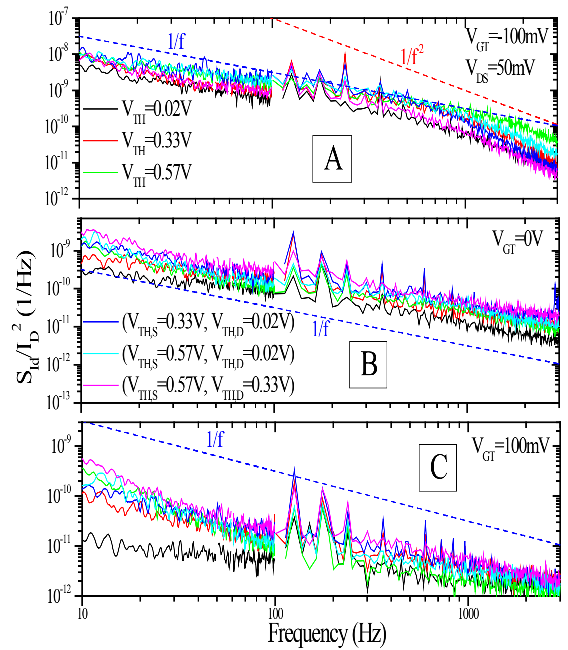

Fig. 9 Normalized drain current noise spectral density as a function of the frequency extracted at V_{GT} = -100mV (A), V_{GT} = 0V (B) and V_{GT} = 100mV (C) for single devices and A-SC structures.

This increase in the normalized noise for all A-SC structures is observed in Fig. 9(B) and (C) in the entire frequency spectrum. Besides that, if the A-SC configuration is composed by noisier transistors, the noise will be larger. Therefore, the highest normalized noise was observed for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.33V) structure, since these single devices exhibit larger noise due to the larger channel doping concentration.

The effective trap density and its effective depth in the gate dielectric can be obtained through (2) and (3), respectively, according to [14, 20]

$$N_T = \frac{S_{Id}.f.W.L.C_{oxf}^{\ 2}}{q^2.k.T.\lambda.g_m^{\ 2}} \tag{2}$$

$$x = \lambda.ln(1/2.\pi.f.\tau_0) \tag{3}$$

where C_{oxf} is the gate capacitance per unit area, given by the ratio between the oxide permittivity and the gate oxide thickness, q is the electron elementary charge, λ is the tunneling attenuation length in the gate oxide, approximately equals 10^{-8}cm for the Si-SiO_2 interface, and τ_0 is the minimum trap time constant, which is assumed equal to 10^{-10}s [14]. In (3), it is admitted that the charge exchange among the traps and the channel is purely elastic [20].

Fig. 10 presents the effective trap density as a function of the gate voltage overdrive for single transistors and A-SC structures extracted at frequency of 45Hz. At V_{GT} = –100mV,

the effective trap density reaches the maximum value for any transistor, which is in accordance with the larger normalized noise verified in Fig. 6. For higher gate voltage overdrive, one can notice a reduction of the effective trap density for all devices, reaching the minimum around V_{GT} = 100mV and then a slight increment of N_T is noted. As expected, the increase of the channel doping concentration raises the effective trap density.

When analyzed the A-SC structures, it is evident the larger effective trap density compared with single transistors for $V_{GT} \leq$ 100mV. When the gate voltage overdrive is incremented, the effective channel length of the A-SC structure tends to $L_S + L_D$. In this condition, it is necessary to substitute L for approximately $L_S + L_D$ in (2) to correct and increase the effective trap density. In Fig. 10, for the sake of simplicity, it was used $L = L_S$ in (2) for all A-SC structures. It is possible to see that the A-SC ($V_{TH,S}$ = 0.33V, $V_{TH,D}$ = 0.02V) and ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) structures exhibit the highest effective trap density in almost all V_{GT}.

Fig. 11 shows the effective trap density as a function of the effective trap depth for single devices and A-SC structures extracted at V_{GT} = 0V. As the noise measurement was performed in the range of frequencies from 10 to 10kHz, the effective trap depth varied from 1.2 to 1.9nm. Larger frequencies are related to traps located close to the silicon interface, whereas lower frequencies are linked to traps deeper inside the gate oxide. For all devices, it can be noted that there is a slight reduction of the effective trap density deeper inside the gate oxide, indicating that the frequency exponent is a little smaller than unity.

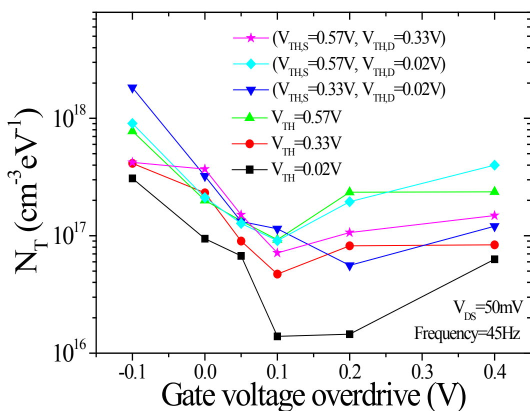

Fig.10 Effective trap density as a function of the gate voltage overdrive for single devices and A-SC structures extracted at frequency of 45Hz.

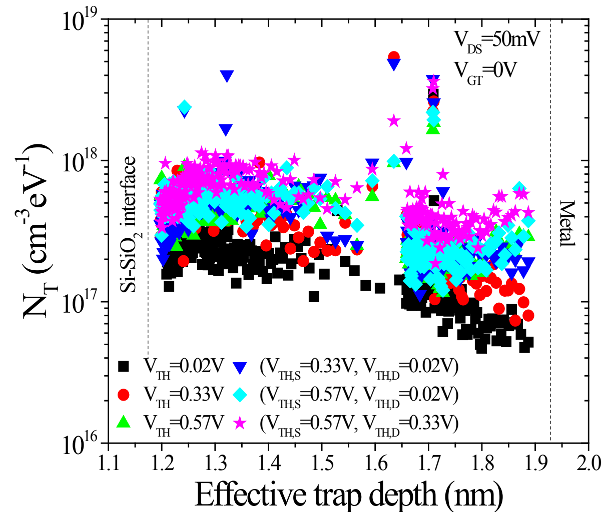

Fig.11 Effective trap density as a function of the effective trap depth for single devices and A-SC structures extracted at V_{GT} = 0V.

For single devices, the increase of channel doping concentration increments the effective trap density in the entire gate oxide depth. Similarly, the series association of two single transistors, composing the A-SC structure, also causes an increase of the effective trap density, mainly for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.33V) structure.

Fig. 12 exhibits N_T as a function of the effective trap depth for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) structure. For all V_{GT}, one can see that a minimum N_T occurs close to 1.65nm. By analyzing Fig. 6, for f < 100Hz (x > 1.65nm), γ = 1.3. This way, there is larger N_T close to the metal. However, for f > 100Hz (x < 1.65 nm), γ = 0.7, indicating that there is a larger N_T close to the Si-SiO_2 interface.

Fig. 13 presents the effective trap density as a function of the effective trap depth for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.33V) structure and single transistors biased in the same V_{GT} of the A-SC structure in order to evaluate the influence of trap density of each transistor which compose the A-SC structure. It is possible to see that the A-SC structure presents effective trap density similar to the M_S transistor, indicating that the asymmetric self-cascode structure is governed by the M_S transistor, as previously noted in Fig. 8.

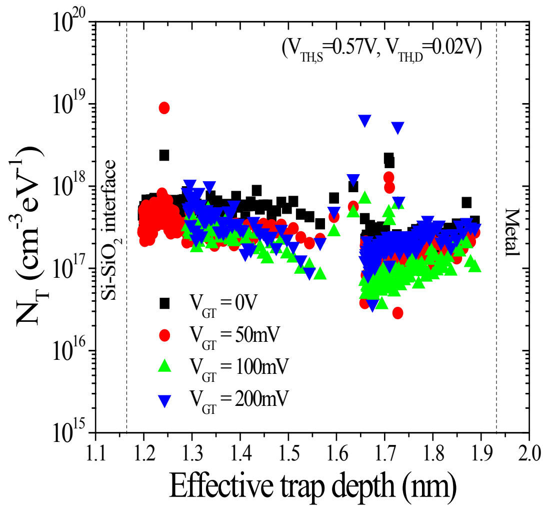

Fig.12 Effective trap density as a function of the effective trap depth for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) structure extracted at different V_{GT}.

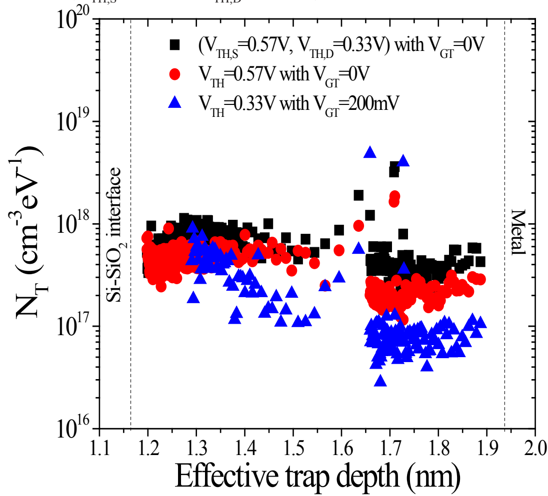

Fig.13 Effective trap density as a function of the effective trap depth for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.33V) structure and single transistors.

B. LFN – saturation regime

Since analog circuits often operate in saturation, the noise in this regime has also been evaluated. When the devices are biased at high V_{DS}, 1/f noise continues to be the dominant noise characteristic at low frequencies, whereas at high frequencies $1/f^2$ noise component arises as presented in Fig. 14, where S_{Id} is plotted against frequency for the A-SC ($V_{TH,S}$ = 0.33V, $V_{TH,D}$ = 0.02V) (A), ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) (B) and ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.33V) (C) structures biased at V_{DS} = 0.7V and different V_{GT}. One can see for all A-SC structures no significant influence of V_{GT} on S_{Id} at low frequencies, only when the g-r noise becomes important there is a dependence on V_{GT}, which is related to the variation of the Lorentzian corner frequency. Apparently, the Lorentzian-like noise starts at the same frequency for the A-SC structures of same V_{GT}, and this frequency is approximately equal to 1kHz at V_{GT} = 200mV. By increasing V_{GT}, the corner frequency increments, being the 1/f noise the dominant noise component.

In Fig. 15, S_{Id}/I_D^2 is plotted against frequency for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) structure at several V_{GT}. According to this figure, higher V_{GT} reduces S_{Id}/I_D^2 as obtained in the linear regime, since there are more carriers flowing in the channel. This way, the capture or emission of any carrier by traps causes a lower impact on I_D, maintaining its value and hence reducing S_{Id}/I_D^2. Also, the Lorentzian-like noise is shifted to higher frequencies as V_{GT} increases. By comparing with Fig. 6, S_{Id}/I_D^2 is larger at V_{GT} = 200mV when the device operates in the saturation regime due to the larger electric field close to the drain, which induces a greater charge trapping in the gate oxide, since the tunneling current through the gate becomes especially important when the transistor operates in this regime. This way, there is an increase of the trap density, which causes an increment in the low-frequency noise [21].

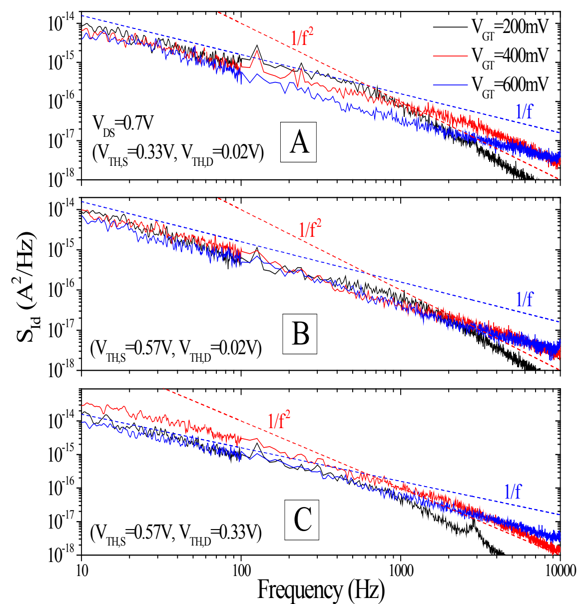

Fig. 14 Drain current noise spectral density as a function of the frequency for the A-SC ($V_{TH,S}$ = 0.33V, $V_{TH,D}$ = 0.02V) (A), ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) (B) and ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.33V) (C) structures extracted at several V_{GT} in saturation (V_{DS} = 0.7V).

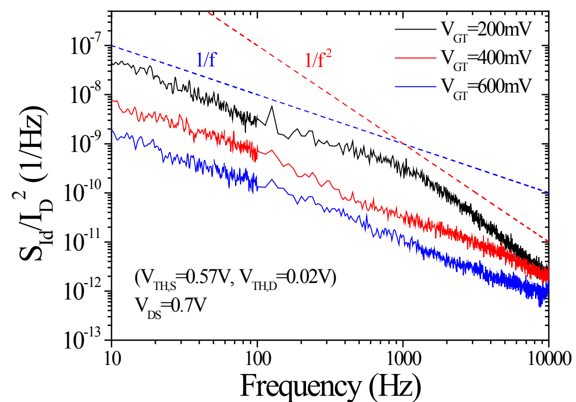

Fig.15 Normalized drain current noise spectral density as a function of the frequency for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) structure biased at several V_{GT} in saturation.

Fig. 16 presents S_{Id}/I_D^2 plotted against frequency extracted at V_{GT} = 200mV (A), 400mV (B) and 600mV (C). One can see that the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.33V) structure exhibits the largest normalized noise in the entire frequency spectrum when compared with the other A-SC structures for all V_{GT}, which can be related to the larger channel doping concentration in the transistors which compose the asymmetric self-cascode structure, degrading the quality of the gate oxide and the silicon interface. As observed before, the corner frequency does not vary among the A-SC structures biased at same V_{GT}.

The curves of S_{Id}/I_D^2 and $(g_m/I_D)^2$ have been plotted as a function of the drain current in Fig. 17 for A-SC structures biased at V_{DS} = 0.7V and frequency of 45Hz. As one can see, the curves show the same trends with the drain current for all transistors. This way, by biasing the A-SC structures at high drain voltage, the carrier number fluctuations continue to be the 1/f noise origin.

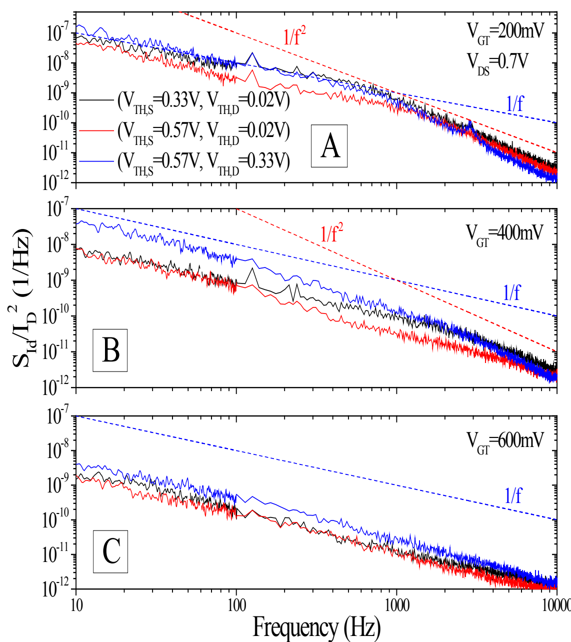

Fig. 16 Normalized drain current noise spectral density as a function of the frequency extracted at V_{GT} = 200mV (A), V_{GT} = 400mV (B) and V_{GT} = 600mV (C) for A-SC structures.

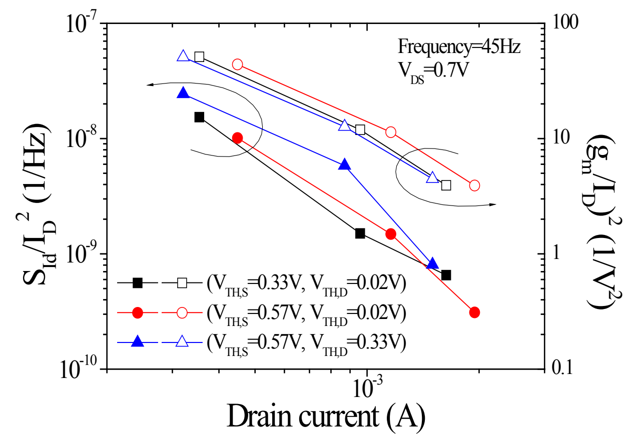

Fig.17 Normalized drain current noise spectral density (left axis, closed symbols) and $(g_m/I_D)^2$ (right axis, open symbols) as a function of the drain current for A-SC structures extracted at frequency of 45Hz.

In order to compare the A-SC structures for different inversion levels, the normalized noise has been plotted as a function of the transconductance to drain current ratio for A-SC structures extracted at frequency of 45Hz in Fig. 18. Based on this figure, one can see similar normalized noise between the A-SC ($V_{TH,S}$ = 0.33V, $V_{TH,D}$ = 0.02V) and ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.02V) structures. The highest S_{Id}/I_D^2 has been observed for the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.33V) structure since the larger channel doping concentration reduces the drain current as well as increases the effective trap density.

V. Conclusions

The low-frequency noise of the A-SC structures of different channel doping concentrations has been analyzed in the linear and saturation regimes and compared with single transistors. At low V_{DS}, it has been found that the drain current noise spectral density is of 1/f type for all V_{GT}. However, at V_{GT} = –100mV, it has also been observed the presence of Lorentzians. The operation in the subthreshold regime has incremented the normalized noise, since the little amount of carriers in the channel makes the carrier trapping

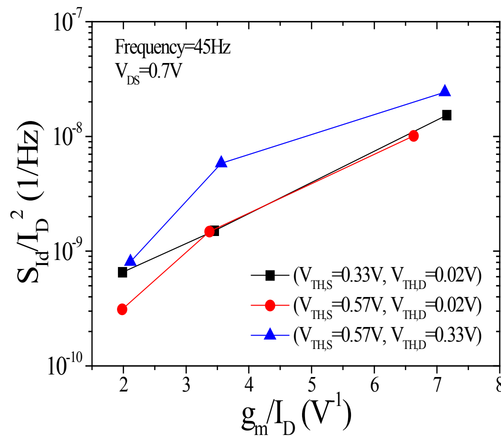

Fig.18 Normalized drain current noise spectral density as a function of the transconductance to drain current ratio for A-SC structures extracted at frequency of 45Hz.

and detrapping more important on the I_D fluctuations. It has been proved that the main type of noise source is linked to carrier number fluctuations. Also, it has been verified that the noise in the A-SC structure is dominated by the noise generated in the M_S transistor. The increase of the channel doping concentration has incremented the normalized noise due to the larger dose of ionic implantation, worsening the quality of the silicon interface and the gate oxide. The A-SC structures have presented larger S_{Id}/I_D^2 compared with single transistors. Finally, the effective trap density has been extracted, it has been observed that the increase of the channel doping concentration has raised N_T in the entire gate oxide depth, with higher N_T for A-SC structures.

At high V_{DS}, it has been verified that the 1/f noise continues to be the dominant noise component at low frequencies, whereas at high frequencies $1/f^2$ noise takes place. By incrementing the gate voltage overdrive, there is a reduction of the S_{Id}/I_D^2 as well as an increase of the corner frequency, shifting the g-r noise to higher frequencies. Also, the normalized noise has been significantly incremented compared with the linear regime, which is linked to the rise of S_{Id}. As observed at low drain voltage, the noise source has also been given by carrier number fluctuations, and the A-SC ($V_{TH,S}$ = 0.57V, $V_{TH,D}$ = 0.33V) structure has presented the largest normalized noise.

Acknowledgements

The authors would like to acknowledge the Brazilian research-funding agencies FAPESP grant #2015/08616-6 and CNPq grants #311466/2016-8 and #427975/2016-6 for the financial support.

References

[1] J.-P. Colinge, *Silicon-on-insulator technology: materials to VLSI*, 3rd ed, Springer, New-York: 2004, 366p.

[2] J.-P. Colinge, "Subthreshold slope of thin-film SOI MOSFET's," *IEEE Electron Device Letters*, vol. 7, no. 4, Apr., 1986, pp. 244-246.

[3] M. Yoshimi, H. Hazama, M. Takahashi, S. Kambayashi, and H. Tango, "Observation of mobility enhancement in ultrathin SOI MOSFETs," *Electronics Letters*, vol. 24, no. 17, Aug., 1988, pp. 1078-1079.

[4] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 36, no. 2, Feb., 1989, pp. 399-402.

[5] D. Flandre, L. F. Ferreira, P. G. A. Jespers, and J.-P. Colinge, "Modelling and application of fully depleted SOI MOSFETs for low voltage, low power analogue CMOS circuits," *Solid-State Electronics*, vol. 39, no. 4, Apr., 1996, pp. 455-460.

[6] J.-Y. Choi, and J. G. Fossum, "Analysis and control of floating-body bipolar effects in fully depleted submicrometer SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 38, no. 6, June, 1991, pp. 1384-1391.

[7] C. Galup-Montoro, M. C. Schneider, and I. J. B. Loss, "Series-parallel association of FET's for high gain and high frequency applications," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 9, Sep., 1994, pp. 1094-1101.

[8] M. de Souza, D. Flandre, R. T. Doria, R. Trevisoli, and M. A. Pavanello, "On the improvement of DC analog characteristics of FD SOI transistors by using asymmetric self-cascode configuration," *Solid-State Electronics*, vol. 117, Mar., 2016, pp. 152-160.

[9] M. de Souza, D. Flandre, and M. A. Pavanello, "Analog performance of asymmetric self-cascode p-channel fully depleted SOI transistors," in *8th International Caribbean Conference on Devices, Circuits and Systems (ICCDCS)*, 2012, pp. 1-4.

[10] M. de Souza, D. Flandre, and M. A. Pavanello, "Asymmetric self-cascode configuration to improve the analog performance of SOI nMOS transistors," in *International SOI Conference*, 2011, pp. 1-2.

[11] R. Assalti, M. A. Pavanello, D. Flandre, and M. de Souza, "Asymmetric self-cascode versus graded-channel SOI nMOSFETs for analog applications," in *30th Symposium on Microelectronics Technology and Devices (SBMicro)*, 2015, pp. 1-4.

[12] M. de Souza, V. Kilchtyska, D. Flandre, and M. A. Pavanello, "Liquid helium temperature analog operation of asymmetric self-cascode FD SOI MOSFETs," in *International SOI Conference*, 2012, pp. 1-2.

[13] R. T. Doria, R. D. Trevisoli, M. de Souza, and M. A. Pavanello, "Application of junctionless nanowire transistor in the self-cascode configuration to improve the analog performance," in *27th Symposium on Microelectronics Technology and Devices (SBMicro)*, 2012, pp. 215-222.

[14] M. V. Haartman, and M. Östling, *Low-frequency noise in advanced MOS devices*, Springer, Dordrecht: 2007, 216p.

[15] C. G. Theodorou, N. Fasarakis, T. Hoffman, T. Chiarella, G. Ghibaudo, and C. A. Dimitriadis, "Origin of the low-frequency noise in n-channel FinFETs," *Solid-State Electronics*, vol. 82, Apr., 2013, pp. 21-24.

[16] A. L. McWhorter, "1/f noise and germanium surface properties," in *Semiconductor Surface Physics*, 1957, pp. 207-228.

[17] F. N. Hooge, "1/f noise is no surface effect," *Physics Letters A*, vol. 29, no. 3, Apr., 1969, pp. 139-140.

[18] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and design of analog integrated circuits*, 5th ed, John Wiley & Sons, Hoboken: 2009, 881p.

[19] G. Ghibaudo, O. Roux, Ch. Nguyen-Duc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect MOS transistors," *Physica Status Solidi (a)*, vol. 124, no. 2, Apr., 1991, pp. 571-581.

[20] S. Put, H. Mehta, N. Collaert, M. Van Uffelen, P. Leroux, C. Claeys, N. Lukyanchikova, and E. Simoen, "Effect of rotation, gate-dielectric and SEG on the noise behavior of advanced SOI MugFETs," *Solid-State Electronics*, vol. 54, no. 2, Feb., 2010, pp. 178-184.

[21] C. Jakobson, I. Bloom, and Y. Nemirovsky, "1/f noise in CMOS transistors for analog applications from subthreshold to saturation," *Solid-State Electronics*, vol. 42, no. 10, Oct. 1998, pp. 1807-1817.