Ground Plane Influence on Analog Parameters of Different UTBB nMOSFET Technologies

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Abstract— **This paper presents an analysis of the silicon film thickness (6 nm and 14 nm), the gate dielectric material (SiO_2 and High- κ material) and the Ground Plane influence on the analog parameters of Ultra Thin Body and Buried Oxide (UTBB) SOI nMOSFET devices, based on experimental and simulation results. Two channel lengths (70 nm and 1μm) have been considered and the analog performance has been analyzed as a function of the back gate bias.**

It is shown that at zero back gate bias , the presence of a Ground Plane improves the transconductance in the saturation region due to the strong coupling between front and back gates in devices with a long channel (1 μm), thin silicon film (6 nm) and SiO_2 as gate dielectric material. However, for the intrinsic voltage gain, output conductance and Early Voltage, the devices without Ground Plane present better results due to the higher drain electrical field penetration.

Short-channel transistors (70 nm) with Ground Plane show an improvement of the analog parameters also due to the high drain electrical field penetration. Similar behavior is noticed in devices with a thicker silicon film (14nm). UTBB nMOSFETs with High- κ material present less influence of a Ground Plane on the parameters analyzed.

Varying the back gate bias in devices with long channel (1 μm) and SiO_2 as gate dielectric material, the analog parameters present better results in devices without Ground Plane, except for the transconductance in long channel transistors with a thin silicon film, for the reason explained before (strong coupling between front and back gates). Devices with High-κ material as gate dielectric show a minor improvement of the analog performance with a Ground Plane.

Index Terms—UTBB, SOI, Analog Parameters, Ground Plane.

I. Introduction

The Silicon-on-Insulator (SOI) technology has been enabling the downscaling of MOSFETs maintaining the planar technology and more recently, UTBB FDSOI (Ultrathin-Body-and-Buried-Oxide Fully-Depleted-SOI) have been developed for the 14 nm and 10 nm technology nodes. This approach is a planar technology solution that presents good performance characteristics like high speed, low power and better control of Short Channel Effect (SCE) [1-5]. However, the strong coupling between front and back interfaces for thinner silicon film and buried oxide increases the effect of the substrate potential drop on the device parameters.

In order to minimize the substrate effect a doping implantation under the buried oxide, called Ground Plane (GP), is an alternative to maintain a proper functioning of the device. The study and analytical modeling of the influence of a GP was reported in [6-8]. Moreover, the presence of a GP on the Dynamic Threshold operation mode was studied and modeled in [9-11]. The analog performance was reported in [12] where the GP influence was studied for the analog figures of merit and in [13-14] where an initial study of the same devices presented in this paper was done.

This paper presents a detailed analysis of the silicon film thickness, the gate dielectric material and GP influence on the main analog parameters like transconductance in saturation regime (gm_{SAT}), output conductance (g_D), intrinsic voltage gain (A_V) and Early voltage (V_{EA}) of UTBB SOI nMOSFETs. A short (70 nm) and a long (1 μm) transistor are considered, whereby also the role of the back gate bias is highlighted.

II. Device Details

Three different combinations of silicon thickness and gate dielectric material were studied as summarized in table I. The reference technology has a silicon thickness (t_{Si}) of 6 nm and gate stack composed of 5 nm SiO_2 thermal oxide and a TiN metal gate electrode (SiO_2 / t_{Si}=6). These devices were fabricated for 1T-DRAM applications, where the gate oxide thickness (t_{oxf}) is thicker to obtain a small gate leakage current [15-16].

The second technology has the same gate stack characteristics of the reference device, but has 14 nm of silicon thickness (SiO_2 / t_{Si}=14). The third technology has 6 nm of silicon thickness (as the reference) and a gate stack composed of 1.5 nm of SiO_2 plus 4.2 nm of HfSiO (High- κ) and a TiN metal gate electrode (HK / t_{Si}=6).

All devices have a silicon film concentration (Na) around 10^{15} cm^{-3} since there is no channel doping, the substrate concentration (Na_{SUB}) is also around 10^{15} cm^{-3} for the same reason. There are devices that have a GP implantation under the buried oxide, by a boron implantation at 25keV and a dose of $5x10^{13}$ cm^{-2}, resulting in a substrate concentration around $1x10^{18}$ cm^{-3} [17].

Two different channel lengths were studied: L= 70 nm and 1 μm. The width of all device is W=1 μm. All devices have a spacer of 10 nm creating an underlap region between

source/drain and channel.

The UTBB SOI nMOSFET devices were fabricated at imec, Belgium, on SOI substrates with a final buried oxide thickness (t_{oxb}) of 18 nm. More process information can be found in [16].

Table I - UTBB SOI Technologies

	Gate Dielectric Material	Silicon Thickness
SiO_2 / t_{Si}=6	SiO_2	6 nm
SiO_2 / t_{Si}=14	SiO_2	14 nm
HK / t_{Si}=14	High-κ	6 nm

A schematic cross-section of the SOI nMOSFET is shown in Figure 1, where V_S, V_D, V_{GF} and V_{GB} are the source, drain, front-gate and substrate (or back-gate) voltage, respectively. t_{oxf}, t_{Si} and t_{oxb} are the gate oxide (front oxide), silicon channel and buried oxide thickness respectively.

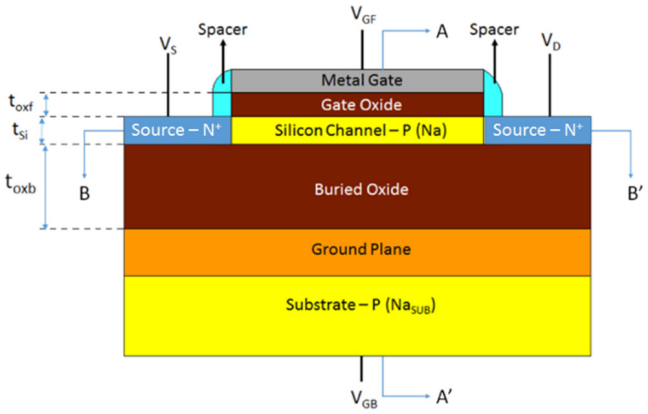

Figure 1. A schematic cross-section of an UTBB SOI device with Ground Plane.

III. Measurement and Simulation Details

Figure 2A shows the measured front threshold voltage V_{TF} as function of V_{GB} for UTBB devices. Measurements were done from V_{GB} = -5 to 5V to extract the threshold voltage. In this range it was noted that the back interface is always in depletion regime. Figure 2B is a blow up of figure 2A, where it is possible to see the different conditions for the third interface (buried oxide/substrate) and how it affects the threshold voltage.

Martino *et al*. [18] proposed an analytical model where the variation of (potential drop in the substrate) affects directly the threshold voltage. The variation of occurs when the back gate voltage varies.

In figure 2b, the value of V_{GBmin} and V_{GBmax} represents the boundary between inversion/depletion and depletion/accumulation regime for the third interface [8].

The analytical model pointed out that for many applications $\varnothing_{SUB}$ could not be neglected when the buried oxide becomes lower than 100 nm. Recently, this effect has become even more pronounced due to a thinner buried oxide (lower than 20 nm)

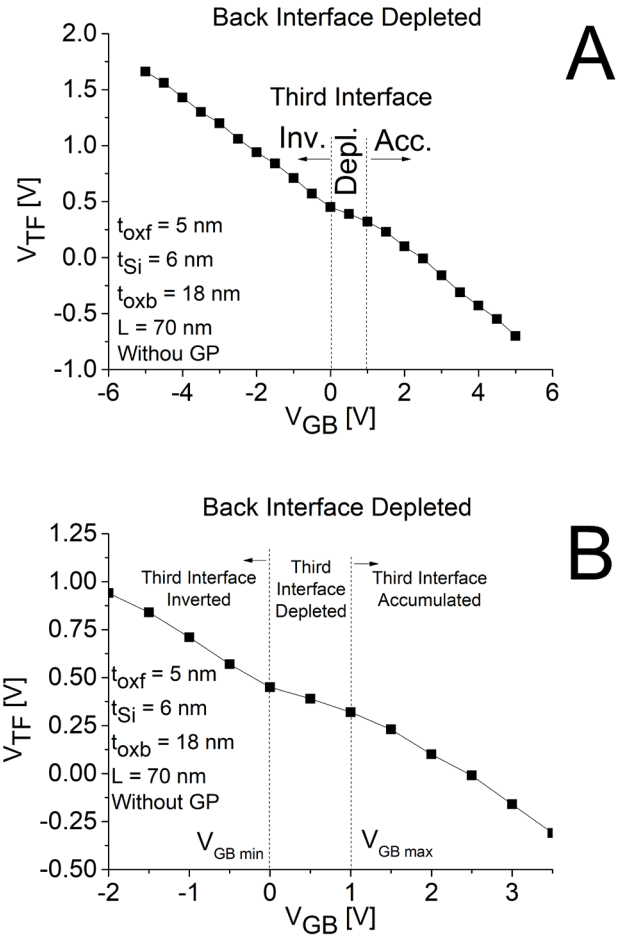

Figure 2. a) Experimental front threshold voltage as a function of back gate voltage. b) blow up of figure 2A.

and silicon film (lower than 10 nm) for UTBB SOI devices.

In order to minimize the depletion region at the buried oxide/substrate interface (which is the cause of the substrate influence on the electrical device characteristics) a Ground Plane (GP) implantation below the buried oxide is normally used in UTBB SOI. To improve the analytical model the quantum confinement effect was also considered [19,20], which changes the effective thickness of the silicon film and gate oxide. Figure 3 shows a curve obtained through the analytical model considering quantum confinement effect.

In order to analyze the different condition which the Ground Plane provides, the analytical model considering the quantum confinement effect was used to determine the back gate bias interval that will be used. The value of V_{GBMax} and V_{GBMin} for the three different devices have been extracted by the model for devices with and without GP, as shown in table II.

The measurements were done with an Agilent B1500 system on 3 to 6 devices per process condition. The I_D vs. V_{GF} curves, with V_{DS} = 50 mV in the triode region and V_{DS} = 1 V in the saturation region were measured with four different values of V_{GB} (-3V; -1V; 0V and 1V), based on the values extracted in table II. The threshold voltage V_{TF} (V_{DS}=50mV)

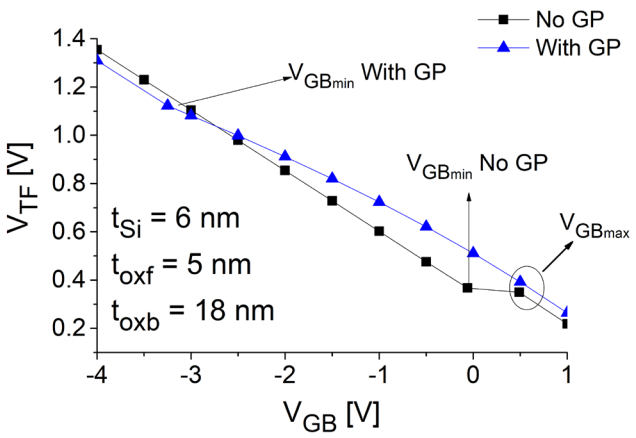

Figure 3. Theoretical V_{TF} vs. V_{GB} for SiO_2 / t_{Si}=6 device with and without GP.

was extracted based on the maximum value of dgm/dV_{GF} as a function of V_{GF} for each V_{GB} [21].

Table II - VGBMax and VGBMin for three technologies with and without Ground Plane

	GP	No GP
	SiO_2 / t_{Si}=6	
V_{GBMax}	0.76 V	0.59 V
V_{GBMin}	-3.40 V	-0.08 V
	SiO_2 / t_{Si}=14	
V_{GBMax}	0.76 V	0.59 V
V_{GBMin}	-3.83 V	-0.09 V
	HK / t_{Si}=6	
V_{GBMax}	0.76 V	0.59 V
V_{GBMin}	-3.40 V	-0.08 V

After extraction of the V_{TF} (V_{DS}=50mV), I_D vs. V_{DS} curves were measured in saturation region with V_{DS} = 1 V and V_{GT} = 200mV for the same V_{GB}. From these curves g_D and V_{EA} parameters were obtained.

Bi-dimensional numerical simulations, using the Atlas simulator [22], were used to analyze the potential in the AA' and BB' cutline as shown in figure 1, to explain the influence of the GP implantation for devices with the same characteristics. The gate electrode considered has a metal work function around 4.53 eV (TiN). Interface traps were considered in the simulations with N_{itf}=N_{itb}=$2x10^{11}$ $eV^{-1}cm^{-2}$ [23]. UTBB SOI nMOSFETs with a substrate doping concentration of Na_{SUB}=10^{18} and 10^{15} cm^{-3} were used to simulate devices with and without GP, respectively.

IV. Results and Analysis

A. Ground Plane Influence varying the back gate voltage

Due to the fact that devices with L= 1 µm present better results, the following analyses were done on these devices.

The value of V_{GB} was chosen based on the values of $V_{GBmáx}$ and V_{GBmin} extracted by the analytical model.

Figure 4 shows the gm_{SAT} for different V_{GB}. For device SiO_2/t_{Si} =6 the values of gm_{SAT} for V_{GB} = 1V are similar for devices with and without GP. However for V_{GB} = 0V, -1V and -3V there is a difference between them.

By simulation, the potential drop were extracted (data of

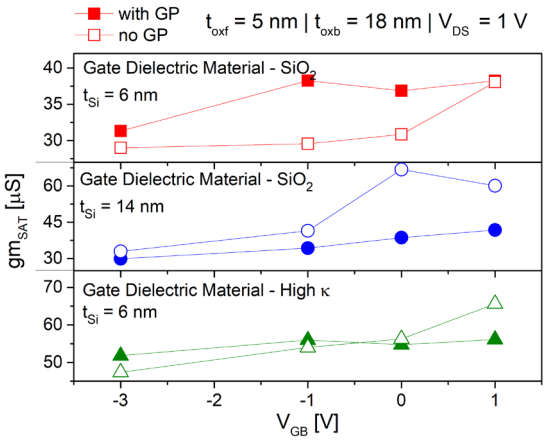

Figure 4. Experimental data of transconductance in saturation region (gm_{SAT}), for three UTBB SOI technologies in function of back gate bias.

the electric potential along the device depth - AA' cutline in figure 1). Figure 5 shows the simulated potential drop as a function of the depth. The extracted values of potential drop at the substrate can be seen in Table III.

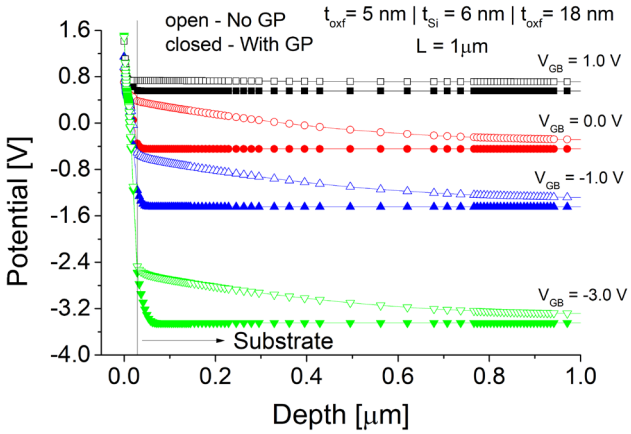

Figure 5. Simulation data of the electric potential along the device depth for V_{GB} = 1V, 0V, -1V and -3V, with and without GP

Table III - Potential Drop At Substrate For Different V_{GB} With And Without GP

	V_{GB} = 1V	V_{GB} = 0V	V_{GB} = -1V	V_{GB} = -3V
Without GP	0.02V	0.67V	0.78V	0.82V
With GP	0.01V	0.10V	0.29V	0.87V
$\Delta\varnothing_{SUB}$	0.01 V	0.57 V	0.49 V	0.05 V

It is observed in table III, for V_{GB} = 1V and -3V, that the difference between $\varnothing_{SUB}$ is around 10 mV and 50 mV, respectively, due to the fact that the substrate effect was minimized/ negligible when the third interface is in accumulation and inversion [7].

For V_{GB} = 0V and -1V, when the third interface is in the depletion regime, the influence of the substrate effect is higher. In these cases the difference between $\varnothing_{SUB}$ of devices without GP and with GP is higher than 500 mV.

The difference between gm_{SAT} of devices without GP and with GP, shown in table III, is related with the strong coupling (supercoupling) between front and back interfaces and it presents a higher gm_{SAT}.

Figure 6 shows the electric potential along the device length (BB' cutline in figure 1), 3 nm from the front interface (in the middle of the channel) for devices SiO_2 / t_{Si}= 6 with and without GP [13].

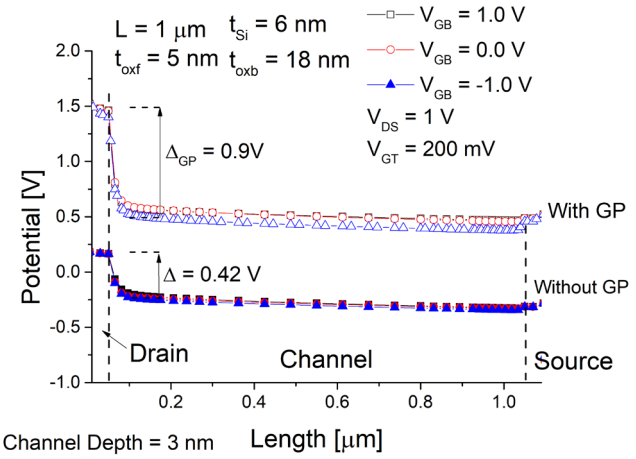

Figure 6. Simulation data of the electric potential along the device length for V_{GB} = 1V, 0V and -1V, with and without GP, 3 nm in depth from the front interface.

In figure 6, devices with GP present a potential difference between the drain and channel (Δ_{GP}) around two times larger than the devices without GP (Δ). This means that the drain electrical field at this region is higher in devices with GP.

However, for the SiO_2 / t_{Si} = 6 case with L = 1 µm the influence of supercoupling between the front and back gates is higher than the drain electrical field penetration.

Already in a device with thicker silicon film (SiO_2 / t_{Si}=14), the coupling between the front and back gate is lower than for a device with silicon a thickness of 6 nm and the influence of the drain electrical field penetration is more important. The higher drain electrical field penetration in devices with GP degrades the analog parameters, as can be seen in table III for the SiO_2 / t_{Si}=14 device.

Figure 7 shows the g_D (7a), A_V (7b) and V_{EA} (7c), respectively, for different values of V_{GB}.

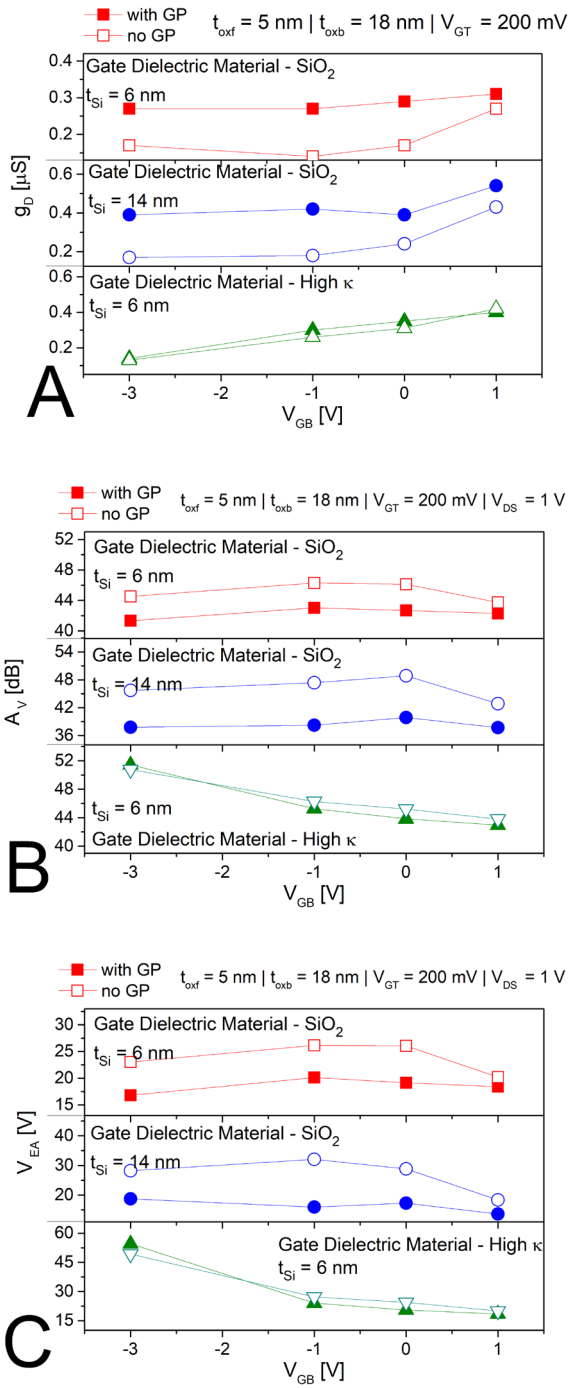

Figure 7. Experimental data of a) output conductance (g_D), b) intrinsic voltage gain (A_V) and c) Early Voltage (V_{EA}), for three UTBB SOI technologies in function of back gate bias.

In figures 4 and 7there are a few cases in which the analog parameter with GP presents better results (disregarding the gm_{SAT} for SiO_2/t_{Si}=6 case that has been explained previously). These occur in devices with t_{Si} = 6 nm + High-κ. However, in HK / t_{Si}=6 devices the presence of a GP does not affect the analog parameters significantly.

In Table IV it is possible to see a lower percentage difference comparing HK / t_{Si}=6 devices with and without GP.

Table IV - Percentage Difference of A_V between devices with and without GP, for V_{GB} = -3V, -1V, 0V and 1V

V_{GB}	**HK / t_{Si}=6 ($_{with\ GP}$ - $_{without\ GP}$) [%]**			
	gm_{SAT}	g_D	A_V	V_{EA}
1 V	-14%	**-6%**	-2%	-7%
0 V	-3%	14%	-3%	-16%
-1 V	**4%**	16%	-2%	-12%
-3 V	**9%**	1%	**1%**	**11%**

B. Ground Plane Influence varying the channel length.

Figure 8 shows the measured normalized transconductance in saturation region (gm_{SAT}), for all devices studied. For the reference devices (SiO_2 / t_{Si}=6) with t_{Si} = 6 nm + SiO_2, one can see that for L=1µm with GP a higher gm_{SAT} than for devices without GP is observed.

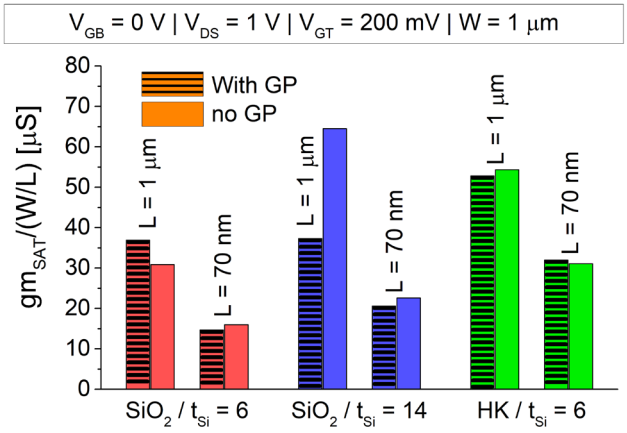

Figure 8. Experimental data of normalized transconductance (gm_{SAT}), for three UTBB SOI technologies.

The difference between gm_{SAT} of devices without GP and with GP, shown in figure 8, is related with the strong coupling (supercoupling) between front and back interfaces [13] as mentioned in the previous section. However, in devices with L=70 nm, the influence of the drain electrical field penetration is higher than the supercoupling between front and back interfaces.

Transistors with t_{Si} = 14 nm + SiO_2 (SiO_2 / t_{Si}=14), for L = 70 nm and 1µm present better results for the case without GP. This can be explained considering that the supercoupling is less effective in these devices, because of the thicker t_{Si}, and the drain electrical field penetration is higher for the condition with GP (degrading the gm_{SAT}).

Device with t_{Si} = 6 nm + High-κ (HK / t_{Si}=6) presents the lower percentage difference comparing devices with and without GP, as shown in Table V.

Table V - Percentage Difference of Transconductance in Saturation Region for devices with and without GP

L	**$gm_{SAT,\ with\ GP}$ - $gm_{SAT,\ without\ GP}$ [%]**		
	SiO_2 / t_{Si}=6	***SiO_2 / t_{Si}=14***	***HK / t_{Si}=6***
70 nm	-8,2 %	-9,0 %	-3,0 %
1 µm	8,6 %	-42,1 %	2,8 %

Figures 9, 10 and 11 show the measured output conductance, intrinsic voltage gain and Early Voltage for the devices studied.

In all cases, devices without GP present better results, due to the lower drain electrical field penetration, in agreement with the tendency observed in [13].

In figures 8 to 11, it is also possible to see that in all cases the analyzed parameters behave as expected for shorter channels [24]. Values of gm_{SAT}, A_V and V_{EA} decrease with the channel length, while g_D increases. Therefore, the device with L= 1 µm presents better results.

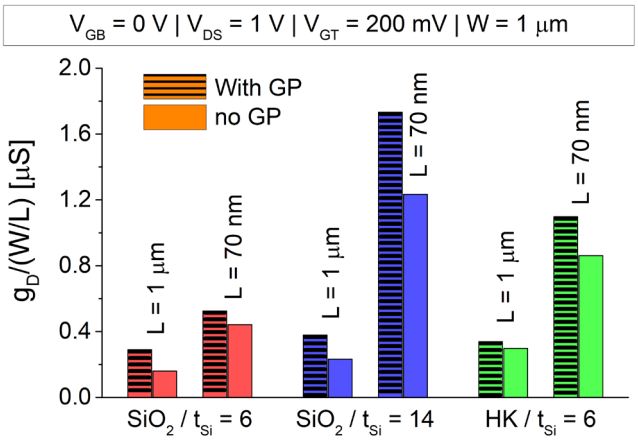

Figure 9. Experimental data of normalized output conductance (g_D), for three UTBB SOI technologies.

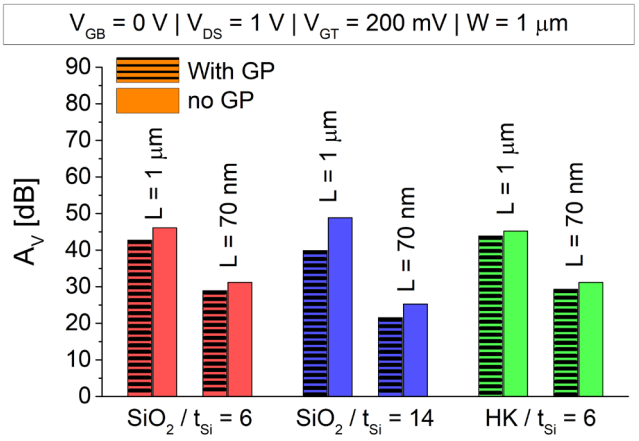

Figure 10. Experimental data of intrinsic voltage gain (A_V), for three UTBB SOI technologies.

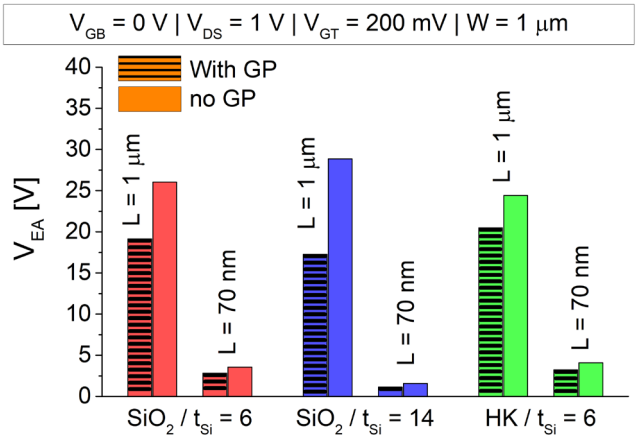

Figure 11. Experimental data of Early Voltage (V_{EA}), for three UTBB SOI technologies.

V. Conclusions

This paper shows the analysis of the Ground Plane (GP) influence on analog parameters for different Ultra Thin Body and Buried Oxide (UTBB) SOI nMOSFET technologies. Experimental data and simulations have been combined.

Analyzing the reduction of the channel length shows that the analog parameters follow the natural tendency as explained in the literature. As the channel length decreases all the analog parameters became worse. This occurs for all three technology conditions studied.

Devices with Ground Plane have a higher drain electrical field penetration, which degrades the analog parameters. All devices with silicon film of 14 nm and without ground plane have better analog parameters than devices with Ground Plane.

Devices with 6 nm of silicon film and SiO_2 as gate dielectric material present better analog parameters when the Ground Plane is absent. However, the transconductance in the saturation region is lower in devices with Ground Plane when the channel length is 1 µm. In this device the drain electrical field penetration is not the principal factor that affects the analog parameters. The presence of a Ground Plane generates a lower potential drop at the substrate and devices without Ground Plane have a higher potential drop at the substrate which degrades the transconductance in the saturation region.

In devices with a High-κ front gate dielectric the percentage variation of the results, comparing UTBB SOI nMOSFETs with and without Ground Plane, is negligible. Therefore, devices with High-κ suffer less influence of the presence of a Ground Plane.

Acknowledgements

The authors would like to thank CAPES, FAPESP and CNPq for the financial support.

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