Analytical Model for Threshold Voltage in UTBB SOI MOSFET in Dynamic Threshold Voltage Operation

V. T. Itocazu[1*], K. R. A. Sasaki[1], V. Sonnenberg[1,2], J.A. Martino[1], E. Simoen[3] and C. Claeys[3,4]

[1]LSI/PSI/USP, University of Sao Paulo, Brazil
[2]FATEC/SP e OSASCO / CEETEPS - Faculdade de Tecnologia de Sao Paulo e de Osasco, Sao Paulo, Brazil
[3]imec, Leuven, Belgium
[4]E.E. Department KU Leuven, Belgium
*corresponding author, e-mail: tatsuo@lsi.usp.br

***Abstract* — This paper presents an analytical model to determine the threshold voltage in Ultrathin Body and Buried Oxide Fully Depleted Silicon on Insulator (UTBB FD SOI) MOSFETs operating in dynamic threshold (DT) voltage modes. The analytical model is based on implementing the quantum confinement effect and the DT restriction. The results show that the proposed analytical model in its simplicity provides a good agreement to the experimental data.**

Index Terms—UTBB, SOI, Analytic Model, Dynamic Threshold.

I. Introduction

The UTBB FDSOI (Ultrathin-Body-and-Buried-Oxide Fully-Depleted-SOI) devices have been enabling downscaling with a planar technology. These devices have been developed for the 14nm and 10nm technology nodes, thanks to the reduced Short Channel Effects, better threshold voltage (V_T) control, better reliability, better power efficiency at high frequency operation and higher compatibility with existing CMOS technology [1-5].

In PDSOI (Partially-Depleted-SOI) devices a technique has been proposed to further improve some digital and analog parameters, called dynamic threshold (DT) MOS mode, where the front gate is connected to the body. Colinge proposed this technique in 1987 [6], as shown in figure 1. During the front-gate voltage (V_{GF}) sweep, the body bias is also increased, which dynamically reduces the V_T.

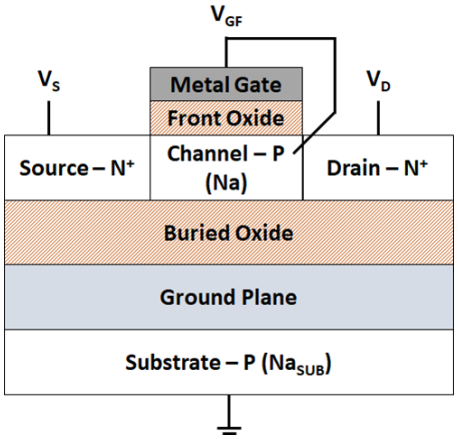

Figure 1. PDSOI schematic structure with the front gate connected with the body

This configuration brings some superior characteristics such as a higher drive current and a subthreshold swing closer to the ideal 60mV/dec [6]. However, in order to avoid a forward biased drain-channel junction, the front gate voltage cannot exceed 0.7 V [6].

In UTBB FDSOI devices, the concept of dynamic threshold mode cannot be the same as for PDSOI, due to the absence of a floating body contact. The solution for FDSOI devices, in order to apply the dynamic technique, is to connect the front gate with the back gate (substrate) [7,8]. Therefore, this technique can be applied in a promising device, with the advantages of a stronger V_{GB} coupling and the buried oxide isolation, allowing V_{GF} higher than 0.7V.

The dynamic threshold mode has been applied in 3 operation modes: the simple dynamic threshold 2 (DT2, $V_{GB} = V_{GF}$) [7,8], also known as Quasi Double Gate [7], the enhanced dynamic threshold (eDT, $V_{GB} = k*V_{GF}$, for k>1) [8,9] and the inverse enhanced dynamic threshold (inverse eDT, $V_{GF} = k*V_{GB}$, for k>1) [8,9]. Figure 2 shows the schematic structure for these 3 operation modes and the conventional operation with $V_{GB} = 0$ V.

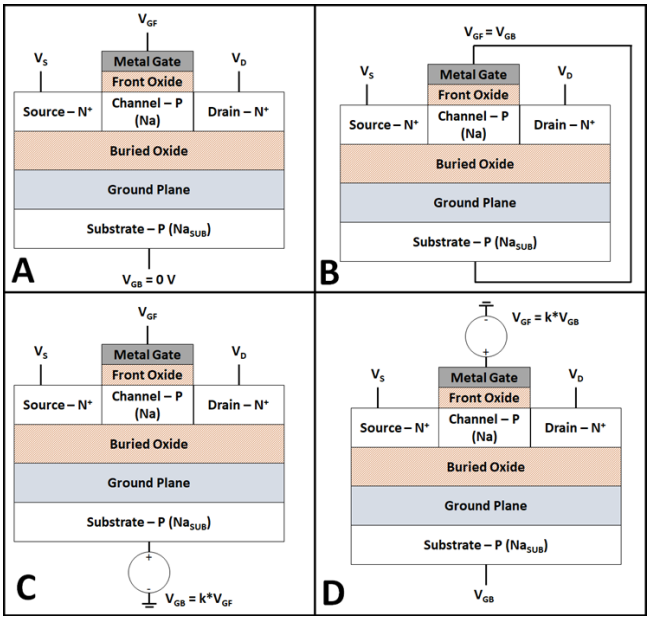

Figure 2. UTBB FDSOI schematic structure for A-) Conventional mode, with $V_{GB} = 0$ V, B-) Dynamic Threshold 2 mode, with $V_{GB} = V_{GF}$, C-) enhanced Dynamic Threshold mode, with $V_{GB} = k*V_{GF}$, D-) inverse enhanced Dynamic Threshold mode, with $V_{GF} = k*V_{GB}$.

II. Device Details

The UTBB SOI nMOSFETs studied in this work were fabricated in imec/Belgium with 20 nm of silicon film thickness (t_{Si}) and a natural doping of Na 1x10^{15} cm^{-3}. For this thickness, inversion layer quantization effects are still negligible.

The gate and buried oxides thicknesses (t_{oxf} and t_{oxb}) are, respectively, 5nm and 10nm. A midgap material, TiN, was used as gate electrode. The thickness of the front oxide is relatively high due to the fact that the devices were fabricated for application in 1T-Dynamic Random

Access Memory cells where it is necessary to have a low gate current. A p-type ground plane (GP) implantation with boron at 25keV and 5x10^{13}cm^{-2} was performed, which is considered as a back gate.

The measurements were done by Agilent B1500. The dimensions of the device are a channel length (L) of 105 nm and a channel width of 920 nm. More process information can be found in [10].

III. Physics-Based Analytical Model For Dynamic Thresold Operation Mode

In literature, there are several analytical models containing numerous equations with various parameters, that can only be solved numerically with precision [11, 12]. In this work the authors propose a simple analytical model, with only a few equations.

The well-known Lim&Fossum model [13] does not consider the potential drop at the substrate. To improve this model Martino et al. [14] proposed an analytical model taking into account the potential drop across the substrate. Also, the quantum confinement effect was taken into consideration from the variation of the silicon film thickness (t_{Si}) and front oxide thickness (t_{oxf}) [15, 16].

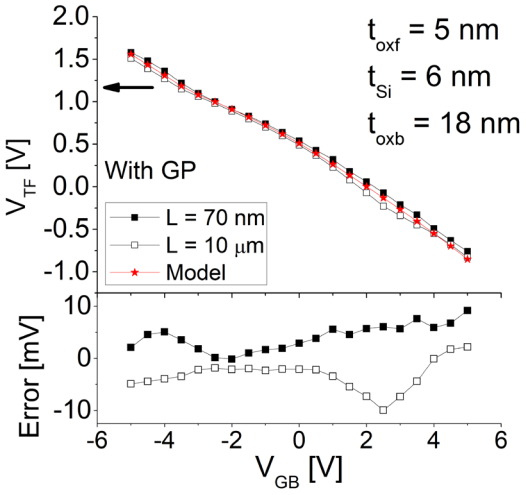

Figure 3. Experimental results with L=10µm and 70nm and analytical model for V_{TF} as a function of V_{GB} for UTBB SOI and the error between experimental data and the model [17].

Although the original model had been developed for 0.5 µm technology nodes, recent studies prove that this model remains valid to determine the threshold voltage for UTBB devices, as already reported in [17, 18, 19] and illustrated in figure 3. An important remark is that this model is only valid for devices with transistor channel length down to 70 nm [17, 18, 19].

A. The model concept

Equations [1] and [2] show the Lim&Fossum model.

$$V_{GF} = \emptyset_{MS1} - \frac{Q_{ox1}}{C_{oxb}} + \frac{qNa\,t_{Si}}{2C_{oxf}} + \left(\frac{\varepsilon_{Si}}{t_{Si}C_{oxf}} + 1\right)\emptyset_{SF} - \frac{\varepsilon_{Si}}{t_{Si}C_{oxf}}\emptyset_{SB} - \frac{Q_{inv}}{C_{oxf}} \quad (1)$$

$$V_{GB} = \emptyset_{MS2} - \frac{Q_{ox2}}{C_{oxb}} + \frac{qNa\,t_{Si}}{2C_{oxb}} + \left(\frac{\varepsilon_{Si}}{t_{Si}C_{oxb}} + 1\right)\emptyset_{SB} - \frac{\varepsilon_{Si}}{t_{Si}C_{oxb}}\emptyset_{SF} - \frac{Q_{S2}}{C_{ox2}} \quad (2)$$

Where, $\varnothing_{MS1}$ is the difference between the metal gate workfunction and the silicon film workfunction, Q_{ox1} and Q_{ox2} are the front and buried oxide charges respectively, C_{oxf} and C_{oxb} are the front and buried oxide capacitance respectively, q is the electron charge, Na is the doping concentration in the silicon film, ε_{Si} is the silicon permittivity, $\varnothing_{SF}$ and $\varnothing_{SB}$ are the potential drop at the front and back interface respectively, Q_{inv} is the inversion charge and Q_{S2} is the charge at the back interface.

The potential drop in the substrate was modeled by modifying equation (2), as shown in equation (3), and by adding equation (4).

$$V_{GB} = \emptyset_{MS2} - \frac{Q_{ox2}}{C_{oxb}} + \frac{qNa\,t_{Si}}{2C_{oxb}} + \left(\frac{\varepsilon_{Si}}{t_{Si}C_{oxb}} + 1\right)\emptyset_{SB} - \frac{\varepsilon_{Si}}{t_{Si}C_{oxb}}\emptyset_{SF} - \emptyset_{SUB} \quad (3)$$

$$\emptyset_{SUB} = \left[\frac{-\sqrt{2qNa_{SUB}\varepsilon_{Si}}}{2C_{oxb}} + \sqrt{\left(\frac{2qNa_{SUB}\varepsilon_{Si}}{4C_{oxb}^{2}} - V_{FB3}\right) + (\emptyset_{SB} - V_{GB})}\right]^{2} \quad (4)$$

Where $\varnothing_{MS2}$ is the difference between the silicon film workfunction and the substrate workfunction, $\varnothing_{SUB}$ is the potential drop in the substrate, Na_{SUB} is the doping concentration in the substrate and V_{FB3} is the flat band voltage at the third interface between the buried oxide and the substrate.

The potential drop in the substrate follows the conditions shown in equations (5) and (6).

$$\emptyset_{SUB} = 0 \rightarrow V_{GB} \geq V_{GBmax} = \emptyset_{SB} - V_{FB3} \quad (5)$$

$$\emptyset_{SUB} = 2\emptyset_{FB} \rightarrow V_{GB} \leq V_{GBmin} = \emptyset_{SB} - V_{T3} \quad (6)$$

Where

$$V_{FB3} = \emptyset_{MS3} - \frac{Q_{ox3}}{C_{oxb}} = \frac{kT}{q}\ln\frac{Na}{Na_{SUB}} - \frac{Q_{ox3}}{C_{oxb}} \quad (7)$$

$$V_{T3} = V_{FB3} + 2\emptyset_{FB} + \frac{\sqrt{2qNa_{SUB}\varepsilon_{Si}2\emptyset_{FB}}}{C_{oxb}} \quad (8)$$

Where Q_{ox3} is the substrate charge, k is the Boltzmann constant, T is the temperature in kelvin, and V_{T3} is the threshold voltage for the third interface.

The quantum confinement generates no current conduction at the front interface, but at a distance x_c from the front interface [12, 13]. For this reason, the value of x_c can be calculated using equation (9), where A_C and B_C are model parameters:

$$\frac{x_c}{t_{Si}} = A_C \exp\left(\frac{V_{GB}}{B_C}\right) \quad (9)$$

where $A_C = 0.05$ and $B_C = 3.1$.

Due to this effect the effective value of the silicon film thickness ($t_{Si,eff}$) and front oxide thickness ($t_{oxf,eff}$) are determined by equations (10) and (11):

$$t_{Si,eff} = t_{Si} - \frac{\varepsilon_{ox}}{\varepsilon_{Si}}x_c \quad (10)$$

$$t_{oxf,eff} = t_{oxf} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}}x_c \quad (11)$$

The equation (9), (10) and (11) and the values of A_C and B_C were extracted from the literature [12,13].

B. Applying the model in Dynamic Threshold mode

There are two different ways to extract the threshold voltage using the analytical model. One is by calculations and the other one is by a graphical approach.

By calculating

In dynamic mode equation (12) or (13) is added to the model.

$$V_{GB} = k * V_{GF} \quad (12)$$

$$V_{GF} = k * V_{GB} \quad (13)$$

Equation (12) represents the DT2 mode for k = 1. When the value of k is higher than 1 (k>1) equation (12) represents the enhanced DT mode. Equation (13) represents the inverse eDT mode, for k>1, however, to facilitate the application in the analytical model, equation (13) can be rewritten as equation (14).

$$V_{GB} = \frac{1}{k} * V_{GF} \quad (14)$$

The first step to calculate the threshold voltage by this model is to define a value for V_{GB} and insert it in equations (3), (4) and (9). The next step is to calculate the effective value of $t_{Si,eff}$ and $t_{oxf,eff}$ in equations (10) and (11). By mathematical iteration, the value of $\varnothing_{SUB}$ is calculated using equations (3) and (4). Finally, the value of V_{TF} is obtained by equation (1). These are the steps to calculate the threshold voltage in the conventional operation mode.

In dynamic mode, the value of V_{TF} calculated in equation (1) is based on using V_{GF} of equation (12) or (14). Followed by choosing a value of k, in this step the dynamic threshold voltage mode is determined and a new value of V_{GB} is calculated

The new value of V_{GB} is inserted in equations (3), (4) and (9), and the process is repeated until equation (12) or (14) converges.

By the graphical approach.

From the V_T x V_{GB} curve calculated from the analytical model, it is possible to determine the value of V_T for UTBB devices operating in: DT2, eDT and inverse-eDT modes.

In the DT2 mode, the value of V_T is extracted from the $V_{GB} = V_{GF}$ condition as previously mentioned. In figure 4 the straight line represents the analytical model of V_T as a function of V_{GB}, the dotted line represents the $V_{GF} = V_{GB}$ curve and the intersection point between the curves represents the V_T value for the DT2 mode.

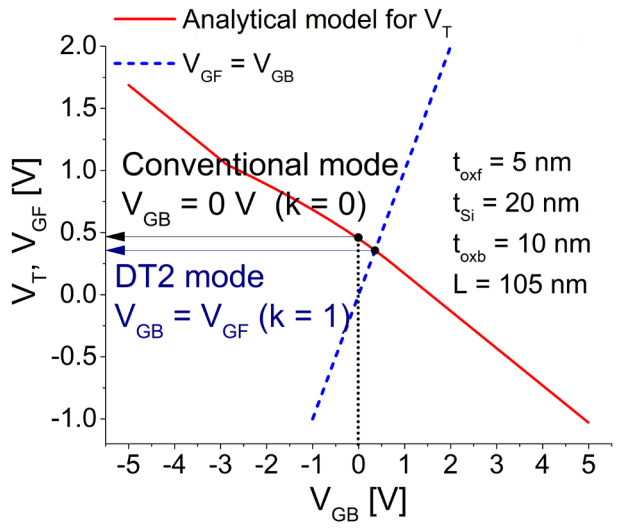

Figure 4. Straight line represents the analytical model of the front threshold voltage as function of back gate voltage, the dotted line represents the $V_{GF} = V_{GB}$ curve. The values of V_T for k = 0 and k = 1 are indicated.

The same reasoning used for the DT2 mode is adopted for eDT and inverse eDT modes. In figure 5 the straight line represents the analytical model V_T as a function of V_{GB}, and the dashed lines are related to the following conditions: $V_{GB} = k*V_{GF}$ and $V_{GB} = (1/k)*V_{GF}$, for k = 2. These curves represent the enhanced DT and the inverse enhanced DT operation modes, respectively. For the eDT mode the V_T of the DT UTBB SOI device is the value of V_{GF} at the intersection point (y-axis). In case of inverse eDT, the V_T is represented by the value of V_{GB} at the intersection (x-axis). In inverse eDT mode, the device operates in a condition that the back interface inverts earlier than the front interface. For this reason the value of the inverse e-DT threshold voltage is the V_{GB}. The same analysis was done for different values of k.

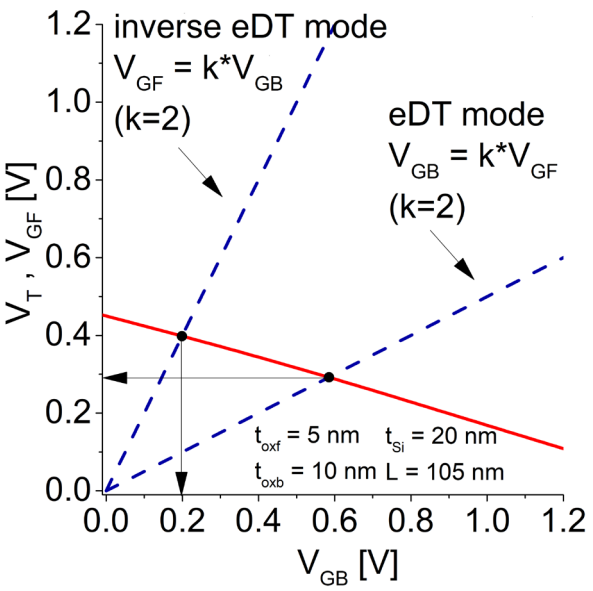

Figure 5. Straight line represents the analytical model of the front threshold voltage as function of back gate voltage, the dashed lines represent $V_{GF} = k*V_{GB}$ (inverse eDT mode) and $V_{GB} = k*V_{GF}$ (eDT mode) curves for k=2.

IV. Comparison Between Model and Experimental Data

The V_T as a function of V_{GB} obtained experimentally is compared with the analytical model in figure 6.

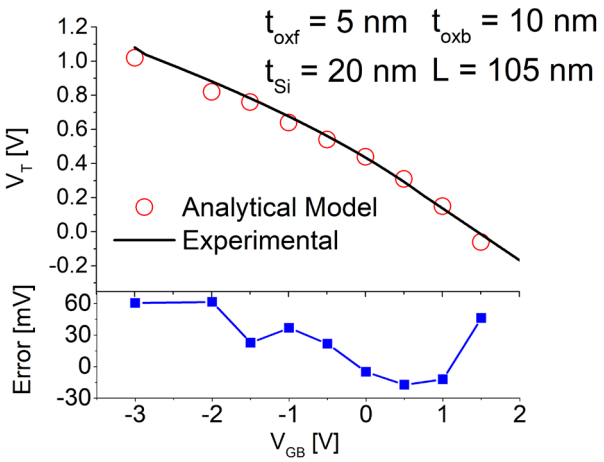

Figure 6. Experimental results and analytical model for V_T as a function of V_{GB} for UTBB SOI with GP. and the error between experimental data and the model.

It is possible to see a good agreement between experimental results and analytical model in figure 6, proving that this model is useful to extract the V_T of UTBB SOI devices with these dimensions.

The value of V_T obtained from figures 4 and 5 is compared with experimental data shown in figure 7. A good agreement is observed for these conditions. In figure 7, for k=0, the operation mode of the transistor is the conventional mode, (figure 6) where V_{GB} = 0V.

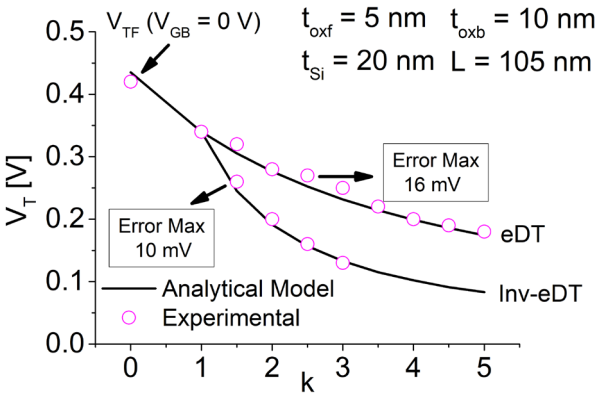

Figure 7. Experimental results and analytical model for V_T of DT2 UTBB SOI nMOSFET as function of k.

V. Influence of Variation of Device Thickeness

Year by year, the ultrathin devices become thinner due to the technology evolution. The following analysis shows the relation of variations of the thickness of the front and buried

oxide and also the silicon film on the threshold voltage for the different dynamic operation modes.

Figure 8 shows the analytical threshold voltage as a function of back gate bias for the device studied (t_{oxf} = 5 nm, t_{Si} = 20 nm and t_{oxb} = 10 nm), called reference device, and three other devices reducing the thickness of the front oxide to 2 nm, the silicon film to 10 nm and the buried oxide to 5 nm.

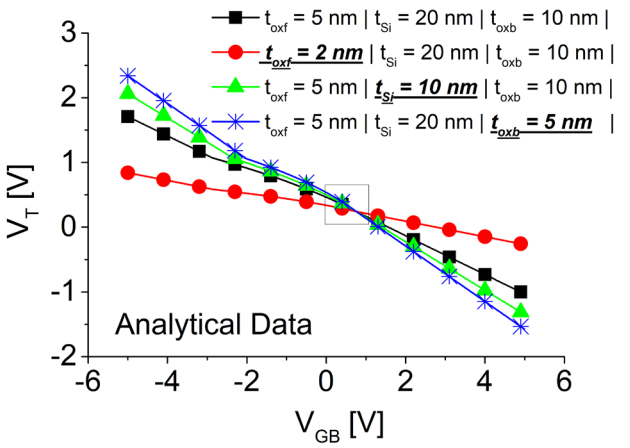

Figure 8. Analytical threshold voltage as a function of back gate bias for 4 different devices.

In figure 8 one can observe that the behavior of the threshold voltage when the back gate varies from -5 V to 5 V is changed for a different thickness of the device layers. To extract the dynamic threshold voltage, the graphic approach will be used.

Figure 9 shows the blow up of figure 8 for V_{GB} and V_T, V_{GF} varying from 0 V to 1V. The straight lines represent the same curves presented on figure 8 and the dashed lines are related to the following conditions: $V_{GB} = V_{GF}$, $V_{GB} = k*V_{GF}$ and $V_{GF} = k*V_{GB}$, for k = 2, 3 and 4.

Analyzing figure 9, it is possible to see that for the inverse enhanced DT mode, the threshold voltage suffers a little change when varying the thickness of the device layers. The same behavior happens for the DT2 operation mode.

However, for the enhanced DT mode, the values of the threshold voltage are very similar when varying the thickness of the device layers. The reduction of the front oxide thickness causes a higher variation in threshold voltage, as observed in figure 8.

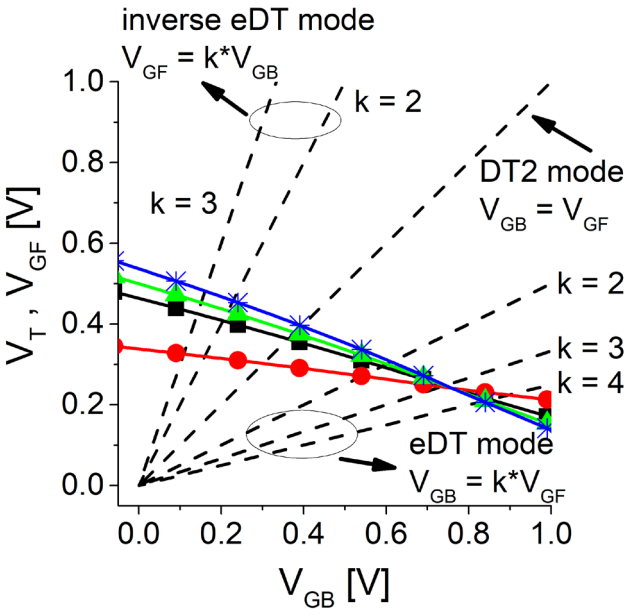

Figure 9. Straight lines - Analytical threshold voltage as a function of back gate bias for 4 different devices. Dashed lines - $V_{GF} = V_{GB}$ (DT2) ,$V_{GF} = k*V_{GB}$ (inverse eDT mode) and $V_{GB} = k*V_{GF}$ (eDT mode) curves for k=2 to 4.

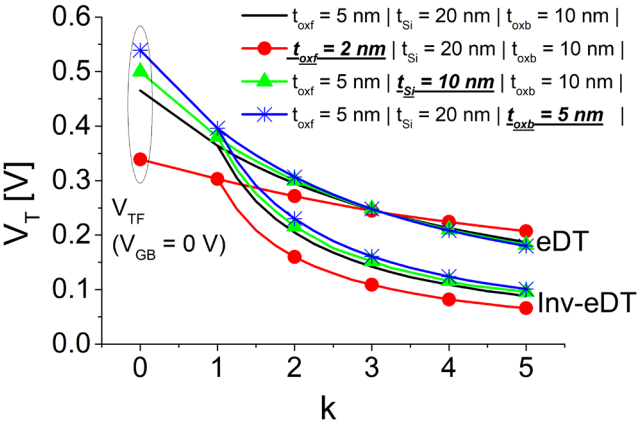

Figure 10. Analytical threshold voltage as a function of k for 4 different devices.

Analyzing the conventional mode (k=0), as expected the reduction of the front oxide thickness decreases the value of the threshold voltage, but the opposite behavior is observed when reducing the silicon film and buried oxide thickness.

When the front oxide thickness becomes smaller, the oxide barrier decreases, thus the voltage required to invert the front interface decreases. As predicted from figure 9, for the eDT mode, the behavior shown in figure 10 is very similar when the thickness of the device layers are reduced.

VI. Conclusions

This paper presents an analytical model of the substrate influence on Dynamic Threshold UTBB SOI devices with different operation modes like enhanced mode (eDT) and inverse eDT mode.

The modeling of the dynamic threshold mode presents two ways to determine the threshold voltage, i.e., by calculation and by graphics. Both ways give the same results and can be applied in this analysis.

The simple analytical model considering the quantum confinement in devices with a ground plane presents a good agreement with experimental results, proving that the simple analytical model with only a few equations can be useful for UTBB devices.

Considering the analysis in threshold voltage as function of back gate bias, the maximum error between model and experimental is lower than 60mV. For the analysis of the enhanced dynamic threshold, an error lower than 16 mV is obtained between the model and the experimental results. For the inverse enhanced dynamic threshold mode this error is lower than 10 mV.

Nowadays, the reduction of the layer thickness of the devices is one of the technological challenges. The reduction of the front oxide thickness can provide a different behavior of the threshold voltage, depending on the DT operation mode. However, the thinning of the buried oxide and the silicon film thickness does not give significant changes in threshold voltage for both DT2 and eDT operation modes.

Acknowledgments

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