Impact of the Nitrogen Concentration of Sub-1.3 nm Gate Oxides on 65 nm Technology Transistor Parameters

A.L.P. Rotondaro, R.T. Laaksonen, and S.P. Singh

Silicon Technology Development, Texas Instruments Incorporated, Dallas, TX, 75243, USA e-mail: antonio@ti.com

ABSTRACT

The nitrogen concentration of ultrathin gate oxides (sub-1.3 nm) was varied in a wide range (from 13 % to 23 %). The threshold voltage and the channel carrier mobility of advanced 65 nm technology CMOSFET transistors fabricated with these oxides were analyzed. It was observed that increasing the nitrogen concentration in the gate oxide results in a negative shift of the threshold voltage for both NMOS and PMOS devices and a degradation of the hole mobility. It was also observed that p-channel transistors are more sensitive to the nitrogen concentration of the gate oxide than n-channel transistors.

Index Terms: Gate Oxide, Nitridation, Threshold Voltage, Mobility.

1. INTRODUCTION

Silicon dioxide has been one of the key materials to enable the booming of the semiconductor industry. Scaling of the gate dielectric thickness for advanced technologies has reached values below 1.5 nm [1]. To overcome gate leakage and boron penetration limitations, alternative gate dielectrics to SiO_2 have been implemented [2, 3]. In most approaches, silicon oxy-nitride (SiO_xN_y) layers are used as gate dielectric. The nitrogen content of the SiO_xN_y gate dielectric is a key parameter that controls boron penetration, reliability and electrical characteristics of the gate dielectric [4, 5]. In this paper, we present the effect of the nitrogen content of ultrathin SiO_xN_y gate dielectrics on the threshold voltage and carrier mobility of advanced 65 nm technology CMOSFETs.

2. EXPERIMENTAL

Ultra-thin (sub-1.3 nm) gate oxides were fabricated in a cluster tool on 200 mm <100> silicon wafers after a pre-oxidation cleaning in NH₄OH: H_2O_2 :H₂O followed by H_2SO_4 :H₂O₂. The fabrication sequence comprises a base oxide growth in N₂O:H₂ ambient at 950 °C in a lamp heated rapid thermal process chamber [6,7]; transfer under low pressure (10 torr, nitrogen purged) to a plasma nitridation chamber where the power and duration of the plasma process were varied to achieve the desired nitrogen concentration in the gate dielectric [3, 4]; transfer under low pressure to a rapid thermal anneal chamber for a post nitridation anneal in an oxygen ambient at 900 °C for 15 seconds and finally the wafers were transferred under low pressure to a polysilicon deposition chamber where they received 1000 Å polysilicon gate electrode deposition. Pilot wafers were processed in a similar manner but skipped the polysilicon deposition step. These pilot wafers were used for physical characterization to determine the nitrogen concentration in atomic % of the gate dielectric films by x-ray photoelectron spectroscopy (XPS) [8]. Since changes in Cox result in changes on the threshold voltage [9], the gate dielectrics were fabricated to ensure that all films had an equivalent oxide thickness in the range of 1.18 +/- 0.04 nm. The nitrogen concentration was varied in the range of 13 % to 23 %.

Advanced (65 nm technology) CMOSFET transistors [10] were fabricated with the different gate oxides. The devices were characterized after 2 levels of copper metallization and all the standard transistor parameters were measured for devices with channel width (W) of 1 μ m and gate length (Lg) from 30 nm to 10 μ m.

The MOSFET linear and saturation threshold voltages were measured using the maximum transconductance method [9].

The mobility of devices with gate length in the range of 50 nm to 100 nm was extracted from the lin-

ear drain current at 1 V gate bias for NMOS (-1 V for PMOS) using the method described by Singh [11]. The mobility value obtained is a good indication of the carrier mobility of short channel devices operating in saturation, as it is measured at high gate effective field.

3. RESULTS AND DISCUSSION

The saturation threshold voltage of the transistors presented a strong dependence with the nitrogen concentration in the gate dielectric (Fig. 1a and 1b). The PMOS devices presented a higher sensitivity to the nitrogen concentration in the gate dielectric (Fig. 1a) than the NMOS transistors (Fig. 1b). For both transistor types the increase of the nitrogen concentration in the gate oxide led to a negative voltage shift of the threshold voltage. This corresponds to a decrease of the threshold voltage of the NMOS transistors and an increase of the absolute value of the threshold voltage of the PMOS transistors. This phenomenon can be understood when considering that the presence of nitrogen in the gate oxide will correspond to a change in the net charge in the gate dielectric, affecting the threshold voltage of the transistors.

The dependence of the long channel devices $(Lg = 1 \ \mu m)$ threshold voltage with the nitrogen concentration in the gate dielectric (Fig. 2a and 2b) can be modeled by equations (1)-(4). These equations provide the threshold voltage in the linear (Vtl) and saturation (Vts) regimes when the nitrogen concentration in the gate oxide (c_N %) is varied and can be used to predict the threshold voltage of the devices once the nitrogen concentration of the dielectric is known.

PMOS Vtl (V) = $-0.0045 - 0.0244 c_N\%$, Rsq = 0.982	(1)
PMOS Vts (V) = $0.0368 - 0.0240 c_N$ %, Rsq = 0.986	(2)
NMOS Vtl (V) = $0.3119 - 0.0075 c_N\%$, Rsq = 0.920	(3)
NMOS Vts (V) = $0.2547 - 0.0073 c_N\%$, Rsq = 0.953	(4)

A close inspection of equations (1)-(4) shows that the coefficient of Vt change with c_N % is similar for the Vtl and Vts of a given device. On the PMOS-FET case it is -24.2 mV/N% and for NMOS it is -7.4 mV/N%. This is in agreement with the proposed mechanism where the threshold voltage shift is a result of the change in the net charge in the gate dielectric by the introduction of nitrogen. The fact that the PMOS Vt is more affected than the NMOS Vt by the nitrogen concentration of the ultrathin gate dielectric can be understood when considering that the nitrogen introduction increases the concentration of fixed charges (Qf) and interface charges (Qit) of the gate dielectric. For both PMOS and NMOS devices, Qf has a positive charge value. However, Qit has different polarity depending on the device studied. In the case of PMOS, Qit has positive charge value and in the case of NMOS Qit has negative charge value at flatband [12]. This means that for the PMOS devices both Qf and Qit have positive charge value and will have an additive effect when shifting the Vt. On the other hand, for the NMOS devices, the negatively charged Qit partially compensates the effect of the positively charged Qf and the net Vt shift is reduced relative to the one seen for PMOS.

The short channel mobility at high effective field was plotted as a function of the source current of the device in the subthreshold region (Fig 3a and 3b). This approach for comparing the mobility of short channel devices eliminates the variability related to the effective gate length of the devices resulting in a more accurate analysis. The hole mobility (Fig. 3a) showed to be affected by the nitrogen content of the gate dielectric whereas the electron mobility (Fig. 3b) appears to be less sensitive to this parameter. The hole mobility reduction with the increase of the nitrogen concentration in the gate dielectric can also be related to the change in the net charge in the gate dielectric.



Figure 1: Saturation threshold voltage as a function of the reciprocal of the gate length for MOSFET devices with different nitrogen concentration in the gate dielectric. a) PMOSFET devices; b) NMOSFET devices.



Figure 2: Threshold voltage of long channel MOSFETs ($Lg = 1 \ \mu m$) as a function of the nitrogen concentration in the gate dielectric for NMOSFETs (solid lines) and PMOSFETs (dashed lines). a) Linear Threshold voltage; b) Saturation Threshold voltage.



Figure 3: Channel carrier mobility as a function of the source current in the subthreshold region for MOSFETs with different nitrogen concentration in the gate dielectric. a) Hole mobility on PMOSFETs; b) Electron mobility on NMOSFETs.

The results indicate that the additive charge introduced by Qf and Qit in the case of PMOS led to significant Coulomb scattering that degraded the hole mobility. In the case of NMOS, the reduced charged Qit minimizes the effects of the positively charged Qf and the net impact on the electron mobility is very small.

Even for the short channel devices studied (50 nm to 100 nm), it is possible to notice that the mobility increases as the source leakage in the subthreshold region decreases (Fig. 3a and 3b) indicating that the carrier mobility is higher for devices with longer channels. This can be understood by taking into account that the long channel devices have an overall lower channel doping concentration compared to the short channel devices. (i.e. the use of pocket implants to control short channel effects increase the channel doping concentration and consequently reduces the carrier mobility in the short channel transistors).

4. CONCLUSIONS

In this paper the effect of the nitrogen concentration in ultrathin gate dielectrics on the threshold voltage and carrier mobility of 65 nm technology MOSFETs has been presented. The increase of the nitrogen concentration in the gate dielectric from 13 % to 23 % results in a negative shift of the threshold voltage for both NMOS and PMOS transistors. The magnitude of the shift is three times higher for the PMOS-FET devices compared to the NMOSFET devices. The carrier mobility is also affected by the changes in the nitrogen concentration of the gate dielectric. The hole mobility is significantly reduced with the increase of the nitrogen concentration whereas the electron mobility remains almost unaffected for the concentration range investigated. It is proposed that the observed effects are a result of changes in the net charge present in the gate dielectric with the introduction of nitrogen.

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