Plasma Etching of Polycrystalline Silicon using Thinning Technology for Application in CMOS and MEMS Technologies

A. M. Nunes[1,2], S. A. Moshkalev[2], P. J. Tatsch[1,2] and A. M. Daltrini[2,*]

[1] School of Electrical and Computer Engineering, FEEC-UNICAMP, UNICAMP, Campinas, SP, Brazil
[2] Center for Semiconductor Components, CCS-UNICAMP, UNICAMP, CP 6061, CEP 13083-970, Campinas, SP, Brazil
* Present address: CEITEC, CEP 91501-970, Porto Alegre, RS, Brazil
e-mail: alcinei@ccs.unicamp.br

ABSTRACT

This work presents results of the study of profile evolution for Si-poly structures during plasma etching using the thinning technology in $SF_6/CF_4/CHF_3$ gas mixtures. Structures with an aspect ratio (height/width) up to 5, widths end in the range of 0.3 – 0.1 μm and 0.3μm thick, were produced. Si-poly structures with high anisotropy (anisotropy factor up to 0.92-0.98) after etching were demostrated. The method can be used for fabrication of sub-micron Si-poly gates in CMOS and in fabrication of MEMS devices.

Index Terms: Thinning Technology, Reactive Ion Etching, Plasma Etching, Anisotropy Factor, Etch Selectivity.

1. INTRODUCTION

Polycrystalline silicon films are used in CMOS technologies to fabricate transistor gates. The main requirements for the polysilicon gate etching are: high etch selectivity for the underlying layer (silicon oxide), highly anisotropic etch profile, and low surface damages (structural and electrical defects) [1,2]. For fabrication of MEMS devices, high aspect ratios, anisotropic profiles and low surface damage are basic requirements [3]. In the Si-poly etching using a reactive ion etching (RIE), a reasonable trade-off between different requirements can be achieved by a proper choice of the etching chemistry.

For this, a hybrid process which consist of two etching steps can be recommended. Basically, in the first step (main etch, until reaching the oxide film), a smaller pressure and thus higher ionic bombardment was used, resulting in more anisotropic profiles. In the second step (final stage of the Si-poly film etching and overetch), a higher pressure was used, leading to a higher selectivity over oxide and lower roughness. Further improvement of the etch profile during the thinning of the Si structure was reached during this stage [4].

It is important to note that etching of Si-poly films by fluorine occurs spontaneously, with the main etch product being SiF_4. Thus, the presence of gases that inhibit lateral etching through sidewalls passivation or polymerization is usually required. Chlorine and bromine containing mixtures are the best choice for nanoscaled devices [5], as these halogens are known to inhibit strongly the lateral etching. For fabrication of sub-micron structures using fluorine chemistry, polymerizing gases, frequently with addition of oxygen, are usually employed to passivate sidewalls [6]. Directionality of the RIE process is determined by a strong ion bombardment of the sample, that removes unsaturated etch products from the bottom surface.

Strong polymerizations on the sidewalls in the mixtures with gases like CF_4, CHF_3 or C_4F_8 can be efficient in reduction of undercut required for highly directional vertical etching [7]. On the other hand, controlled lateral etching (with the lateral etch rate strongly reduced as compared with the vertical etching) might be interesting for some applications in MEMS and CMOS technologies. For example, in fabrication of suspended structures in MEMS devices, plasma etching of monocrystalline Si (polycrystalline Si sacrificial layer) can offer some advantages over conventional wet etching, which frequently causes collaps of the structures like cantilevers in the final (drying) stage of the process. In a CMOS technology, controlled lateral etching during the overetch step can result in considerably thinner Si-poly structures as

compared with the patterns prepared by an optical lithography, see for example [8], where gate widths of 10nm were obtained using a thinning (it was called notching in [8]) technology in high density reactors. This thinning technique might be an interesting alternative for small research laboratories, where still exists a great number of lithography devices with ~ 1 μm minimum resolution. The thinning technology developed in the present work, is able to produce structures as narrow as 0.1 – 0.3 μm using conventional photolithography. Sub-micron structures with high aspect ratio and vertical sidewalls have been obtained using optical lithography and fluorine based plasma etching in a conventional RIE reactor.

2. EXPERIMENTAL

The polysilicon films were deposited by CVD in a low pressure vertical pancake type reactor on 0.9μm thick oxide films. The oxide films were thermally grown in a conventional furnace at the temperature of 1000°C on *n*-type single crystal Si (100) wafers. The sequence of the stages for oxide grown are presented in Table I.

Before the growth, the standard RCA method was used for samples cleaning [9]. The characteristics of the process and the polysilicon film are shown in Table II. For more details can be found somewhere [10].

A conventional photolithography process was used for a pattern transfer to the wafer, employing the Karl Suss MBJ3 mask aligner. The lithography patterns were lines with spacing varying from 5 to 125 μm. The resist and the developer used were AZ5214 and MIF312, respectively. The etching system used in this work was a capacitively coupled parallel plates reactor operating in a RIE mode with 6cm inter-electrode gap. The samples (~0.5x0.5cm size) wafers were put on the lower RF (13.56 MHz) powered electrode (12cm diameter). The upper electrode is connected with the walls, being at the ground potential. The gases mixtures used for etching were: $SF_6/CF_4/CHF_3$ and $SF_6/CF_4/N_2$. The pressure was varied from 50 to 150 mTorr, the power from 30 to 85 W and DC self bias voltage from 6 to 300V.

Table I. Procedure for wet oxidation before the deposition of Si-poly (T=1000°C).

Stages	Environment	Time (min)
1	N_2	>3
2	N_2	30
3	O_2	10
4	$O_2 + H_2O$	180/240
5	N_2	10
6	N_2	>3

Table II. Characteristics of the polysilicon film.

Mixture	SiH_4/H_2
Flow	40/4800 sccm
Pressure	5 Torr
Temperature	800°C
Time	5 – 60 min
Thickness	0.3 – 5μm
Deposition rate	60 – 80nm/min
Refractive Index	3.9 – 4.15
Grain Size by XRD	~21 nm

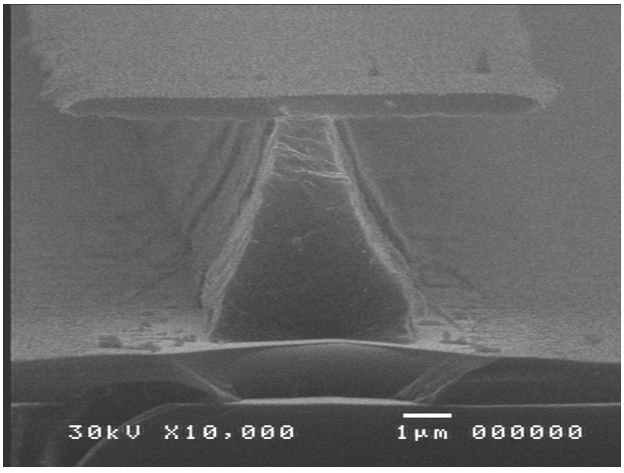
3. RESULTS AND DISCUSSION

A. Etching in $SF_6/CF_4/CHF_3$ mixtures

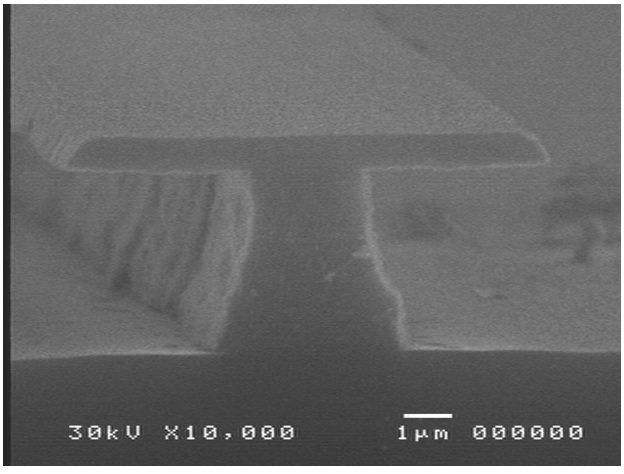
Neat SF_6 plasmas are known to etch silcion very fast. For example, in our experiments, the vertical Si etch rate (*ER*) as high as 1.2 μm/min was achieved at a pressure of 100 mTorr, RF power of 50 W and the SF_6 flow of 7 sccm. The etch selectivity over silicon oxide as high as $S = 100$ was obtained. However, the etch profile is isotropic ($A \sim 0.2$) due to relatively fast lateral etching. In order to improve the anisotropy, additions of polymerizing gases like CF_4 and/or CHF_3 are necessary. Some examples of etch profiles in a 4 μm thick Si-poly film, obtained for SF_6 mixtures with CF_4 and CHF_3 during the overtech phase, are shown in Figure 1. As can be seen by comparing the Figures. 1 a and b (without and with CHF_3, respectively), addition of CHF_3 is more efficient that of CF_4 in reduction of the lateral etch rate and controlling the etch profile. Notable reduction of the lateral etch rate (especially for the upper part of the Si structure) is observed, indicating strong passivation effect of CHF_3. Moreover, this effect is apparently different for the upper and lower parts of the etched structure, resulting in considerable improvement of the anisotropy factor (from 0.60 to 0.86).

B. Effect of pressure

As shown in Figure 2, the etched profiles obtained with $SF_6/CF_4/CHF_3$ mixtures, improve considerably with pressure (anisotropy factor changes from 0.83 to 0.98 as the pressure grows from 50 to 150 mTorr). It can be seen also that the lateral etch rate tends to saturate as the pressure rises above 100 mTorr. An example of highly anisotropic profile obtained under high pressure conditions is shown in Figure 3. In this work, the anisotropy factor, under the thinning conditions (A_t), is determined in another way (see Appendix) as compared with the conventional definition.



(a)



(b)

Figure 1. SEM images of the polysilicon profile after etching. Process conditions: Si-poly thickness of 4 µm, 100mTorr, 50W, 21 min. a) SF6/CF4/CHF3 = 1.5/5/0, total flow 13 sccm, 103V, ER=430nm/min, ER_{LU}=211nm/min, ER_{LL}=135nm/min, A_t=0.60, S~35; b) SF6/CF4/CHF3 = 1.5/5/2, total flow 17 sccm, 114V, ER=358nm/min, ER_{LU}=180nm/min, ER_{LL}=150nm/min, A_t=0.86, S~30.

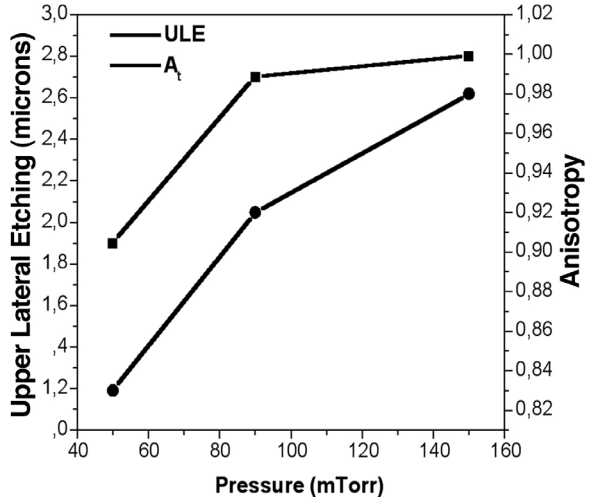


Figure 2. Upper lateral etching and anisotropy factor vs. pressure in $SF_6/CF_4/CHF_3$ plasma. Conditions: $SF_6/CF_4/CHF_3$ = 3/10/4 sccm, 50W, 72-262 V, 8.5min.

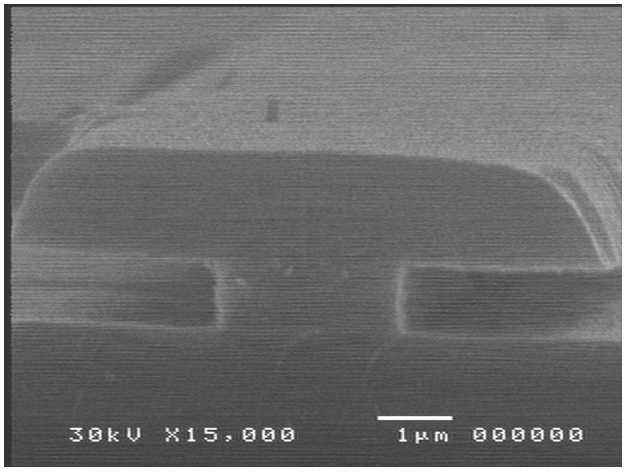


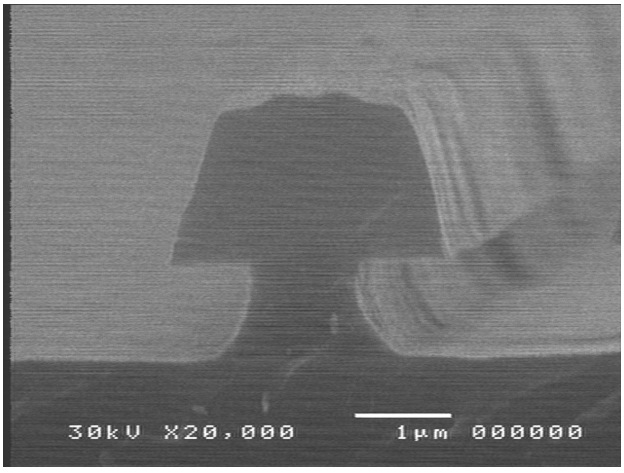
Figure 3. SEM image of the polysilicon profile after etching. Process condition: SF6/CF4/CHF3 = 1.5/5/2, total flow 17 sccm, 150mTorr, 50W, 72V, 8.5min, ULE=2.8µm, LLE=2.8µm, A_t=0.98, S~40.

C. Profile evolution during the thinning stage

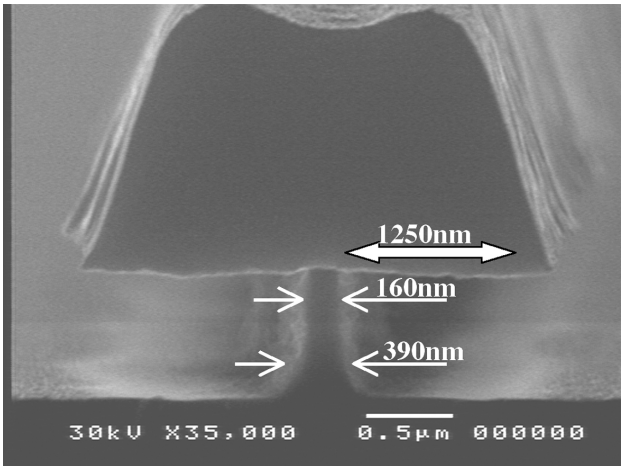
In the beginning of the thinning stage, a characteristic concave etch profile frequently can be observed, see Figure 4a, where the results for a 1µm thick Si-poly film etching are shown. After 2 minutes long overetch step, the Si-poly structure was thinned up from 2.8 µm to 0.16 µm in the upper part and 0.39 µm at the bottom, see Figure 4b.

More detailed data on the profile evolution during the thinning stage have been obtained for the case of a 4 µm thick Si-poly etching.

In Figure 5, the temporal evolution of the anisotropy factor, lateral etching (for the top of the Si structure) and etch profile, is shown. It is possible to see a dramatic change of the etching regime at the end of the main etch stage, corresponding to about 12 minutes of etching. After this, the etch profile starts to change from a concave to a flatter one, since the etching at the bottom of the Si structure (LLE) is notably faster than that at the top (ULE). This is likely due to enhanced transport of etching species (mainly, F radicals) along the surface of the oxide due to diffusion. Note that before the oxide surface is reached (the main etch stage), the surface transport of fluorine along the silicon surface is reduced, as the fluorine radicals are readily adsorbed/trapped in the Si surface layer and consumed in the etching process. As the interaction of fluorine radicals with the oxide is much weaker, their fast diffusion along the oxide surface (to the bottom of the Si structure) is possible. This results in acceleration of the lateral etching at the bottom (from 140 nm/min to 180 nm/min) and fast improvement of the anisotropy factor observed immediately after the beginning of the overetch stage (from ~0.55 to 0.75 in about 3 minutes).



(a)



(b)

Figure 4. SEM images of the polysilicon profile after etching. Process conditions: SF6/CF4/CHF3 = 1.5/5/2, total flow 17 sccm, 100mTorr, 50W, 104V. a) 3min, ULE=0.93μm, LLE=0.5μm, A_t=0.63; b) 5min, ULE=1.24μm, LLE=1.16μm, A_t=0.85.

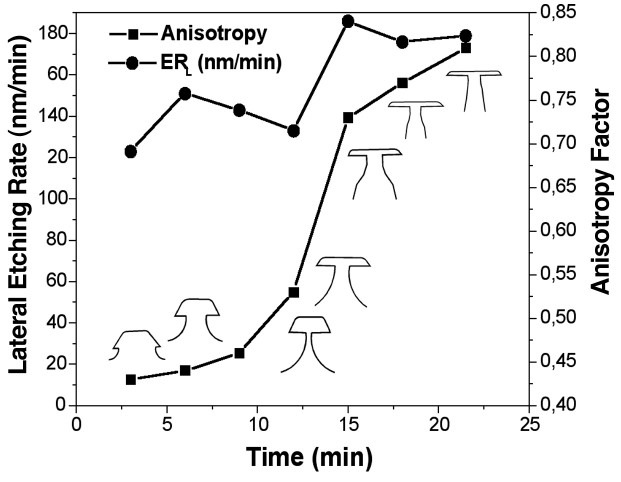


Figure 5. Temporal evolution of the upper lateral etching (ULE) and anisotropy factor in $SF_6/CF_4/CHF_3$ plasma for 4μm thick Si-poly. Conditions: $SF_6/CF_4/CHF_3$ = 3/10/4 sccm, 100mTorr, 50W, 100-114V.

Etch profiles for different stages of the process presented in Figure 5, are shown in Figure 6 a - e.

D. Thickness Variation

Additional experiments were carried out in order to illustrate the effect of the Si-poly layer thickness on the etch profile evolution. For this, etching was carried out for the same time (9 minutes), for 4 samples of Si-poly with different thickness (4, 1, 0.7 and 0.3 μm), see Figure 7. It is important to note that the lateral etch rate grows strongly as the oxide layer is reached (compare the Figure 8 a and 8 b where the ULE is equal to 1.31 and 2.56 μm). This indicates that when the oxide surface is reached, it serves as a secondary source of fluorine radicals as they diffuse along the oxide surface (LLE, lower lateral etching) or are desorbed from the surface and adsorbed in upper parts of the ecthing profiles (ULE, upper lateral etching).

As can be seen by comparison of Figure 8 a and Figs. 8 b,c, the anisotropy improves strongly after the end of the main etch stage. This gives further support to the hypothesis of enhanced transport of etching species along the oxide surface. With further reduction of the Si-poly layer thickness, the ULE value changes only slightly (compare Figs. 8 b and c). Another interesting observation is that for thinner layers, the difference between etching at the top and bottom of the structure becomes smaller.

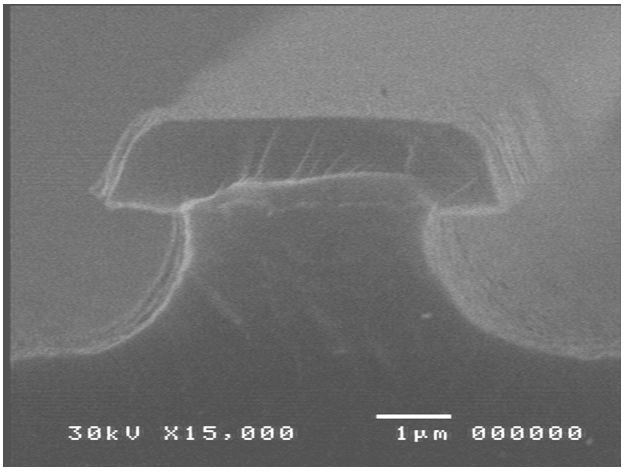
E. High aspect ratio Si-poly structures

Under the conditions of the thinning process developed here, it was possible to obtain reproducibly the Si-poly structures with minimum width in the range of 150-300 nm. Thinner structures could be obtained as well, however the reproducibilty was poor. As an example, Figure 9 shows a 1 μm high Si structure with the minimum width of about 65 nm in the middle of the structure (arrow 1) while at the bottom the width is about 200 nm (arrow 2). Thus the structure aspect ratio is better than 5.

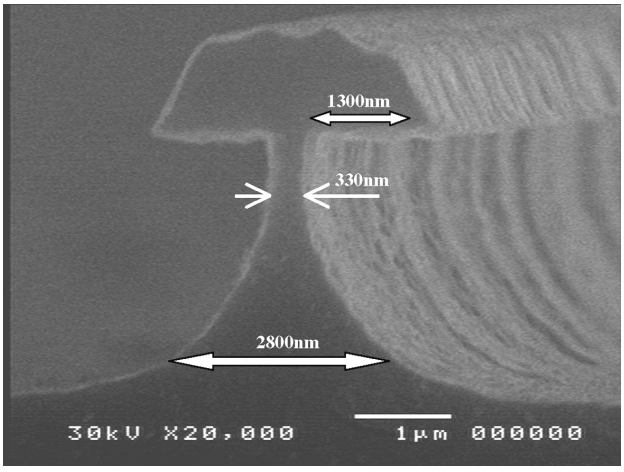
F. 300nm thick Si-poly structures

While the 4μm thick films etching study is helpful for better understanding of the phenomena involved and the dynamics of etching (and for MEMS applications), for fabrications of CMOS transistor gates, so fine Si-poly films with as low as 300nm [11].

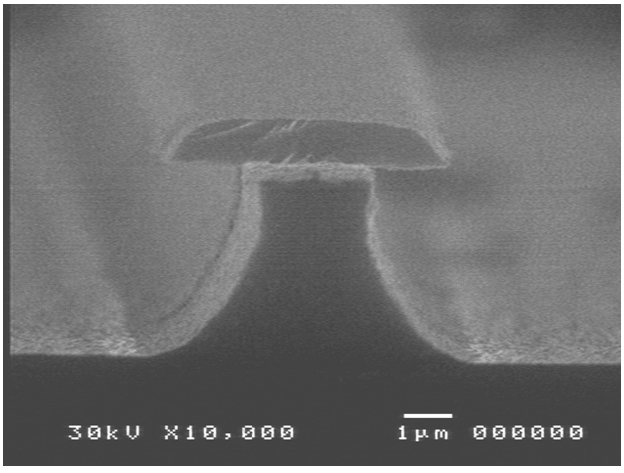
The Figs. 10 a and b, show images of the 300nm thick Si-poly after 7.5 minutes etching. Under thinning conditions, i.e., after reaching the oxide, the greater the thickness, the greater is the etching rate (ER=284nm/min, for 1μm thickness, see Figure 7). In Figs. 10 a and b, the etch rate was considerably



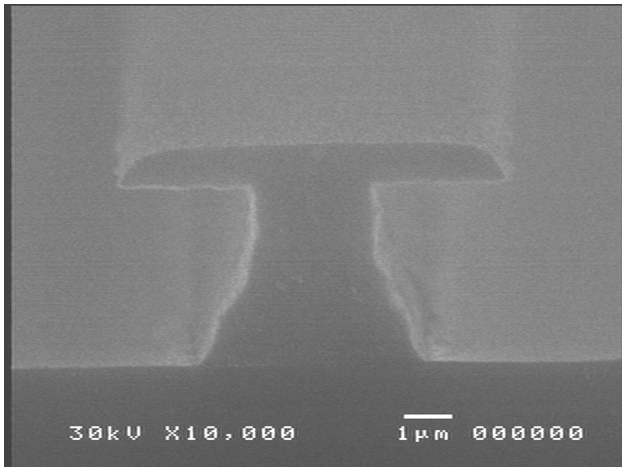
(a)



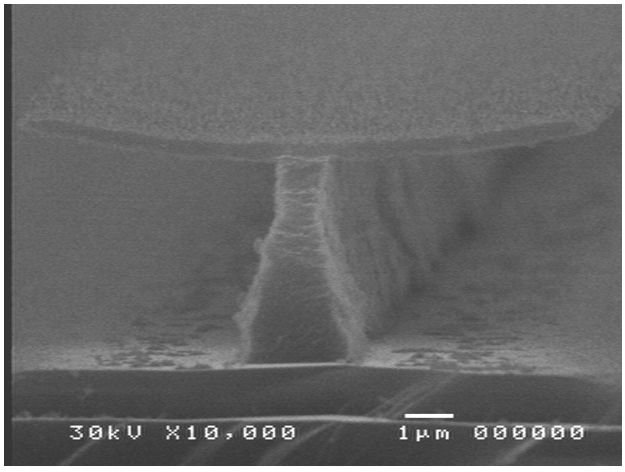
(b)



(c)



(d)



(e)

Figure 6. SEM images of the polysilicon profile after etching. Process conditions: SF6/CF4/CHF3 = 1.5/5/2, total flow 17 sccm, 100mTorr, 50W, 100V. a) 6min, ULE=0.96µm, A_t=0.43; b) 9min, ULE=1.31µm, A_t=0.46; c) 12min, ULE=1.50µm, A_t=0.51; d) 15min, ULE=2.8µm, A_t=0.73; e) 27.5min, ULE=5.6µm, LLE=5.12µm, A_t=0.86.

lower: ER~200nm/min; this can be attributed to the difficulty of the transport of reactive species through the tunnel formed during etching relatively long.

The final inverted profile (Figure 10a) shows the greater etching speed in the inferior part of the structure (flow of the reactive species along the oxide surface).

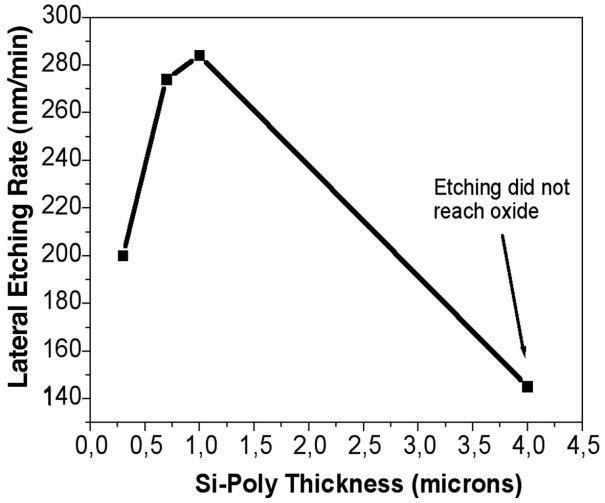
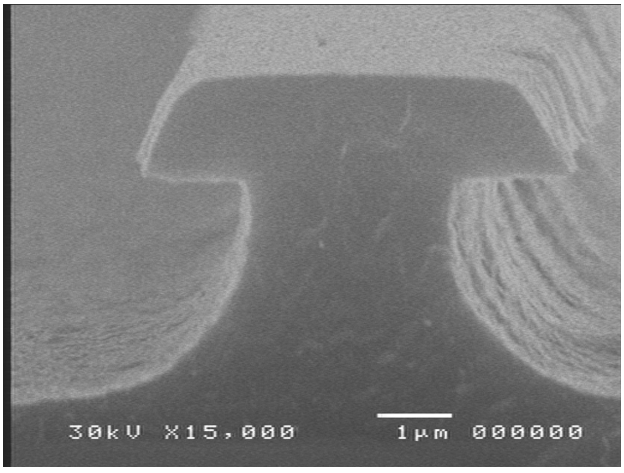
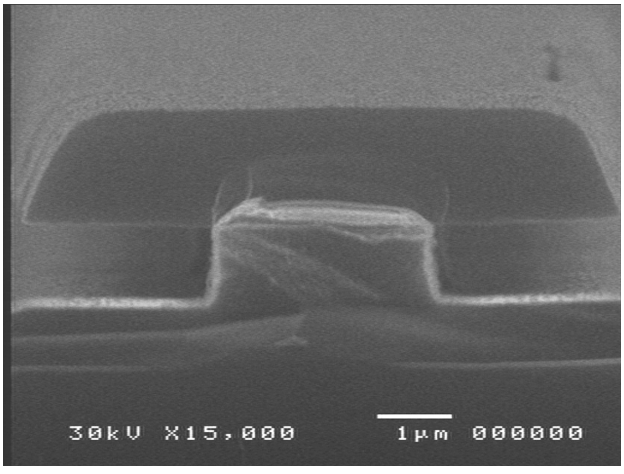


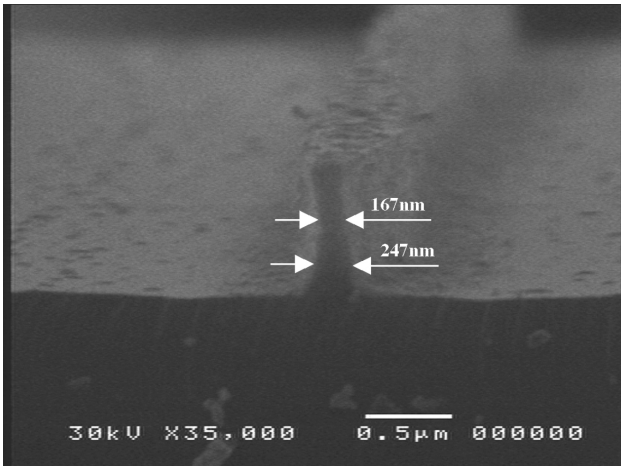
Figure 7. Lateral Etching Rate vs. Si-Poly Thickness in $SF_6/CF_4/CHF_3$ plasma. Conditions: $SF_6/CF_4/CHF_3$ = 3/10/4 sccm, 100mTorr, 50W, 105V, 9min.



(a)



(b)



(c)

Figure 8. SEM images of the polysilicon profile after etching. Process conditions: SF6/CF4/CHF3 = 1.5/5/2, total flow 17 sccm, 100mTorr, 50W, 105V, 9min. a) Thickness 4µm, ULE=1.31µm, A_t=0.43; b) 1µm, ULE=2.56µm, LLE=2.47µm, A_t~0.92; c) 0.7 µm, ULE=2.47µm, LLE=2.41µm, A_t~0.92. Note that in the last case, the resist layer was removed.

The tests of repeatability under this process conditions showed good results with variations in the lateral etching rate being <10% (see, for example, Figs. 10).

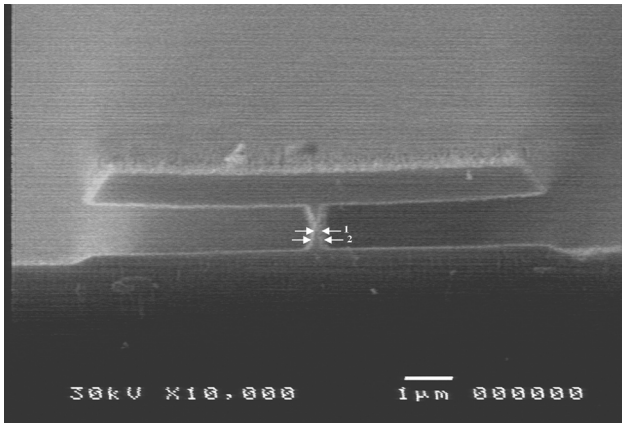
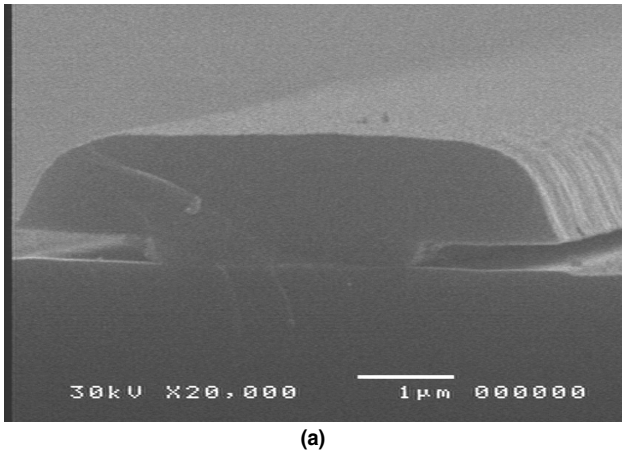
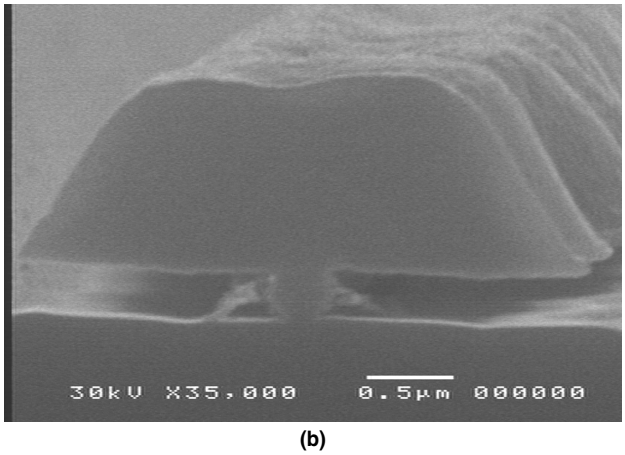


Figure 9. SEM image of the polysilicon profile after etching. Process condition: SF6/CF4/CHF3 = 1.5/5/2, total flow 17 sccm, 100mTorr, 50W, 130V, 15min, A_t=0.95, S~30.



(a)



(b)

Figure 10. SEM image of the 300nm thick polysilicon profile after etching of 7,5min. Process condition: SF6/CF4/CHF3 = 1.5/5/2, total flow 17 sccm, 100mTorr, 50W, 86V. (a) ULE=1.5µm, (b) ULE=1.49µm.

4. CONCLUSION

This work presents the results of the thinning technique developed for a conventional RIE etcher using fluorine and carbon containing gas mixtures. The method can be used for fabrication of sub-micron Si-poly gates in CMOS technology, with the mini-

mum line width being considerably narrower than that available with a conventional photolithography technique, and also in MEMS devices fabrication. High anisotropy of Si structures is obtained, with the anisotropy factor obtained being as high as 0.92-0.98. The improvement of the Si-poly etched structure anisotropy is explained by the process of enhanced transport of etching species (fluorine radicals) along the oxide surface during the overtech stage. The method was used to etch Si-poly layers with thickness from 4 to 0.3 μm.

The viability of the technique for application in CMOS transistor gate using 300nm thick Si-poly and final width of ~250nm with acceptable repeatability (difference <10%), was presented.

ACKNOWLEDGEMENTS

The authors would like to thank Profa. Dra. Lucila Cescato (IFGW/UNICAMP) for SEM inspections, MSc. Antônio Celso S. Ramos (LPD/UNICAMP) for technical support, MSc. Ricardo Cotrin for samples of Si-poly, all CCS staff for help in this work and CNPq (PNM Program) for financial support.

APPENDIX

Definition of the anisotropy factor

To characterize the process of conventional etching, a commonly used factor of anisotropy is determinated as

$$A = 1 - L / H \qquad (1)$$

where L is the undercut (lateral etching under the photoresist) and H is the etch depth. When the overtech step is absent or short, the parameters L and H are proportional to the horizontal and vertical etch rates, respectively. However, in the case of a thinning process where the overetch phase is essential (see Figure 11), and the etch front moves basically in the lateral direction, it is necessary to redefine the A factor as follows:

$$A_t = 1 - \Delta / H \qquad (2)$$

$$ER_{LU} = ULE/t \qquad (3)$$

$$ER_{LL} = LLE/t \qquad (4)$$

where A_t is the anisotropy factor for the thinning process; Δ = ULE – LLE, ULE – the upper lateral etching; LLE - the lower lateral etching, H - the etch depth (thickness of the Si-poly film); ER_{LU} – the upper lateral etching rate; ER_{LL} – the lower lateral etching rate; t is time of the etching process.

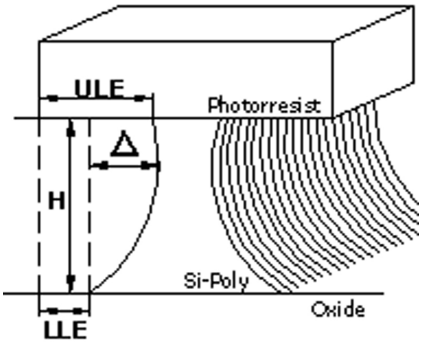


Figure 11. Definition of the anisotropy factor for the thinning process.

REFERENCES

[1] G. S. Oehrlein, M. F. Doemling, B. E. E. Kastenmeier, P. J. Matsuo, N. R. Rueger, M.Schaepkens, and T. E. F. M. Standaert, IBM J. Research and Development, 43, 1/2, 1999, 181-196.
[2] Y. S. Song, J. W. Kim, and C. W. Chung, Thin Solid Films, 467, 2004, 172-175.
[3] F. Laermer and A. Urban, Microelectron. Eng., 67/68, 2003, 349-355.
[4] A. M. Nunes, P. J. Tatsch, S. A. Moshkalyov, A. M. Daltrini, M. Machida, in Proceedings of the 8º Encontro Brasileiro de Física dos Plasmas, Niteroi-RJ, 2005.
[5] M. Tuda, K. Shintani and J. Tanimura, Plasma Sources Sci. Technol., 12, 2003, S72-S79.
[6] N. St. J. Braithwaite, and T. Matsuura, Contrib. Plasma Phys., 44, 5/6, 2004, 478-484.
[7] A. Tserepi, E. Gogolides, C. Cardinaud, L. Rolland, and G. Turban, Microelectron. Eng., 411, 41/42, 1998, 411-414.
[8] J. Foucher, G. Cunge, L. Vallier, O. Joubert, Microelectron. Eng., 61-62, 2002, 849-857.
[9] Kern, RCA Review, 31, 187, 1970.
[10] R. C. Teixeira, I. Doi, M. B. P. Zakia, J. A. Diniz, J. W. Swart, Mat. Sci. Eng. B, 124-125, 2005, 138-142.
[11] L. Dreeskornfeld, J. Hartwich, J.Kretz, L. Risch, W. Roesner and D. Schmitt-Landsiedel, J.Vac.Sci.Technol. B, 20(6), 2002, 2777-2779.