Fabrication of Ti-Si-Ti Metal-Semiconductor-Metal Photodetectors Using Low Temperature Rapid Thermal Annealing

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ABSTRACT

The electrical properties of Ti-Si-Ti Metal-Semiconductor-Metal (MSM) photodetector were studied as a function of annealing temperature, using Rapid Thermal Annealing (RTA) process. Low temperatures were used at the RTA (200-350°C) in order to avoid the formation of silicides. We observed a decrease in the dark current on samples annealed between 200 and 300°C. The lowest dark current was obtained in the sample annealed at 250°C (4.8 nA), which is one order of magnitude lower than as-deposited sample (53.5 nA). The sample annealed at 350°C had an increase in dark current (82.9 nA). This behavior of the dark current can be explained by the increase in the barrier height at 200-300°C annealing temperature range, due to increase of the thickness of the amorphous interdiffused Ti-Si interfacial layer, and decrease in the barrier value at sample annealed at 350°C, due to pre formation of C49 $TiSi_2$.

Index Terms: Metal-Semiconductor-Metal; Photodetetors; Schottky barrier height; Rapid Thermal Annealing.

1. INTRODUCTION

Planar Schottky Metal-Semiconductor-Metal (MSM) photodetector has been subject of study in the last years due to ease of fabrication, low capacitance per unit area (in comparison with conventional vertical p i n photodiodes) and fabrication compatibility with conventional MOS processes, making it suitable to be applied in optoelectronic integrated circuits (OEIC) [1], optical interconnections on chip-to-chip level [2-3] and integrated optical sensors [4-5].

To obtain good signal detection, the signal-to-noise current ratio should be as high as possible, which is made in MSM devices by decreasing the dark current and increasing the photocurrent.

Several techniques were reported to decrease the dark current. Some of them consists in: depositing a passivation coating over the entire active area, minimizing the charge surface conduction by interface states [3]; minimize the tunneling current due to high electric field under the electrode contact pads, by implementing an insulator layer under the pads area [5-6]; pattern the entire metal over a very thin insulator film, to obtain an effect of barrier enhancement layer, decreasing the thermionic emission current [7]; and construct the MSM device with two different metals, one to each electrode, to obtain higher values of hole and electron barrier heights [8].

To enhance the photocurrent, a transparent material can be used in the electrodes [9] or the electrodes fingers can be fabricated in a trench form over an intrinsic amorphous silicon layer, which enhances the electrical field onto deep depths and improve the optical absorption of the incident radiation [10].

Another possibility to modify the electrical behavior of metal-semiconductor devices is an annealing process [11-14]. Generally, the annealing process is used to obtain silicides, but in this work, the silicides were avoided because the two most common titanium silicide phases results in ohmic contacts (C54 $TiSi_2$) or in lower barrier height in p type silicon, when compared to as deposited Ti/Si interface barrier height (C49 $TiSi_2$) [14]. Since the annealing process in this work should not result in silicides, the annealing was done just to modify the metal semiconductor interface. Using the information about the silicides temperature formation and barrier height, it was decided that the annealing temperature range should be lower than 380°C, which is the annealing temperature that starts the formation of C49 $TiSi_2$ phase, as described

in Ogawa et al [11]. The only information found in the literature about Ti/Si Schottky contact annealing was in Bakir et al [3], which reported that Ti-Si-Ti MSM devices annealed during one hour, in conventional furnace, on N_2 atmosphere at 200°C, have decreased in one order of magnitude the dark current. However, for samples annealed during two hours, Bakir observed a slightly increase in the dark current.

Due to the lack of information available at the literature about the effects of low temperature annealing in a Ti/Si Schottky contact, it was not possible to confirm that the best results in terms of barrier height value would be obtained in a 200°C annealing process. To obtain the optimum annealing temperature, four different annealing temperatures were used, all of them in the temperature range of 200-350°C, to verify which annealing temperature gives the best barrier height enhancement in Ti/p-Si contacts.

In this paper, we show the effects of low temperature RTA process in the electrical properties of Ti Si Ti MSM devices. The Rapid Thermal Annealing (RTA) was chosen because it has much less thermal budget, better wafer to wafer temperature control and easiness to adjust the temperature.

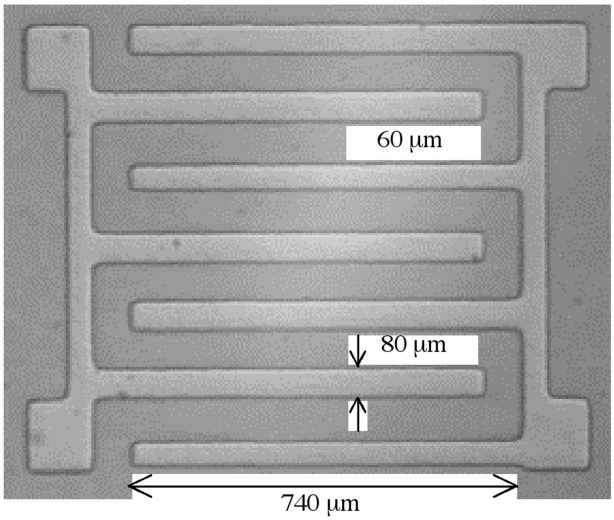

Figure 1. Titanium interdigitated electrodes

Table I. Temperature ramp-up used in RTA processes

Annealing Temperature (°C)	Ramp-up (°C/s)
200	3.8
250	4.2
300	4.6
350	5.1

2. DEVICE FABRICATION

The MSM devices were fabricated on <100> p-type silicon wafer, 3 inches (75 mm) in diameter and resistivity 1-10 Ω.cm. All wafers were cleaned using the standard RCA process. Immediately before the metal deposition, all wafers were dipped in diluted HF solution (1:100) to remove the oxide of the surface, which ensures good electrical contact between the metal and semiconductor.

Titanium was used as electrode material due to excellent adhesion on silicon surface and lower work function than silicon, which promotes higher barrier values on a p-type silicon. The Ti film (220 nm thick) was deposited using sputtering process in Ar atmosphere during 80 minutes, in a process pressure of 46.10^{-4} Torr (613.10^{-3} Pa) and 250 W of RF power. The base pressure was 1.10^{-5} Torr (1.10^{-3} Pa).

The metal interdigitated structure of the electrodes was patterned in the Ti film using a wet etching solution of 20 H_2O + 1H_2O_2 + 1 HF at room temperature. Figure 1 shows the Ti interdigitated electrodes.

The annealing processes were done in an AG 410 Heatpulse RTA furnace in four samples, using four different temperatures: 200, 250, 300 or 350°C, in dry N_2 ambient during 5 minutes. The RTA temperature ramp-up is shown in Table I. After the annealing process, the samples were naturally cooled. Before each RTA process, all samples were submitted to a dry N2 flow during 5 minutes at room temperature, to remove water adsorption from the surface and ensure that the furnace has only nitrogen on its atmosphere.

3. EXPERIMENTAL RESULTS

The electrical parameters of the MSM devices were extracted using current-voltage measurements of dark current and photocurrent. One He-Ne laser (wavelength = 632.8 nm and optical power = 520 μW) was used to irradiate the photodetectors and obtain the photocurrent values. Before each measurement, the laser beam was adjusted to cover the entire active area to ensure maximum photocurrent. Table II shows the results of the dark current, photocurrent, DC responsivity (photocurrent generated per incident optical power) and photo/dark current ratio, obtained from the fabricated photodetectors.

The samples annealed between 200 and 300°C had lowered the dark current about one order of magnitude, obtaining similar results described in Bakir et al [3]. The drawback verified in the samples annealed between 200 and 300°C is the decrease of the photocurrent by a factor of six, resulting in a DC responsivity of the annealed samples of only 17% of the DC responsivity of the as-deposited sample. However, the

Table II. Electrical parameters of MSM devices at 5 V bias

Sample	Dark current (nA)	Photocurrent (μA)	DC Responsivity (A/W)	Photo/Dark current ratio (x10^3)
as-deposited	53.5	120.4	0.231	2.25
annealed at 200°C	9.4	20.8	0.039	2.21
annealed at 250°C	4.8	21.4	0.041	4.46
annealed at 300°C	7.0	22.4	0.043	3.20
annealed at 350°C	82.9	10.0	0.019	0.12

photo/dark current ratio in the annealed samples could still be enhanced by about 50%, compared to as-deposited sample. The best results were obtained with the sample annealed at 250°C. In Figure 2 is shown the dark current and photocurrent behavior of as-deposited and 250°C annealed samples. The faster current saturation that occurs in the annealed sample compared to the as-deposited sample can be attributed to a metal semiconductor interface that is closer to the ideal in the annealed sample, minimizing the value of diffusion potential of the Schottky contacts [15]. Due to this, a more intense electrical field is obtained in the depleted area in the annealed samples, obtaining a faster collection to the electrodes of the electron-hole pairs generated in the active area. The large dimensions were used because it makes easier to the photodetectors to be fabricated and to adjust the illuminated area. Also, it was shown in Khunkhao et al [16] that MSM devices with large dimensions (> 10μm) also work very well, despite off the existence of the undepleted region.

The sample annealed at 350°C had increased the dark current and decreased the photocurrent, when compared to as deposited sample.

The barrier heights and ideality factors were calculated using the thermionic emission model described in [5, 17] and are shown in Table III.

For the as-deposited sample, the barrier height obtained is very close to the one reported by Çancaya et al [18]. The ideality factor is close to unity, indicating that the fabrication process gives good Schottky contact.

The annealed samples between 200 and 300°C had higher values of barrier height than as deposited, keeping the ideality factor close to unity. The increase in the barrier value is the reason why both dark and photocurrent had decreased. With a higher value of contact barrier, fewer carriers will have energy to surpass the contact potential and reach the electrodes [5, 8, 19]. The explanation to this behavior of the barrier height value is the increase in the thickness of the amorphous Ti-Si interface layer when it is submitted to an annealing process, resulting in a more uniform metal-semiconductor interface. The amorphous inter-diffused Ti-Si phase is present at the interface even in the as deposited samples, due to the ballistic energy of the sputtered Ti atoms during the deposition process [11, 12]. The value of barrier height reported by Ogawa et al [11] below 380°C is 0.73 eV, which is very close of the values obtained for the samples annealed between 200 and 300°C.

In the sample annealed at 350°C, the barrier height value was lower than as deposited, also keeping the ideality factor close to unity. This behavior can be explained by the pre formation of C49 $TiSi_2$ phase in the Ti-Si interface, which occurs at temperatures between 380 and 485°C. In this temperature range, there is the coexistence of amorphous Ti-Si and crystalline C49 $TiSi_2$-Si phases at the interface [11]. The value of barrier height for the sample annealed at 350°C is in between the values reported by Ogawa et al [11] for Schottky barrier contacts of Ti-Si (0.73 eV) and C49 $TiSi_2Si$ (0.57 eV).

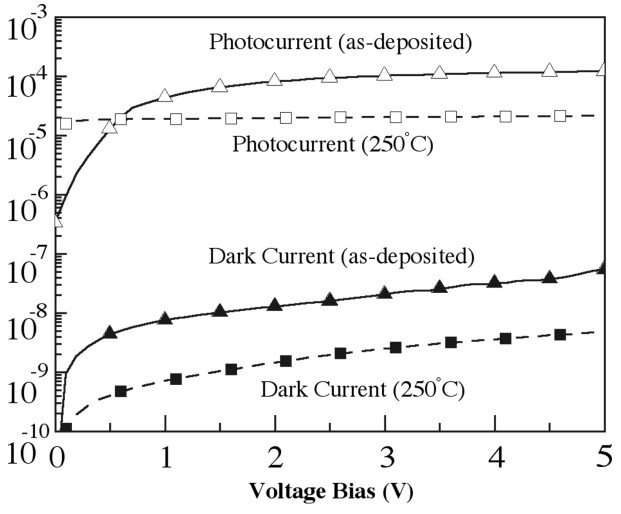

Figure 2. Current-voltage curves of as-deposited (solid lines) and 250° C annealed (dotted lines) samples obtained at room temperature.

Table III. Electrical parameters of thermionic emission model

Sample	Barrier Height (eV)	Ideality factor
as-deposited	0.70	1.02
annealed at 200 °C	0.74	1.02
annealed at 250 °C	0.75	1.01
annealed at 300 °C	0.74	1.01
annealed at 350 °C	0.67	1.01

4. CONCLUSIONS

The Ti-Si-Ti MSM photodetectors fabricated using RTA process showed higher barrier values when annealed in temperature range of 200-300°C, compared with the as deposited sample. Thus, a decrease in the dark current of one order of magnitude was obtained using a low thermal budget process. The best results obtained were on 250°C annealing temperature. The ideality factor was also kept very close to unity, indicating good Schottky contact on annealed samples. Despite off the significant decrease in responsivity, the photo/dark current ratio could still be increased, showing that the RTA process improves the overall performance of MSM devices.

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