Study Of MOS Capacitors With TiO_2 And SiO_2/TiO_2 Gate Dielectric

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ABSTRACT

Abstract— MOS capacitors with TiO_2 and TiO_2/SiO_2 dielectric layer were fabricated and characterized. TiO_2 films where physical characterized by Rutherford Backscattering, Fourier Transform Infrared Spectroscopy and Elipsometry measurements. Capacitance-voltage (1MHz) and current-voltage measurements were utilized to obtain, the effective dielectric constant, effective oxide thickness (EOT), leakage current density and interface quality. The results show that the obtained TiO_2 films present a dielectric constant of approximately 40, a good interface quality with silicon and a leakage current density, of 70 mA/cm² for V_G = 1V, acceptable for high performance logic circuits and low power circuits fabrication, indicating that this material is a viable substitute for current dielectric layers in order to prevent tunneling currents.

Index Terms: high-κ dielectrics, TiO_2, MOS Capacitors, double dielectric layer.

1. INTRODUCTION

The progress in complexity and efficiency of CMOS circuits has been achieved throughout the last decades by scaling the geometric dimensions of the metal oxide-semiconductor field-effect-transistor (MOSFET) [1-5]. This scaling had to be accompanied by a decrease in the gate oxide thickness in order to maintain electrostatic control of the charges induced in the channel [3,4,6,7].

The silicon industry has been scaling SiO_2 aggressively for the past 15 years for low power, high performance CMOS logic applications. SiO_2 thin films as thin as 1.2 nm have already been utilized, however tunneling current increases exponentially for decreasing dielectric thickness, becoming significant for SiO_2 films thinner than 3 nm. Another problem for ultra-thin SiO_2 dielectric layers, when p+ polysilicon is used as gate contact in p-MOSFET's, is the low barrier against boron diffusion which causes a shift in the device threshold voltage [8-11]. To overcome these problems, much research is directed to the substitution of SiO_2 by high – κ materials making possible the use of thicker films [3,4,5,7,11]. An alternative material, in spite of its relatively low dielectric constant (4 – 7), is SiO_xN_y because it is totally compatible with the silicon MOS technology and has improved properties, such as enhanced resistance to high field stress, enhanced hot carrier immunity, resistance against boron penetration, higher dielectric strength and higher dielectric constant, over conventional SiO_2 [11-13]. This material, obtained through a thermal oxynitridation, is already utilized in the MOS technology. However, according with the International Technology Roadmap for Semiconductors, to meet the scaling goals and at the same time keep the gate leakage current within tolerable limits (10 A/cm²) a dielectric constant higher than 25 will be needed by 2008 [14]. There are numerous challenges associated with implementing such an advanced gate stack, including ensuring adequate channel carrier mobility with the new high-κ dielectric, and reducing to tolerable levels the defects, charge trapping, and instabilities at the high-κ/ Si interface. Its important to observe that electric permitivity is not the unique criterion for dielectric performance, it is also desirable that the material present the following properties: to be amorphous, in order to eliminate leakage along grain boundaries, have a large optical bandgap, have a large band offset between its conduction/valence band and Si conduction/valence band, be thermodynamically stable and a good barrier against boron diffusion and present a good silicon/dielectric interface quality [5].

Several high-κ materials are considered to replace SiO_2 gate dielectric, among all these candi-

dates, HfO_2 has been mentioned as the most promising, because is more thermodynamically stable on Si than other high-k materials, it has a reasonably high dielectric constant (~25) and a relatively large band gap (5.68 eV). [15,16] However this film presents a poor interface quality with Si, high oxygen diffusion rate through the film, causing a low-κ interfacial layer growth, and a low crystallization temperature (500°C) [17,18]. To produce good interface quality an ultra-thin SiO_2 film is grown between both materials, producing a high k/SiO_2 stack. The SiO_2 layer between the high k film and the Si substrate reduces the equivalent dielectric constant [19]. Some works report that nitrogen incorporation in HfO_2 (HfO_xN_y) produces a film with improved interface properties, suppressing impurity penetration, enhancing reliability and increasing the crystallization temperature (>1000°C) [17]. On the other hand this HfO_xN_y film presents a lower dielectric constant of approximately 13.

In this way, the study of other metal oxides, with a dielectric constant higher than 25, is very interesting [3-5]. However with the large number of criteria, mentioned above, required for SiO_2 or SiO_xN_y substitution it is not surprising that no definite solution to the problem has yet been presented. Thus, up to this moment, the ITRS does not have an adequate material to substitute them. In this work we present a study of titanium dioxide (TiO_2) as gate dielectric layer. Even though the electronic bandgap of this material is relatively small (3.5 eV), its dielectric constant can be varied from 40 to 110. Depending on the growth process TiO_2 presents two important phases, Anatase and Rutile. The last one is the thermally stable phase that presents the higher dielectric constant, approximately 80, Anatase is a thermally unstable phase with lower dielectric constant transforming in Rutile phase at temperatures over 600° C [20]. However this material presents high leakage current values, unacceptable for transistor fabrication, it presents also a higher silicon/dielectric interface state density, when deposited onto Silicon and submitted to high temperature it can segregate into a SiO_2 and metallic oxide (M_xO_x) [4]. In order to minimize these problems it is interesting to utilize a thin SiO_2 layer separating the TiO_2 film from the Si substrate. In this way, the interface quality is preserved and the other problems minimized, turning this material viable and very attractive to substitute the current dielectric material.

In this work a set of MOS Capacitors utilizing TiO_2 and Si/TiO_2 films as gate dielectric layer were fabricated. The TiO_2 films were deposited by reactive sputtering at room temperature and the SiO_2 films were thermally grown. We characterize these capacitors by I –V and high frequency C-V measurements.

2. EXPERIMENT

A. Films deposition

TiO_2 films were deposited by reactive sputtering, utilizing a gaseous mixture of argon (60%) and oxygen (40%) and a titanium target. SiO_2 films were thermally grown at 1000°C in O_2 ambient.

All the films studied were deposited onto p-type (100) single crystalline silicon substrates in the 1-10 Ω.cm resistive range, for Fourier Transform Infrared (FTIR), Rutherford Backscattering Spectroscopy (RBS) and Ellipsometry measurements.

The refractive index and the thickness of the samples were obtained by ellipsometry measurements performed in a Gaertner equipment having a He-Ne laser (632.8 nm) as light source. The amount of Ti and O per unit area (atoms cm^{-2}) was obtained by RBS experiments at LAMFI/USP, Sao Paulo, using a He^+ beam with an energy E=1.7 MeV and a detection angle $\theta = 170^o$. To simulate the spectra we utilize the SIMNRA program.

B. MOS Capacitors Fabrication

Two sets of MOS Capacitors were fabricated on p-type (100) – oriented silicon wafers with resistivity in the 1-10 Ω.cm range. The silicon substrates were chemically cleaned by standard RCA procedure and subsequent etching in diluted HF solution to remove the native SiO_2 layer. In sequence ~ 58 nm of TiO_2 insulating layer was deposited by reactive sputtering from Ar (60%) and O_2 (40%). In the case of the double gate layer, firstly a SiO_2 thin film was thermally grown at 1000°C in O_2 ambient following by the TiO_2 film deposition. In the table I, are shown the set of fabricated MOS capacitors and studied in this work. The metallic contacts for all of the studied capacitors were obtained by the sputtering technique depositing 300 nm of Al. The $9x10^{-4}$ cm^2 capacitor contact area was defined by photolithography and subsequent chemical etching, the contacts were annealed in forming gas atmosphere (4% of H_2 and 96% of N_2) at 450°C for 30 min.

The high (1MHz) frequency C-V measurements were performed in a Keithley, model 82 – DOS

Table I. MOS Capacitors fabricated

Capacitor	Dielectric gate	TiO_2 thickness (nm)	SiO_2 thickness (nm)
1	TiO_2	58	—
2	SiO_2/TiO_2	58	6
3	SiO_2/TiO_2	58	14
4	SiO_2	—	49

Simultaneous C – V, equipment and the I-V characteristics were measured in a HP 5156A. From these curves, the equivalent dielectric constant, the equivalent oxide thickness (EOT) and the leakage current density were calculated.

3. RESULTS

A. Films physical characterization

In figures 1 and 2, are shown, respectively, the RBS and FTIR spectra for the TiO_2 material, utilized as gate dielectric layer in the MOS capacitors. A chemical composition of 65% O_2 and 34% Ti was obtained, indicating that this film is stoichiometric TiO_2 material. In the FTIR spectrum we observe absorption bands around 423 and 443 cm^{-1}, close to the anatase band at 438 cm^{-1}[21].An absorption band around 605 cm^{-1}, close to the rutile phase band (610cm^{-1}) is also observed [21], indicating that the deposited film presents a mixture of phases. The ellipsometry measurements, gave a refractive index of approximately 2.47, close to the obtained for anatase phase (2.56) [21].

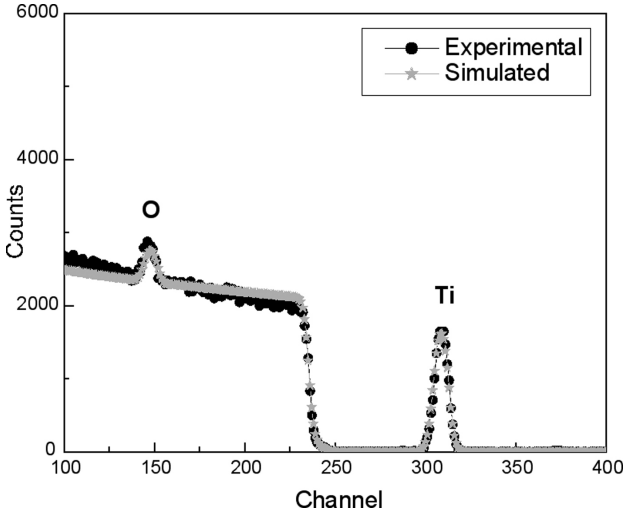


Figure 1. TiO_2 RBS spectra.

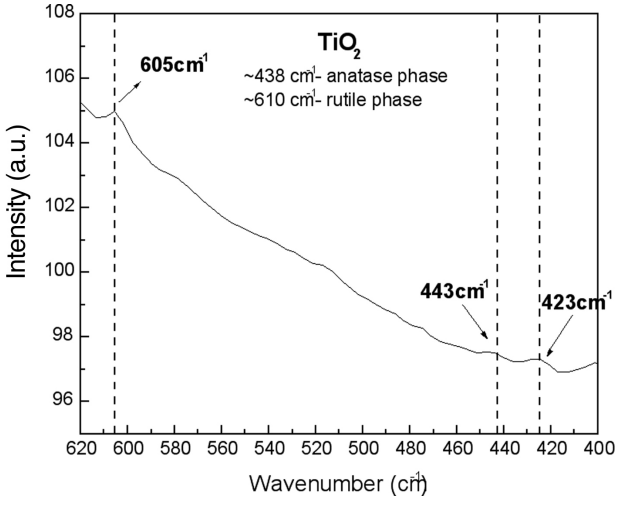


Figure 2.TiO_2 FTIR spectrum.

B. MOS Capacitors results

The high frequency (1 MHz) C-V curves for the fabricated MOS capacitors are shown in figure 3.

The curve for the MOS capacitor with just TiO_2 layer does not present saturation of C_{ox} (oxide capacitance), probably due to the high leakage current through the dielectric. However it is possible to observe that the curve presents just a small shift towards higher or lower values of V_G, indicating that the effective charge density remains within acceptable values. This effective charge density might be the cause of the lateral inversion effect, observed through the small step in inversion. MOS capacitors fabricated with thermally grown SiO_2 present a shift to negative voltage values indicating the presence of a significant amount of positive charge probably due to furnace contamination.

To analyze the interface quality, the curves were normalized (figure 4).

It is possible to observe that the capacitor utilizing 14 nm SiO_2 presents the best interface quality together with the device with only SiO_2 as gate dielectric layer, since they present a very abrupt C_{min} to C_{ox} increase. The capacitor with only a TiO_2 layer, presents good interface properties too, but this is masked by the leakage current through the film, that prevents the saturation of the dielectric capacitance value.

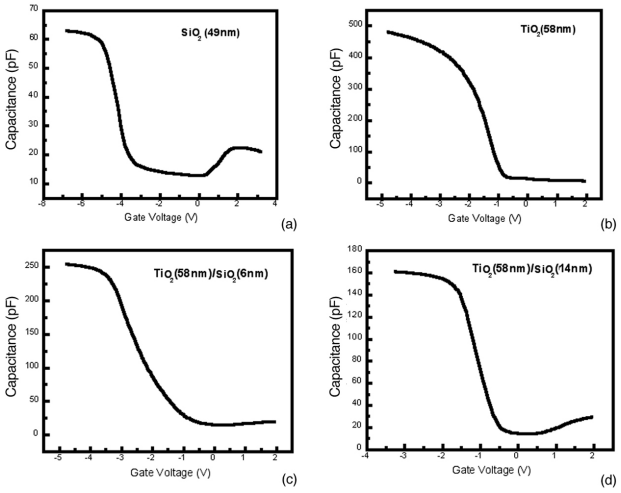
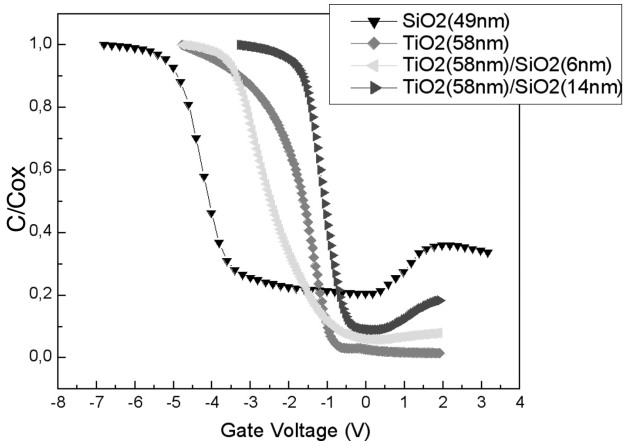


Figure 3. C-V curves for MOS capacitor with (a) SiO_2, (b) TiO_2 (c) TiO_2/6nm (d) TiO_2/14nm SiO_2 dielectric layer.



Figue 4. Normalized C-V curves.

Table II. Dielectric Constant, Equivalent oxide thickness (EOT) and Leakage current density to V_G=1V extracted from C-V and I-V curves.

Capacitor	Gate Dielectric	Dielectric Constant	EOT (nm)	Leakage current density to V_G= 1 V (A/cm^2)
1	TiO_2 (58nm)	40	5	0.07
2	TiO_2(58nm)/ SiO_2 (6nm)	20	12	4.7x10^{-6}
3	TiO_2(58nm)/ SiO_2 (14nm)	15	19	3.2x10^{-6}
4	SiO_2 (49nm)	3.9	49	1.3x10^{-8}
	SiO_2 thermally grown grown (high quality) [4]	*3.9*	*5*	*<10^{-9}*

In figure 5 the leakage current density curves as function of the applied gate voltage are shown. In table II, are presented the results for effective dielectric constant, equivalent oxide thickness (EOT) and the leakage current density for 1 V of V_G , extracted from the C-V and I-V measurements, and is present too this values to a SiO_2 thermally grown with high quality extracted to a review report [4], to compare with our results.

The deposited TiO_2 analyzed presented a dielectric constant value of approximately 40, an order of magnitude higher than the obtained for SiO_2 (3.9). A device with EOT of 5 nm was fabricated with this material and it presented a leakage current density of 70 mA/cm^2, acceptable for high performance logic circuits (maximum of 100 A/cm^2) and low power circuits (maximum 10A/cm^2) fabrication, but not sufficiently low for power-limited applications (1 mA/cm^2) [3,14]. This leakage density current value, when compared with a thin film of high quality thermally grown SiO_2 film with the same thickness of 5nm (< 10 nA/cm^2), is still high.

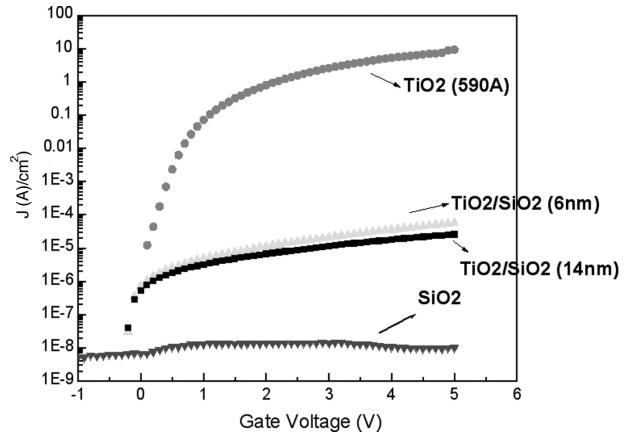


Figure 5. Leakage current density x V_G.

Some works report that adding a thin SiO_2 film between the TiO_2 and the Si interface, reduces the leakage current density in 3 to 4 orders of magnitude. In this work we utilize a 6 and a 14 nm thin SiO_2 film at the TiO_2/Si interface, as it can be observed in table II, a layer of 6 nm of SiO_2 is sufficient to reduce the leakage current in 3 orders of magnitude. These results indicate that TiO_2 deposited onto a thin silicon dioxide layer at the Si interface is a strong candidate to substitute the current dielectric in CMOS fabrication.

4. CONCLUSIONS

MOS capacitors with TiO_2 and TiO_2/SiO_2 gate dielectric were fabricated and characterized. The physical characterization of the TiO_2 films show that it is a stoichiometric material and its phase is closer to anatase.

The C-V and I-V results show that the obtained TiO_2 films present a dielectric constant of approximately 40, with a good interface quality with silicon and with a leakage current density, for V_G = 1V, of 70 mA/cm^2, acceptable for fabricating high performance logic circuits (maximum of 100 A/cm^2) and low power circuits (maximum 10A/cm^2) fabrication. However, this leakage current is higher yet, when compared to a SiO_2 thermally film (high quality) with the same thickness (< 10 nA/cm^2). To reduce this leakage current we utilize a thin SiO_2 film layer between Si and the TiO_2 layer, sufficient to reduce this current 3 orders of magnitude, but increase a dielectric constant. More research is needed to solve the leakage current problem without a significant decrease in the effective dielectric constant, also studies are on the way to analyze thermal stability against phase transformation.

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REFERENCES

[1] C.K. Maiti*, S.K. Samanta, G.K. Dalapati, S.K. Nandi, S. Chatterjee, Electrical characterization of TiO_2 gate oxides on strained-Si *Microelectronic Engineering,* 72 (2004) 253

[2] Roy Pailya et. al, Pulsed laser deposition of TiO_2 for MOS gate dielectric, *Applied Surface Science*, 187 (2002) 297

[3] S.A. Campbell, et al.Titanium dioxide (TiO_2)-based gate insulators. *IBM J.Res. Develop*. 43, Nº3, (1999) 383

[4] G.D. Wilk, R.M.Wallace, J.M. Anthony, High-*k* gate dielectrics: Current status and materials properties considerations. *J.Appl.Phys. APPLIED PHYSICS REVIEW*, Vol.89, number 9 (2001) 5243.

[5] T Busani and R.A.B Devine , Dielectric and infrared properties of TiO_2 films containing anatase and rutile. *Semiconductor Science and Technology* 20, Nº8 (2005) 870.

[6] Hisashi Fukuda et. al, Structural and Electrical Properties of Crystalline TiO_2 Thin Films Formed by Metalorganic Decomposition*. Japanese Journal Applied Physics,* 38, (1999) 6034.

[7] H.D.B. Gottlob et.al. Introduction of crystalline high-k gate dielectrics in a CMOS process, *Journal of Non-Crystalline Solids*, 351 (2005) 1885.

[8] K. Eriguchi, Y.Harada, M. Niwa, Effects of base layer thickness on reliability of CVD Si_3N_4 stack gate dielectrics *Microelectronics Reliability,* 41 (2001) 587.

[9] C. S.Mian, I. Flora, Nitrogen in ultra-thin gate oxides: its profile and functions, *Solid-State Electronics*, 43 (1999) 1997

[10] G.lucovsky, Silicon oxide/silicon nitride dual-layer films: a stacked gate dielectric for the 21 st century. *Journal of Non-Crystalline solids* 254 (1999) 26.

[11] M.L.Green, Ultrathin (< 4nm) SiO_2 and Si-O-N gate dielectric layers for silicon microelectronics: Undestanding the processing, structure, and physical and electrical limits. *J. Appl. Phys. APPLIED PHYSICS REVIEW*, Vol.90, number 5 (2001) 2057.

[12] B.Hajji, P.Temple-Boyer, F. Olivié, A. Martinez, Electrical characterisation of thin silicon oxynitride films deposited by low pressure chemical vapour deposition. *Thin Solid Films,* 354 (1999) 9.

[13] J.Chan, et al., Oxynitride gate dielectric prepared by thermal oxidation of low-pressure chemical vapor deposition silicon-rich silicon nitride**.** *Microeletronics Reliability,* 43 (2003) 611.

[14] The International Technology Roadmap for Semiconductors, 2005 (http://www.itrs.net/links/2006Update/2006UpdateFinal.htm).

[15] Zhaorui Song et al. Influence of nitrogen element on total-dose radiation response of high-k Hf-based dielectric films . *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, 257, (2007) 501.

[16] G. He et al. Optical and electrical properties of plasma-oxidation derived HfO_2 gate dielectric films. *Applied Surface Science* 253 (2007) 3413

[17] G.He et al. Structural and interfacial properties of high-k HfO_xN_y gate dielectric films. *Materials Science in Semiconductor Processing*, 9 (2006) 870.

[18] J-H Park et al., Electrical properties of HfO_xN_y thin films deposited by PECVD*. Surface & Coatings Technology*, 201 (2007) 5336.

[19] E.Amat et al. Influence of the SiO_2 layer thickness on the degradation of HfO_2/SiO_2 stacks subjected to static and dynamic stress conditions. *Microelectronics Reliability*, 47 (2007) 544.

[20] Masaru Kadoshima et al. Rutile-type TiO_2 thin film for high-κ gate insulator, *Thin Solid Films*, 424, 224 (2003).

[21] Jun-Ying Zhang, et al. Nanocrystalline TiO_2 films studied by optical, XRD and FTIR spectroscopy, *Journal of Non-Crystalline Solids*, 303 (2002) 134.