Charge-Based Continuous Equations for the Transconductance and Output Conductance of Graded-Channel SOI MOSFET's

Michelly de Souza[1] and Marcelo Antonio Pavanello[1,2]

[1] Laboratório de Sistemas Integráveis, Universidade de São Paulo, São Paulo, Brazil
[2] Departamento de Engenharia Elétrica, Centro Universitário da FEI, São Bernardo do Campo, Brazil
e-mail: michelly@lsi.usp.br

ABSTRACT

This paper presents charge-based continuous equations for the transconductance and output conductance of submicrometer Graded-Channel (GC) Silicon-On-Insulator (SOI) nMOSFET. The effects of carrier velocity saturation, channel length modulation and drain-induced barrier lowering were taken into account in the proposed equations. Experimental results were used to test the validity of the equations by comparing not only the transconductance and the output conductance, but also the Early voltage and the open-loop voltage gain, showing a good agreement in a wide range of bias.

Index Terms: Graded-Channel, SOI MOSFET, Transconductance, Output Conductance, Device modeling.

1. INTRODUCTION

The significant advantages of fully depleted SOI MOSFETs over conventional bulk ones has made it a good alternative for low-power low-voltage applications due to their steeper subthreshold slope, reduced body factor and larger drain current [1]. From the analog design point of view, the SOI technology provides improved performance in terms of gain and frequency, due to the reduced junction capacitances provided by the buried oxide layer and the larger transconductance (g_m). Also the ratio between transconductance and drain current (g_m/I_{DS}) is appreciably improved in FD SOI devices due to the reduced body factor [2].

The Graded-Channel (GC) SOI nMOSFET is an asymmetric channel device that has been proposed and demonstrated to improve the SOI MOSFET analog characteristics [3, 4]. In this device, the threshold voltage ion implantation is performed at the source side only and the remaining channel is kept with the natural wafer doping concentration. This lightly doped region presents negative threshold voltage, and in a simplistic way, can be understood as an extension of the drain region for positive values of applied front gate voltage (V_{GF}), reducing the effective channel length ($L_{eff} \cong L - L_{LD}$, L being the mask channel length and L_{LD} the length of the lightly doped region, as presented in figure 1).

This channel engineering provides several advantages over the conventional SOI transistor, mainly for analog applications, such as enhanced drain breakdown voltage, larger transconductance, reduced drain output conductance (increasing the Early voltage) and improved breakdown voltage [3-5]. This potential of GC devices for analog applications has already been demonstrated in operational transconductance amplifiers [5] and current mirrors [6].

Aiming to explore the potential of this asymmetric channel device for the design of analog circuits, an analytical charge-based continuous model has been proposed for the simulation of DC characteristics of GC SOI devices, allowing accurate analog circuit simulation in all regimes of operation [7]. Despite good

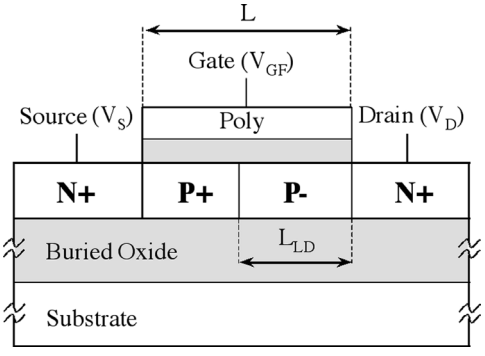

Figura 1. Cross-section of a Graded-Channel SOI nMOSFET.

agreement with experimental results was attained for the transconductance (g_m) and output conductance (g_D), in this model the derivatives of the drain current (I_{DS}) were obtained numerically. However, from the analog design point of view, the development of analytical continuous explicit expressions for the transconductance and the output conductance would be useful for design purposes.

In this work we present continuous charge-based analytical equations for the transconductance and output conductance of short-channel GC SOI nMOSFET, valid from weak to strong inversion. The equations include effects of channel length modulation, velocity saturation and drain induced barrier lowering. Experimental results were used to test the resulting expressions, achieving a good agreement.

2. GC SOI CHARGE-BASED CURRENT MODEL

Considering a steep transition of the doping concentration at the boundary of highly and lightly doped regions of the channel, the GC SOI transistor can be interpreted as a series association of two uniformly doped SOI transistors, each representing one part of the channel – highly doped (HD) and lightly doped (LD), as proposed in [8]. Therefore, as proposed in [7], the GC SOI drain current (I_{DS}) can be obtained computing that of a conventional SOI transistor [9] corresponding to the highly doped part of the channel and including short-channel effects such as mobility reduction, channel length modulation and carrier velocity saturation (equation 1). This channel region acts as a main transistor, whose drain voltage, $V_{D,HD}$, is a fraction of the drain bias, V_D, applied to the GC structure, and is dependent on the characteristics of both regions.

$$I_{DS} = \frac{W}{L_{eff}} \frac{\mu_n}{1 + V_{DE}\dfrac{\mu_n}{L_{eff} v_{sat}}} \times \left[v_T \left(Q_{D,HD} - Q_{S,HD} \right) - \frac{Q_{D,HD}^{\ 2} - Q_{S,HD}^{\ 2}}{2nC_{oxf}} \right] \quad (1)$$

where W is the channel width, L_{eff} is the effective channel length, equal to $L - L_{LD} - \Delta L - L_{sat}$ (ΔL is the lateral diffusion length and L_{sat} the length of the saturated region), V_{DE} is the main transistor effective drain voltage, v_{sat} is the saturation velocity, v_T is the thermal voltage, n is the body factor, C_{oxf} is the gate oxide capacitance per unit of area, μ_n is the inversion layer mobility, given by equation (2), as in [9].

$$\mu_n = \frac{\mu_0}{1 + \alpha \left| E_{n,eff} \right|} \quad (2)$$

where α is the scattering constant, μ_0 is the low-field mobility, which accounts for the mobility dependency on doping concentration and $E_{n,eff}$ is the average normal field in the channel, given by

$$E_{n,eff} = \frac{2\Phi_F + (V_S + V_{DE})/2}{t_{Si}} + B_E - \frac{(Q_S + Q_D)/2}{2\varepsilon_{Si}}$$

where

$$B_E = -\frac{Q_{depl}}{2C_{oxb} t_{Si}} \left(\frac{1}{1 + C_{Si}/C_{oxb}} + 1 \right) - \frac{V_{GB}}{\left(1 + C_{Si}/C_{oxb}\right) t_{oxb}}$$

and $Q_{depl} = -qN_a t_{Si}$ (N_a is the doping concentration, t_{Si} is the silicon film thickness), t_{oxb} is the buried oxide thickness, C_{Si} and C_{oxb} being the silicon film capacitance and buried oxide capacitance per unit area, respectively.

In equation (1), $Q_{D,HD}$ and $Q_{S,HD}$ are the inversion charge densities at the drain and source edges of the highly doped region, given by

$$Q_{i,HD} = C_{oxf} n v_T \left(1 - \sqrt{1 + \frac{4 Q_{i2,HD}^{\ 2}}{\left(C_{oxf} n v_T \right)^2}} \right) \quad (3a)$$

where

$$Q_{i2,HD}^{\ 2} = -C_{oxf} n v_T S_{NT} \cdot ln \left[1 + \sqrt{\frac{-Q_0/(2C_{oxf})}{n v_T S_{NT}^2}} \cdot e^{K1} + e^{K2} \right] \quad (3b)$$

and i=D for charge density at the drain edge and i=S at the source, S_{NT} (<1) is a fitting parameter that controls the transition between weak and strong inversion regimes,

$$K1 = \frac{V_{GF} - V_{thfl} - nV(y)}{2nv_T} \quad \text{and} \quad K2 = \frac{V_{GF} - V_{thf} - nV(y)}{2nv_T S_{NT}},$$

where V(y) is the channel potential drop, equal to V_{DE} and V_S, respectively, at $y = L - L_{LD}$ and $y = 0$, V_{thf} and V_{thfI} being the equivalent threshold voltages in strong and weak inversion regimes, Q_0 the inversion charge density at $V_{GF} = V_{thfI}$ [9] and V_{GF} the applied front gate voltage. The V_{DE} voltage, which corresponds to the drain voltage that effectively reaches the so-called "virtual" drain of the highly doped part of the channel [4], can be calculated as

$$V_{DE} = V_{DSAT} - V_{DSAT} \frac{ln\left[1 + exp\left(A_{TS} \left(1 - \dfrac{V_{D,HD}}{V_{DSAT}} \right) \right) \right]}{ln\left[1 + exp(A_{TS}) \right]} \quad (4)$$

where A_{TS} is a fitting parameter that controls the transition from triode to saturation regions, V_{DSAT} is the saturation voltage and $V_{D,HD}$ is the potential drop on the highly doped region, obtained as a function of bias, geometry, threshold voltage and mobility of both channel regions, as proposed in [7].

3. TRANSCONDUCTANCE AND OUTPUT CONDUCTANCE EQUATIONS DEVELOPMENT

Although analytical charge-based continuous expressions for the transconductance and output conductance of FD SOI MOSFETs have been proposed in [9], they are valid only for long-channel devices. According to this work, after including short-channel effects in the SOI charge-based model, simple analytical expressions cannot be applied to obtain the derivatives of the drain current, making the differentiation of I_{DS} more convenient. Therefore, in this paper, we have obtained analytical expressions for the transconductance (g_m) and output conductance (g_D) of GC SOI devices, by analytically differentiating the drain current of the main transistor (equation (1)) with respect to V_{GF} or V_D:

$$\frac{dI_{DS}}{dV_x} = \frac{W}{L_{eff}} \frac{\mu_n}{1+V_{DE}\dfrac{\mu_n}{L_{eff}v_{sat}}} \times \left[v_T\left(\frac{dQ_{D,HD}}{dV_x} - \frac{dQ_{S,HD}}{dV_x}\right) - \frac{\dfrac{Q_{D,HD}dQ_{D,HD}}{dV_x} - \dfrac{Q_{S,HD}dQ_{S,HD}}{dV_x}}{nC_{oxf}} \right] + \frac{W}{L_{eff}} \left[\frac{\dfrac{d\mu_n}{dV_x}}{1+V_{DE}\dfrac{\mu_n}{L_{eff}v_{sat}}} + \frac{\mu_n}{L_{eff}v_{sat}} \left(\frac{\dfrac{dV_{DE}}{dV_x}\mu_n + \dfrac{d\mu_n}{dV_x}V_{DE}}{\left(1+V_{DE}\dfrac{\mu_n}{L_{eff}v_{sat}}\right)^2} \right) \right] \times \left[v_T\left(Q_{D,HD} - Q_{S,HD}\right) - \frac{Q_{D,HD}^2 - Q_{S,HD}^2}{2nC_{oxf}} \right] \quad (5)$$

where V_x is equal to V_{GF} for the transconductance equation and V_D for the output conductance. It is worthwhile noting that, in the above equation, the effect of the GC structure over the effective drain voltage the inversion charge density at the drain edge of the main transistor is considered by means of $Q_{D,HD}$. As can be seen from equation (5), g_m and g_D are function of the mobility, effective drain voltage and inversion charge density derivatives, being the last one given by equation (6). In this equation, one can note that the derivative of $Q_{i,HD}$ with respect either to V_{GF} or V_D, is expressed as a function only of the derivatives of K1 and K2.

$$\frac{dQ_i}{dV_x} = \frac{-4S_{NT}^2 \cdot ln\left[1+\dfrac{\dfrac{-Q_0}{C_{oxf}}e^{K1}+e^{K2}}{nv_TS_{NT}}\right] \times \left(\dfrac{\dfrac{-Q_0}{C_{oxf}}e^{K1}\dfrac{dK1}{dV_x}+e^{K2}\dfrac{dK2}{dV_x}}{nv_TS_{NT}}\right)}{\sqrt{1+\dfrac{4}{\left(nC_{oxf}v_T\right)}\left[-nC_{oxf}v_TS_{NT}\,ln\left(1+\dfrac{\dfrac{-Q_0}{C_{oxf}}e^{K1}+e^{K2}}{nv_TS_{NT}}\right)\right]^2 \times \left(1+\dfrac{\dfrac{-Q_0}{C_{oxf}}e^{K1}+e^{K2}}{nv_TS_{NT}}\right)}} \quad (6)$$

A. Transconductance

It can be numerically verified that the term $\left(1+V_{DE}\dfrac{\mu_n}{L_{eff}v_{sat}}\right)^{-1}$ in the drain current equation has a small impact on the derivative of the term $\left(\dfrac{W}{L_{eff}}\dfrac{\mu_n}{1+V_{DE}\dfrac{\mu_n}{L_{eff}v_{sat}}}\right)$ when the drain voltage is kept constant. Therefore, its derivative with respect to V_{GF} has been neglected. As a result, equation (5) turns to equation (7), to obtain the transconductance of a GC device.

$$g_m = \frac{dI_{DS}}{dV_{GF}} = \frac{W}{L_{eff}} \frac{\mu_n}{1+V_{DE}\dfrac{\mu_n}{L_{eff}v_{sat}}} \left[v_T\left(\frac{dQ_{D,HD}}{dV_{GF}} - \frac{dQ_{S,HD}}{dV_{GF}}\right) - \frac{Q_{D,HD}\dfrac{dQ_{D,HD}}{dV_{GF}} - Q_{S,HD}\dfrac{dQ_{S,HD}}{dV_{GF}}}{nC_{oxf}} \right] + \frac{\dfrac{d\mu_n}{dV_{GF}}}{1+V_{DE}\dfrac{\mu_n}{L_{eff}v_{sat}}} \frac{W}{L_{eff}} \left[v_T\left(Q_{D,HD} - Q_{S,HD}\right) - \frac{Q_{D,HD}^2 - Q_{S,HD}^2}{2nC_{oxf}} \right] \quad (7)$$

where $\dfrac{d\mu_n}{dV_{GF}} = \dfrac{\mu_0\alpha A}{(1+\alpha E_{eff})^2}$ and $A = \dfrac{dQ_{S,HD}}{dV_{GF}}\left(\dfrac{2\varepsilon_{Si}+t_{Si}nC_{oxf}}{4\varepsilon_{Si}t_{Si}nC_{oxf}}\right) + \dfrac{dQ_{D,HD}}{dV_{GF}}\left(\dfrac{1}{4\varepsilon_{Si}}\right)$. In this case, the term $\dfrac{dQ_{S,HD}}{dV_{GF}}$ is calculated with $\dfrac{dK1}{dV_{GF}} = \dfrac{1}{2nv_T}$ and $\dfrac{dK2}{dV_{GF}} = \dfrac{1}{2nv_TS_{NT}}$.

On the other hand, $\dfrac{dQ_{D,HD}}{dV_{GF}}$ is obtained with $\dfrac{dK1}{dV_{GF}} = \dfrac{1-n\dfrac{dV_{DE}}{dV_{GF}}}{2nv_T}$ and $\dfrac{dK2}{dV_{GF}} = \dfrac{1-n\dfrac{dV_{DE}}{dV_{GF}}}{2nv_TS_{NT}}$ that are dependent on the derivative of the effective drain voltage of the highly doped transistor (dV_{DE}/dV_{GF}), which will be shown below and includes the effect of the saturation voltage (V_{DSAT}) due to carrier velocity saturation. However, the derivative of V_{DE} (which is a function of V_{DSAT}, that is a mobility-dependent parameter) depends on the term A, which in turn is a function of the derivative of $Q_{D,HD}$. In order to make the model explicit, we have used the approximation $\dfrac{dV_{DE}}{dV_{GF}} \cong -\dfrac{dQ_{S,HD}}{dV_{GF}}\dfrac{1}{nC_{oxf}}$ to estimate the term A [9] and afterwards we obtained a new and more accurate expression for the derivative of V_{DE} (equation 8).

$$\frac{dV_{DE}}{dV_{GF}} = \frac{dV_{DSAT}}{dV_{GF}} - \frac{dV_{DSAT}}{dV_{GF}} \frac{1}{ln(1+e^{ATS})} ln\left[1+e^{ATS\left(1-\frac{V_{D,HD}}{V_{SAT}}\right)}\right]$$
$$-V_{SAT} \times \frac{ATS \cdot e^{ATS\left(1-\frac{V_{D,HD}}{V_{SAT}}\right)} \cdot \left[\frac{dV_{D,HD}}{dV_{GF}} V_{SAT} + \frac{dV_{DSAT}}{dV_{GF}} V_{D,HD}\right]}{V_{DSAT}^2 \cdot ln\left(1+e^{ATS}\right) \cdot \left(1+e^{ATS\left(1-\frac{V_{D,HD}}{V_{SAT}}\right)}\right)} \quad (8)$$

where $\frac{dV_{DSAT}}{dV_{GF}} = v_T \cdot \frac{e^{\frac{V_{SAT}-v_T}{v_T}} \times B}{1+e^{\frac{V_{SAT}-v_T}{v_T}}}$ V_{SAT} is the saturation voltage in strong inversion only [9] and

$$B = \frac{v_{sat}L_{eff}}{\mu_0}\alpha A + \frac{1}{\sqrt{\left(\frac{v_{sat}L_{eff}}{\mu_n}\right)^2 + 2\frac{v_{sat}L_{eff}}{\mu_n}\frac{(-Q_{S,HD})}{C_{oxf}n}}}$$
$$\times\left(-\frac{\alpha A\left(v_{sat}L_{eff}\right)^2\left(1+\alpha E_{eff}\right)^2}{\mu_0^2}\right.$$
$$\left.+\frac{\alpha A v_{sat}L_{eff}}{\mu_0}\frac{Q_{S,HD}}{C_{oxf}n} - \frac{v_{sat}L_{eff}}{\mu_n}\frac{dQ_{S,HD}}{dV_{GF}}\frac{1}{C_{oxf}n}\right)$$

As mentioned before, the parameter $V_{D,HD}$ is the voltage drop across the highly doped part of the channel. Although this parameter can be calculated as proposed in [7], its derivative results in complicated equations, and it has been approximated to [10]

$$V_{D,HD} \cong \frac{V_D}{1+\frac{\mu_n L_{LD}(V_{GT,HD})}{\mu_{nLD}L_{eff}(V_{GT,LD})}} \quad (9)$$

where μ_{nLD} is the mobility of the lightly doped region, and $V_{GT,j}=V_{GF} - V_{thf,j}$ is the gate voltage overdrive of each channel region (j=HD for highly doped and j=LD for lightly doped). Naming $C = \mu_n L_{LD} V_{GT,HD}$ and $D= \mu_{nLD} L_{eff} V_{GT,LD}$, the differentiation of equation (9) with respect to V_{GF} leads to

$$\frac{dV_{D,HD}}{dV_{GF}} \cong \frac{-V_D\left\{D\cdot\left[L_{LD}V_{GT,HD}\frac{d\mu_n}{V_{GF}} + L_{LD}\mu_n\right] + C\cdot\left[L_{eff}V_{GT,LD}\frac{d\mu_{nLD}}{dV_{GF}} + L_{eff}\mu_{nLD}\right]\right\}}{\left(1+\frac{C}{D}\right)^2 \times C^2} \quad (10)$$

being $\frac{d\mu_{nLD}}{dV_{GF}}$ calculated using the same expression applied for $\frac{d\mu_n}{V_{GF}}$, replacing μ_0 and α, which are doping-dependent, by their respective values for the lightly doped region and considering $\frac{dQ_{S,LD}}{dV_{GF}} \cong -nC_{oxf}$ and $\frac{dQ_{D,LD}}{dV_{GF}} \cong 0$ (see [9]).

B. Output Conductance

Differently from the differentiation of I_{DS} with respect to V_{GF}, varying the drain bias, the derivative of the term $\left(\frac{W}{L_{eff}}\frac{\mu_n}{1+V_{DE}\frac{\mu_n}{L_{eff}v_{sat}}}\right)$ has a great influence on the value of g_D and has to be considered when differentiating equation (1) with respect to V_D. As a result, the output conductance of GC SOI devices can be expressed by equation (5), replacing V_x with V_D.

The differentiation of the inversion charges with respect to V_D is similar to the differentiation with V_{GF}. However, in this case, the effect of drain induced barrier lowering (DIBL) must be included, through the parameter σ ($V_{thf} = V_{thf0} - \sigma V_D$, V_{thf0} being the threshold voltage of a long-channel transistor). Therefore, the term $\frac{dQ_{S,HD}}{dV_D}$ calculated with $\frac{dK1}{dV_D} = \frac{\sigma}{2nv_T}$ and $\frac{dK2}{dV_D} = \frac{\sigma}{2nv_T S_{NT}}$. In $\frac{dQ_{D,HD}}{dV_D}$, $\frac{dK1}{dV_D} = \frac{1}{2nv_T}\left(\sigma - n\frac{dV_{DE}}{dV_D}\right)$ and $\frac{dK2}{dV_D} = \frac{1}{2nv_T S_{NT}}\left(\sigma - n\frac{dV_{DE}}{dV_D}\right)$. Once again, the derivative of the inversion charge density at the drain is dependent on the effective drain voltage V_{DE}, which includes the effect of saturation velocity and can be obtained through equation (6). Again, $V_{D,HD}$ was simplified through equation (9), resulting in

$$\frac{dV_{D,HD}}{dV_D} \cong \left(1+\frac{\mu_n L_{LD}(V_{GT,HD})}{\mu_{nLD}L_{eff}(V_{GT,LD})}\right)^{-1} \quad (11)$$

Both equations, for g_m and g_D, are valid for any bias condition of the GC operation and result in very accurate expressions for the transconductance and output conductance of GC devices, without the need of obtaining drain current curves, as will be shown in the next section.

4. RESULTS AND DISCUSSION

The proposed set of equations was verified against experimental measurements of fabricated GC SOI nMOSFETs. Starting from a SOI wafer with doping concentration of 10^{15} cm^{-3} and buried oxide thickness of 390nm, devices were fabricated with a 30nm-thick gate oxide in a silicon layer with final thickness of 80nm. The threshold voltage ion implantation led to a body concentration level of about 10^{17} cm^{-3}. The measured devices have channel width of 18μm, length of 0.5μm and 0.8μm, and different

L_{LD}/L ratios. A conventional SOI device with L=0.5μm has also been measured for comparison purposes. The measurements were performed using a HP4145B semiconductor parameter analyzer and long integration time. The relation L_{LD}/L has been experimentally obtained from I_{DS} versus V_{DS} curves, according to the procedure described in [4]. By using the proposed model, devices with the same dimensions and doping concentrations of the measured ones were simulated. For all performed comparisons, the required model parameters were obtained as presented in [7].

Transconductance curves are presented in figure 2 as a function of the gate voltage overdrive (V_{GT}) with applied V_{DS} of 0.1V and 1.5V for GC SOI nMOSFETs with L=0.5μm and L_{LD}/L=0.16, 0.29 and 0.53, which correspond to effective channel lengths of 0.42, 0.35 and 0.24μm, respectively.

As illustrated in figure 2, the proposed equation is able to describe the increase of maximum g_m and its larger degradation reported in [4] as L_{LD}/L increases. Besides, one can note that the g_m calculated using the proposed equation (lines) agrees very well with the experimental results (symbols), both in triode (A) (V_{DS}=0.1V) and saturation (B) (V_{DS}=1.5V).

By using the proposed g_D equation and numerically differentiating the measured drain current curves as a function of drain bias of GC devices with L=0.5μm, the curves of the output conductance were obtained, varying the L_{LD}/L ratio with V_{GT} of 200mV (figure 3A). From the presented curves one can note the reduction of g_D provided by the channel engineering in comparison to the conventional transistor. Even the device with L_{LD}/L=0.53, which suffers from short-channel effects (L_{eff}=0.24μm), presents smaller g_D than the conventional transistor. Figure 3B presents the output conductance obtained varying the gate bias for a 0.5μm-long GC device with L_{LD}/L=0.28, which emphasizes the capability of the proposed equation to describe g_D in a wide range of bias, from weak to strong inversion, except in the region where the parasitic bipolar transistor starts to act, which was not in the scope of this work and usually is not a region of interest for analog circuits.

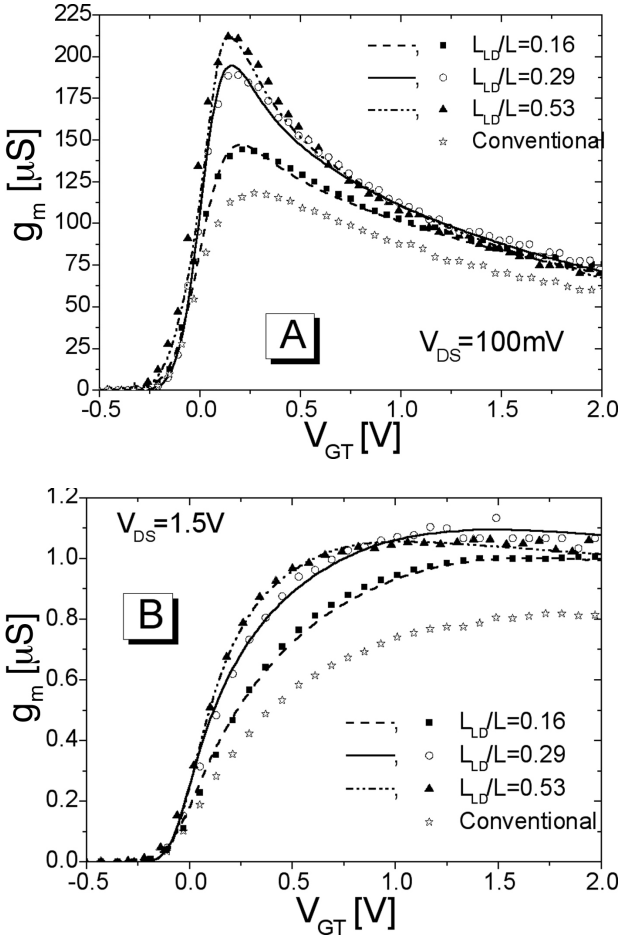

Figure 2. Measured (symbols) and modeled (lines) transconductance as a function of the gate voltage overdrive for 0.5μm-long devices.

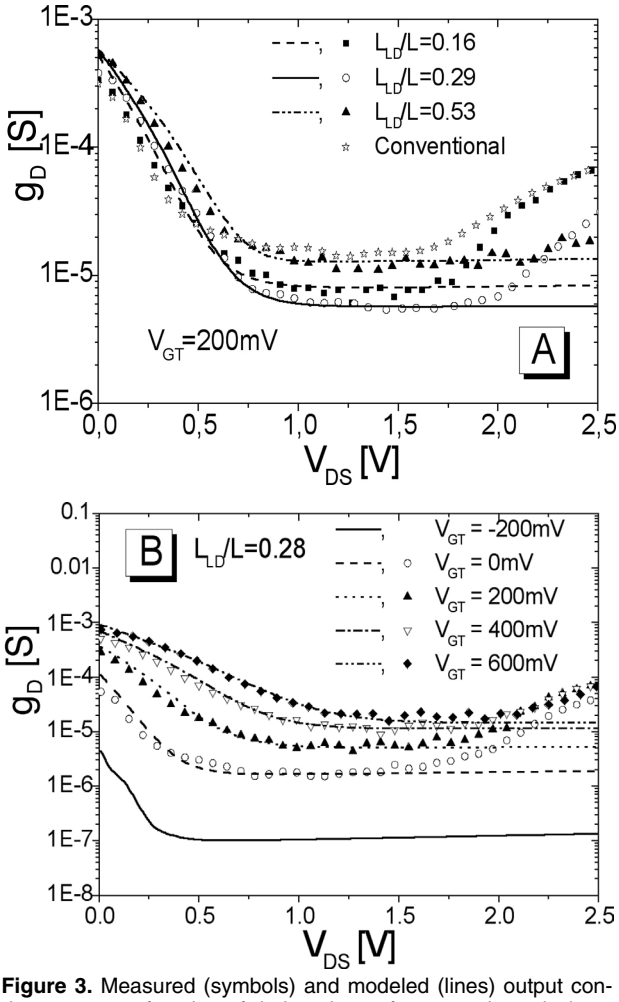

Figure 3. Measured (symbols) and modeled (lines) output conductance as a function of drain voltage, for 0.5μm-long devices, at V_{GT} of 200mV (A) and at different V_{GT} for a GC device with L_{LD}/L=0.28 (B).

After validating the proposed equations by comparing the transconductance and output conductance curves, important parameters for analog applications were also obtained. The transconductance over the drain current (g_m/I_{DS}) ratio is an important parameter for analog design, since is marks the transistor efficiency of converting bias current into transconductance. Figure 4 presents the comparison between g_m/I_{DS} as a function of the scaled drain current ($I_{DS}/W/L_{HD}$) obtained through measurements (symbols) and the equation developed in this work (lines) for 0.8μm-long GC transistors with L_{LD}/L=0.27 and 0.39 (effective channel length of 0.58 and 0.49μm, respectively), obtained at V_{DS} = 1.5V. For the case of the modeled results, the drain current was obtained through equation (1), with V_{DE} calculated as proposed in [7]. The presented results stress the continuity of the proposed equation in all regions of device operation.

By using the calculated g_D, presented in figure 3A, and the drain current obtained through the model proposed in [7] (equation 1), the curves of I_{DS}/g_D as a function of V_{DS} (which, in the saturation region, represents the Early voltage, V_{EA}) were plotted and are presented in figure 5. Besides the good matching between modeled and measured results, one can point out the improvement on the Early voltage provided by the presence of the lightly doped region near the drain. In the worst case (L_{LD}/L=0.53) there is an improvement of about twice in the value of V_{EA} in comparison with the conventional device.

Classically, the intrinsic voltage gain (A_V) of a single transistor is given by the ratio g_m/g_D [2]. From the available experimental curves, the values of experimental gain were obtained for the 0.5μm long GC SOI transistors at V_{DS}=0.8 and 1.5V with V_{GT}=200, 500 and 800mV. By using the proposed equations the curves of A_V were obtained. The results are presented in figure 6 as a function of V_{GT}, being the open symbols the experimental results with V_{DS}=0.8V and the solid symbols the results with V_{DS}=1.5V. The presented curves allow noting the increase in the gain provided by the GC structure. Considering the worst case, there is an improvement of at least 6.5 dB when the devices are biased at V_{GT}=200mV and V_{DS}=0.8V and at least 8.5 dB at V_{DS}=1.5V and the same V_{GT}.

5. CONCLUSION

This work presented analytical continuous expressions for the transconductance and output conductance of short-channel GC SOI nMOSFETs. Short-channel effects such as mobility degradation, channel length modulation, velocity saturation and drain induced barrier lowering have been included in

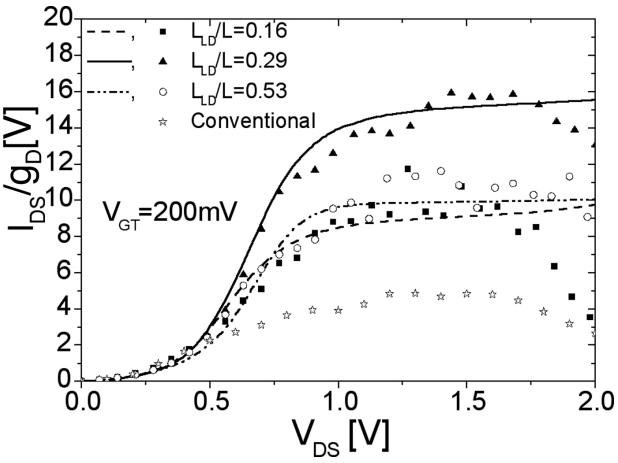

Figure 5. Measured (symbols) and modeled (lines) drain current over output conductance (I_{DS}/g_D) as a function of drain bias obtained at V_{GT}=200mV.

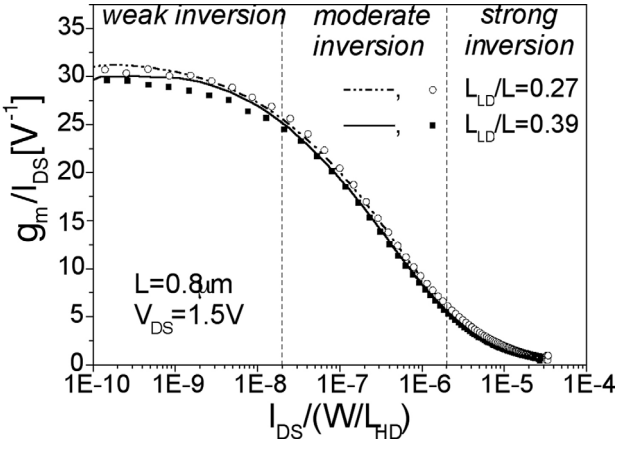

Figure 4. Measured (symbols) and modeled (lines) transconductance over drain current curves as a function of the scaled drain current obtained at V_{DS}=1.5V.

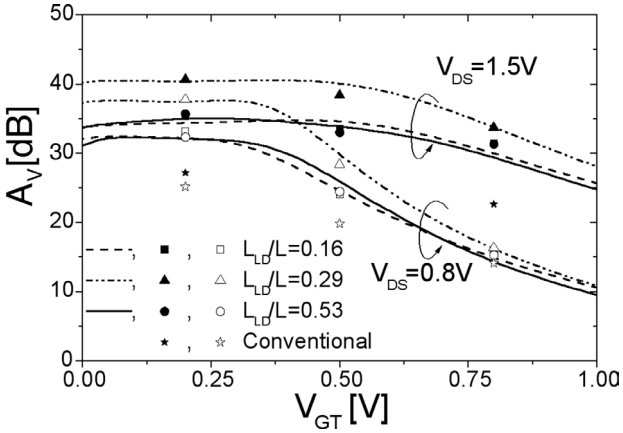

Figure 6. Experimental (symbols) and modeled (lines) DC open-loop voltage gain as a function of V_{GT} for devices with L=0.5um biased at V_{DS}=0.8V and V_{DS}=1.5V.

the proposed set of equations. The proposed equations results were verified against experimental data, providing an accurate description of the transconductance and output conductance under several bias conditions. The transconductance over drain current ratio, Early voltage and open-loop voltage gain were also used to verified the model capability for analog design purposes. For all performed comparisons, a good agreement was achieved in all regions of operation, with smooth transitions between different regions of device operation.

ACKNOWLEDGEMENTS

The authors would like to acknowledge FAPESP and M. A. Pavanello acknowledges CNPq for the financial support to the execution of this work. The authors are indebted to Dr. Denis Flandre, from UCL, Belgium, for supplying the devices.

REFERENCES

[1] J. P. Colinge. Silicon-On-Insulator Technology: Materials to VLSI, 3rd ed. Massachusetts: Kluwer Academic Publishers; 2004.
[2] D. Flandre, J. P. Eggermont, D. De Ceuster, P. Jespers. Electronics Letters, v. 30, n. 23, p. 1933 (1994).
[3] M. A. Pavanello, J. A. Martino, D. Flandre. Solid-State Electronics, v. 44, n. 7, p. 1219 (2000).
[4] M. A. Pavanello, J. A. Martino and D. Flandre, Solid-State Electronics, vol. 44, n. 6, p. 917 (2000).
[5] M. A. Pavanello, J. A. Martino, D. Flandre. Solid-State Electronics, v. 46, n.8, p. 1215 (2002).
[6] M. A. Pavanello, J. A. Martino, D. Flandre. In Proceedings of Silicon-On-Insulator Technology and Devices 2001; p. 319-324 (2001).
[7] M. de Souza, M. A. Pavanello, B. Iñiguéz and D. Flandre. Solid-State Electronics, vol. 49, n.10, pp. 1683-1692 (2005).
[8] M. A. Pavanello, B. Iñiguez, J. A. Martino and D. Flandre, *4th IEEE Int. CaracasConference on Devices, Circuits and Systems,* Aruba, D030-1 (2002).
[9] B. Iñíguez, L. F. Ferreira, B. Gentinne B and D. Flandre D. *IEEE Transactions on Electron Devices*, vol. 43, pp. 568-575 (1996).
[10] M. de Souza, M. A. Pavanello, B. Iñíguez and D. Flandre, in Microelectronics Technology and Devices, SBMicro 2004, *The Electrochemical Society Proceedings*, Vol. 2004, pp. 27-32 (2004).