Study of Matching Properties of Graded-Channel SOI MOSFETs

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ABSTRACT

In this paper an overall analysis on the matching properties of Graded-Channel (GC) SOI MOSFETs in comparison to conventional SOI transistors is performed. Experimental results show that GC devices present poorer matching behavior in comparison to conventional SOI counterpart for equal mask channel length, whereas for same effective channel length, almost the same matching behavior. The analytical model for the drain current of GC devices is used to investigate the reasons for this matching worsening. Two-dimensional numerical simulations are used to validate the model-based analysis both in linear and saturation regions.

Index Terms: Silicon-on-Insulator, Graded-Channel, Mismatch, Charge-Based Model, MOSFET.

1. INTRODUCTION

The concept of matched devices is one of the most important features in analog circuit design, as most analog circuits operation rely on the similarity of electrical behavior of close devices [1]. However, in practice, the characteristics of designed matched transistors are slightly different. Therefore, the design of precise analog circuits requires studies into the matching behavior of devices in order to yield a good understanding of the physical phenomena of device variations and its impact on the circuit performance.

The Graded-Channel (GC) SOI nMOSFET is a device with asymmetric doping channel profile, proposed to improve the SOI analog characteristics [2]. By simply using a mask arrangement in the standard SOI CMOS process, the threshold voltage ion implantation is performed at the source side only, keeping the remaining channel, at the drain side, with the natural wafer doping concentration. This so-called lightly doped region presents negative threshold voltage and, in a simplistic way, can be understood as an extension of the drain region for positive values of applied front gate voltage (V_{GF}), reducing the effective channel length ($L_{eff} = L - L_{LD}$, L being the mask channel length and L_{LD} is the length of the lightly doped region). Figure 1 presents the cross section of a GC SOI nMOSFET.

Previous works reported several GC devices advantages over conventional ones for analog applications [2, 3, 4], namely larger transconductance (g_m), reduced drain output conductance (g_D) and appreciable reduction in the harmonic distortion [5], as already demonstrated in analog circuits such as operational transconductance amplifiers [6] and current mirrors [7].

Despite the advantages of this transistor for analog applications, few information of matching properties of GC SOI transistors is known [8]. In this work an overall evaluation of the impact of the GC channel engineering on the matching properties of SOI transistor will be presented.

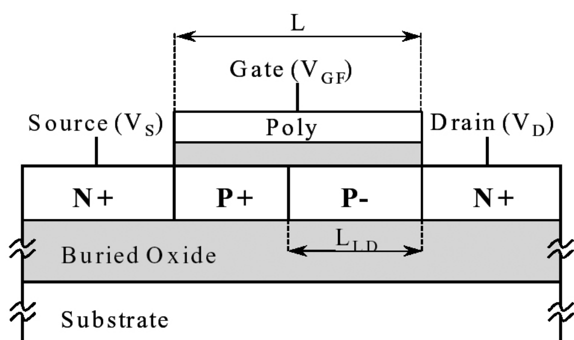

Figure 1: Cross-section of a Graded-Channel SOI nMOSFET.

Experimental results are shown to support this analysis. In order to investigate the components of mismatching that are influenced by this specific graded-channel engineering, the analytical model for the drain current of GC devices is used, and two-dimensional numerical simulations were also performed aiming to predict the matching behavior both in linear and saturation region. Section 2 describes the main characteristics of the devices used in this work. Section 3 demonstrates matching properties extracted from the performed experimental measurements. Sections 4 and 5 present the model-based and two-dimensional based matching study, respectively. The conclusions of this work are pointed-out in Section 6.

2. DEVICES CHARACTERISTICS AND MEASUREMENTS

In order to evaluate matching properties of GC transistors, test structures including arrays of 10 transistors with channel width (W) of 20μm, mask channel length of 2μm and different L_{LD}/L ratios were fabricated. The distance between two consecutive transistors is 32 μm and the total distance between the first and the last one is of 288μm. These structures were fabricated by starting from a SOI wafer with doping concentration ($N_{a,LD}$) of 10^{15} cm^{-3} and buried oxide thickness (t_{oxb}) of 390nm, with a 30nm thick gate oxide (t_{oxb} and silicon layer with final thickness of (t_{Si}) 80nm. The threshold voltage ion implantation led to a body concentration level of about ($N_{a,HD}$) 6 x 10^{16} cm^{-3}.

The experimental curves were obtained for a single chip, with a Keithley 4200 Semiconductor Characterization System with medium integration time. The relation L_{LD}/L has been experimentally obtained from I_{DS} *versus* V_{DS} curves, according to the procedure described in ref. [4].

3. EXPERIMENTAL RESULTS

The most important MOSFET parameters at DC operation are the threshold voltage, the current factor and body factor [1], thus, variations in these parameters must be evaluated. However, since the source and substrates are connected in most applications, the body factor mismatch can be neglected [1]. Therefore, the relative mismatch in the drain current (ΔI_{DS} / I_{DS}) can be expressed as a function of the mismatch in the threshold voltage (ΔV_T) and current factor ($\Delta\beta$ / β), as shown in equation (1) [9]:

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{1}{I_{DS}}\frac{dI_{DS}}{dV_T}\Delta V_T + \frac{\Delta\beta}{\beta} \quad (1)$$

The threshold voltage variation is a result of random mismatch of technological parameters such as doping concentration, silicon film and gate oxide thickness [10], and is usually said to be the drain current mismatch component that dominates when devices operate in weak inversion [11]. In modern MOS processing, the gate oxide and silicon film present small variation, which makes the doping concentration variation the main source of threshold voltage mismatch [1]. The doping concentration variation refers both to the original wafer doping concentration and posterior modifications through ion implantation for threshold voltage adjust.

From the experimental I_{DS} *versus* V_{GF} curves obtained with small applied drain voltage (V_{DS}=25mV), the threshold voltage has been extracted using the double derivative method [12]. The I_{DS} *versus* V_{GF} curves were measured with 2 mV step in order to improve accuracy on threshold voltage extraction.

Table I presents the extracted values of mean V_T ($V_{T,mean}$) and standard deviation (σ_{V_T}) for several GC devices, a conventional and an undoped device with the same mask channel length (L=2μm and W=20μm). From the presented results one can note that the undoped device (L_{LD}/L=1) presents smaller V_T variation than the conventional one (L_{LD}/L=0), confirming that the deviation of doping concentration increases when ion implantation is applied. In addition, it is possible to see the decrease of V_T, and the standard deviation rise, in graded-channel devices both due to the effective channel reduction with L_{LD}/L increase.

According to ref. [1], the standard deviation of threshold voltage can be expressed by equation (2) where σ_{0V_T} is the normalized threshold voltage standard deviation.

$$\frac{\sigma_{0V_T}}{V_{T,mean}} = \frac{\sigma_{0V_T}}{V_{T,mean}\sqrt{W \times L}} \quad (2)$$

The above equation shows a proportionality of the standard deviation with the inverse square root of the gate area. As expected, the larger the size, the smaller the variation of the threshold voltage.

Table I. Matching Data for the Threshold Voltage of Different GC SOI devices (W=20μm and L=2μm).

Parameter	$V_{T,mean}$ [mV]	σ_{V_T} [mV]
L_{LD}/L= 0 (Conventional SOI)	412.2	6.2
L_{LD}/L=0.15	389.4	6.4
L_{LD}/L=0.35	380.6	6.9
L_{LD}/L=0.42	379.0	7.6
L_{LD}/L=0.72	314.4	8.7
L_{LD}/L=1	-313.2	5.1

Figure 2 presents $\sigma_{V_T} / V_{T,mean}$ as a function of $(W.L_{eff})^{-1/2}$ for GC and conventional transistors. In this figure symbols correspond to the experimental data while the straight line is the result of linear regression intersecting the origin, which is in agreement with experimental data reported in refs. [13,14] for bulk MOS devices from different technologies.

Table II presents the values of normalized σ_{0V_T} and $\sigma_{0V_T}/V_{T,mean}$ calculated from the experimental data presented in Figure 2 and using equation (2), considering L_{eff} instead of the total channel length. As can be noted, as the L_{LD}/L increases, σ_{0V_T} decreases. However, the factor $\sigma_{0V_T}/V_{T,mean}$ does not present large variation, since the mean value of $V_{T,mean}$ also decreases with the effective channel length reduction. These results confirm that the larger threshold voltage deviation is related to the reduction of L_{eff} as L_{LD}/L increases. In addition, it indicates that, despite the reduced $V_{T,mean}$ and larger standard deviation, any difference between GC devices and the conventional one does not lie in the threshold voltage mismatch.

Figure 3 presents the current factor variation as a function of gate voltage overdrive ($V_{GT} = V_{GF} - V_T$) in order to neglect the threshold voltage differences between the studied devices. In these curves, the standard deviation has been calculated with respect to the measured current.

The presented results show that the drain current deviation increases as devices approach weak inversion (low values of V_{GT}). This increase in $\sigma_{I_{DS}}/I_{DS,mean}$ is related to the threshold voltage mismatch, that becomes more significant at low values of V_{GT} [11]. However, as the gate voltage is increased, $\sigma_{I_{DS}} / I_{DS,mean}$ tends to a constant value, which, in the 2μm-long Conventional SOI transistor, lies near to 1.15%. Besides, one can observe that the drain current variation increases with L_{LD}/L. It suggests that the current factor in GC devices is more susceptible to variations than in the conventional SOI transistor. As the effective channel length decreases with L_{LD}/L increase, one can expect that a given effective channel length variation will be more significant, causing the larger mismatch in the drain current of GC SOI transistors than in the conventional one with the same mask channel length.

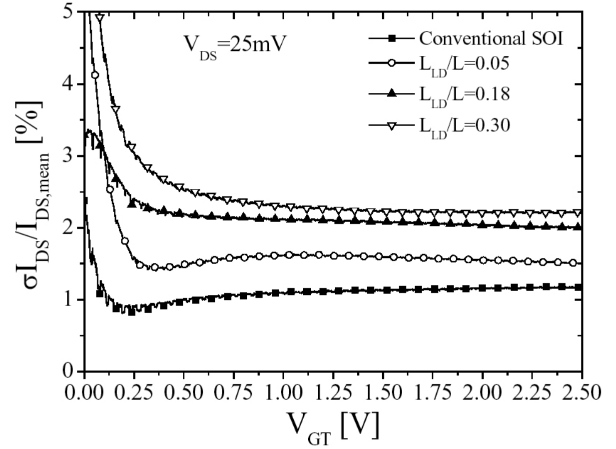

Figure 3. Drain current mismatch as a function of the gate voltage overdrive at low drain bias (V_{DS}=25mV).

Further investigation into the reasons for this worsening of matching, caused by the graded-channel engineering, will be presented in the next section, by using an analytical model, in order to analyse the components influencing the matching behavior.

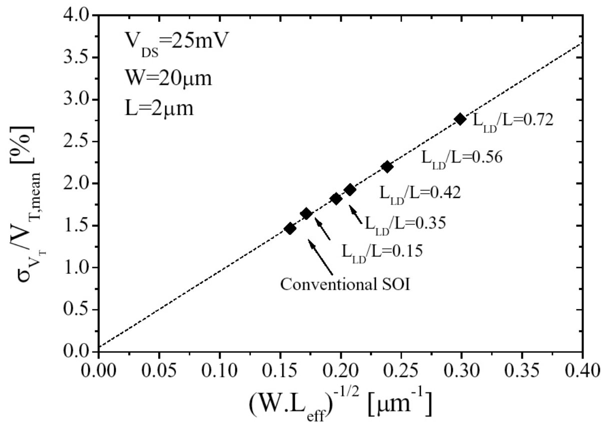

Figure 2. / $V_{T,mean}$ versus $(W.L_{eff})^{-1/2}$ for GC SOI devices varying the L_{LD}/L ratio.

Table II. Calculated σ_{0V_T} and $\sigma_{0V_T}/V_{T,mean}$ for the experimental data presented in Figure 2.

Parameter	σ_{0V_T} **[mV.μm]**	$\sigma_{0V_T}/V_{T,mean}$ **[μm]**
L_{LD}/L=0 (Conventional SOI)	39.21	0.0927
L_{LD}/L=0.15	37.32	0.0958
L_{LD}/L=0.42	36.68	0.0928
L_{LD}/L=0.56	35.24	0.0923
L_{LD}/L=0.72	29.12	0.0926

4. CHARGE-BASED ANALYTICAL MODEL MISMATCH ANALYSIS

In order to better understand the components that influence the matching in graded-channel transistors, analytical results provided by the continuous model for drain current of GC devices [15] were used.

This model considers a steep transition of the doping concentration at the boundary of highly and lightly doped regions of the channel. This way, the graded-channel transistor can be interpreted as a series association of two uniformly doped SOI transistors, each representing one part of the channel - highly doped (HD) and lightly doped (LD), as proposed in ref. [16]. Therefore, as presented in ref. [15], the GC SOI drain current (I_{DS}) can be obtained computing that of a conventional SOI transistor [17] correspon-

ding to the highly doped part of the channel. This channel region acts as a *main* transistor, whose drain voltage, $V_{D,HD}$, is a fraction of the drain bias, V_D, applied to the GC structure, and is dependent on the characteristics of both regions. The drain current, including short-channel effects such as mobility reduction, channel length modulation and carrier velocity saturation is then given by equation (3).

$$I_{DS} = \beta \cdot k_Q \tag{3}$$

where $\beta = \dfrac{\mu_n}{1 + V_{DE}\dfrac{\mu_n}{L_{eff} v_{sat}}} C_{oxf} \dfrac{W}{L_{eff}}$ and

$$k_Q = \left[v_T C_{oxf}\left(Q_{D,HD} - Q_{S,HD}\right) - \frac{Q_{D,HD}^{\ 2} - Q_{S,HD}^{\ 2}}{2n} \right]$$

, μ_n being the inversion layer mobility, C_{oxf} the gate oxide capacitance per unit of area, v_T the thermal voltage, V_{DE} the effective drain voltage, v_{sat} the saturation velocity, n the body factor and $Q_{D,HD}$ and $Q_{S,HD}$ the inversion charge densities at the drain and source edges of the highly doped region. $Q_{D,HD}$ and $Q_{S,HD}$ are given by equation (4).

$$Q_{i,HD} = C_{oxf} n v_T \times \left\{ 1 - \sqrt{1 + \frac{4\left[-C_{oxf} n v_T S_{NT} \cdot \ln\left(1 + \sqrt{\dfrac{-Q_0/(2C_{oxf})}{n v_T S_{NT}^{\ 2}}} \times e^{K1} + e^{K2} \right) \right]^2}{\left(C_{oxf} n v_T\right)^2}} \right\} \tag{4}$$

where i stands for D for charge density at the drain edge or S at the source, S_{NT} (<1) is a fitting parameter that controls the transition between weak and strong inversion regimes, $K1 = \dfrac{V_{GF} - V_{TI} - nV(y)}{2nv_T}$ and $K2 = \dfrac{V_{GF} - V_T - nV(y)}{2nv_T S_{NT}}$.

V(y) is the channel potential drop, equal to V_{DE} and V_S, respectively, at y = L-L_{LD} and y = 0, V_T and V_{TI} being the equivalent threshold voltages in strong and weak inversion regimes and Q_0 the inversion charge density at V_{GF} = V_{TI} [17]. The V_{DE} voltage, which corresponds to the voltage that effectively reaches the drain of the highly doped part of the channel, can be obtained through equation (5).

$$V_{DE} = V_{DS,SAT} - V_{DS,SAT} \frac{\ln\left[1 + \exp\left(A_{TS}\left(1 - \dfrac{V_{DS,HD}}{V_{DS,SAT}} \right) \right) \right]}{\ln\left[1 + \exp(A_{TS}) \right]} \tag{5}$$

with A_{TS} being a fitting parameter that controls the transition from triode to saturation regions, $V_{DS,HD}$ the drain-to-source voltage drop across the highly doped region, calculated as proposed in ref. [15] and $V_{DS,SAT}$ is the saturation voltage given by [18].

$$V_{DS,SAT} = 2v_T + n_T \times \left[\ln\left(1 + \exp\left(\frac{\left(\dfrac{v_{sat} L_{eff}}{\mu_n} + \sqrt{\left(\dfrac{v_{sat} L_{eff}}{\mu_n}\right)^2 + 2\dfrac{v_{sat} L_{eff}}{\mu_n}\dfrac{\left(-Q_{nf,S}\right)}{C_{oxf} n}} \right) - v_T}{v_T} \right) \right) \right] \tag{6}$$

The relative mismatch can then be expressed as a function of the mismatch in the current factor ($\Delta\beta / \beta$) and in the charge-dependent term of equation (3) ($\Delta k_Q / k_Q$), as shown in equation (7). It is worthwhile noting that any threshold voltage variation is included in the term ($\Delta k_Q / k_Q$), due to the charge dependency on V_T.

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta\beta}{\beta} + \frac{-\Delta k_Q}{k_Q} \tag{7}$$

In order to perform an analysis of these components, the model parameters were initially extracted as described in ref. [15] to fit typical drain current curves obtained from fabricated GC SOI transistors with W/L = 20μm/2μm and L_{LD}/L=0.25, 0.40 and 0.53. Figure 4 and 5 present the results of the comparison between I_{DS} *versus* V_{GF} at V_{DS}=100mV and I_{DS} *versus* V_{DS} at V_{GT}=200mV, respectively, demonstrating the good agreement between experimental and modeled results to support the model-based analysis (except at high V_{DS} when impact ionization effects become significant).

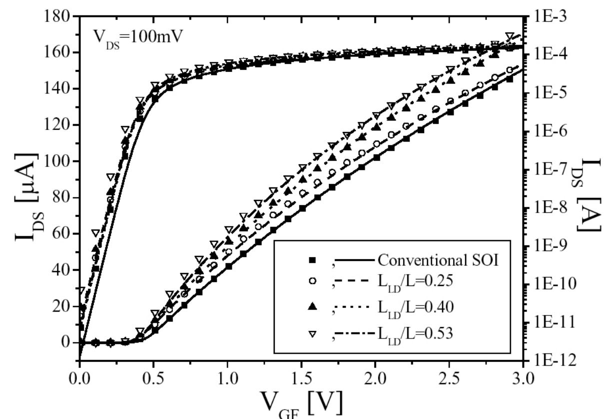

Figure 4. Comparison between typical measured (symbols) and modeled (lines) I_{DS} versus V_{GF} (V_{DS}=100mV).

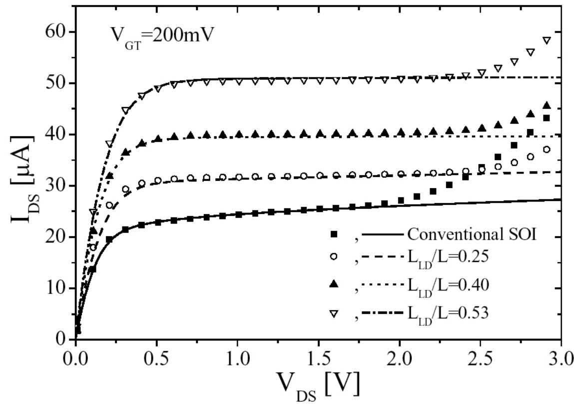

Figure 5. Comparison between typical measured (symbols) and modeled (lines) I_{DS} versus V_{DS} (V_{GT}=200mV) curves.

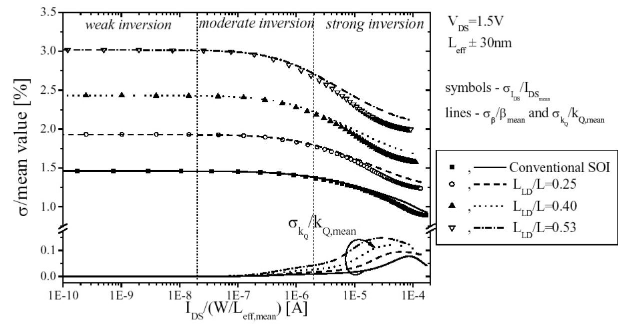

Figure 7. Standard deviation of the modeled drain current and its β and k_Q terms as a function of the normalized drain current in saturation region (V_{DS}=1.5V).

After adjusting the parameters to the experimental curves, the drain current of all devices were obtained by varying their effective channel length in ± 30nm, which is larger than the 1.15% found in the previous section, in order to analyze the deviation of the terms of equation (7). It has been verified that the mobility variation is not the dominant parameter in β deviation and therefore it was kept constant in all this analysis, as well as the threshold voltage and subthreshold slope. The results obtained in linear region are presented in Figure 6.

As the threshold voltage variation has been neglected, one can observe that there is no drain current deviation increase as devices approach weak inversion, as observed in the experimental curves. From the analysis of these curves, one can also note that the main contribution to the mismatch in the drain current in linear region is the β variation and not k_Q variation (equation 7). In addition, it is possible to see that $\sigma_{I_{DS}} / I_{DS,mean}$ coincides with the imposed percentage of variation in L_{eff}. Since the effective channel length decreases with L_{LD}/L, it becomes clear that for a fixed effective channel length variation, the mismatch will be larger in GC SOI devices than in the conventional one with the same mask channel length.

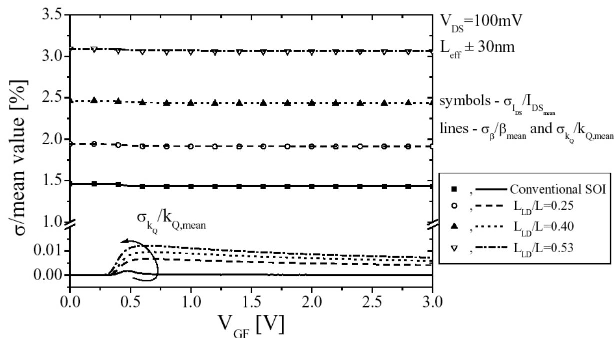

Figure 6. Standard deviation of the modeled drain current and its β and k_Q terms as a function of the gate voltage in linear region (V_{DS}=100mV).

The same analysis has been performed in the saturation region (V_{DS}=1.5V) and the resulting $\sigma_{I_{DS}} / I_{DS,mean}$ curves are presented in Figure 7 as a function of the normalized drain current.

The analysis of this figure allows for noting that the mismatch in the saturation region remains constant and close to the mismatch in linear region in weak and moderate inversion, while, in strong inversion, it tends to decrease. This reduction of $\sigma_{I_{DS}}/ I_{DS,mean}$ is due to $\sigma_\beta / \beta_{,mean}$ reduction, caused by the increase of the saturation voltage deviation (and hence V_{DE}) as can be seen in Figure 8. Besides compensating part of the effective channel length variation, the increase of $\sigma_{V_{DS,SAT}}/ V_{DS,SAT,mean}$ influences the term k_Q in equation (3), by means of $Q_{D,HD}$, promoting the increase of $\sigma_{k_Q} / k_{Q,mean}$, which becomes responsible for the difference between $\sigma_{I_{DS}} / I_{DS,mean}$ and $\sigma_\beta / \beta_{,mean}$ when moving from weak to strong inversion. In addition, one can observe that the saturation voltage variation tends to be larger in all GC transistors than in the conventional one, as shown in Figure 8, due to its dependence on the effective channel length in strong inversion, as shown in equation (6).

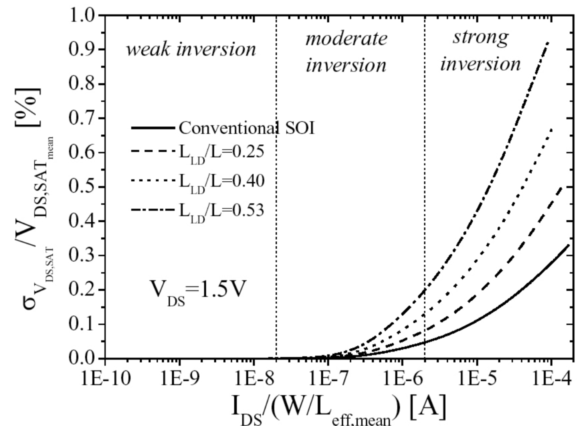

Figure 8. Standard deviation of the modeled saturation voltage as a function of the normalized drain current in saturation region (V_{DS}=1.5V).

5. ANALYSIS OF TWO-DIMENSIONAL SIMULATION RESULTS

In order to confirm the results obtained through experimental and modeled data, numerical two-dimensional simulations were performed using Atlas program [19]. By including physical models accounting for mobility dependence on velocity saturation and doping concentration, bandgap narrowing, Auger recombination, doping-dependent lifetime and impact ionization, simulations were adjusted to fit the experimental data.

All devices were simulated considering a steep transition of the doping concentration at the boundary of highly and lightly doped regions of the channel and the same devices characteristics of the measured ones (t_{oxf} = 30nm, t_{Si} = 80nm, t_{oxb} = 390nm, $N_{a,HD}$ = 6×10^{16} cm^{-3} and $N_{a,LD}$ = 10^{15} cm^{-3}).

Since the model-based analysis showed that the channel length variation dominates the current mismatch in linear region, one can assume, from the experimental results, that the average deviation in the mask channel length, verified in the conventional SOI device, is about 1.15%. Therefore, the conventional SOI was simulated with its designed dimensions and with a channel length variation of ± 23nm. The comparison between the experimental data (symbols) and simulated results (lines) is shown in Figure 9.

Afterwards, the same total channel length variation was imposed to the mask channel length of the GC SOI device with L_{LD}/L=0.30. However, it resulted in $\sigma_{I_{DS}} / I_{DS,mean}$ value close to the one obtained for the conventional SOI transistor. This indicates that there is an additional component in the variation of β, which may be related to the mismatch of the effective channel length, caused by the lateral diffusion of dopants from the highly doped into the lightly doped region and/or mask misalignment on the L_{LD} definition in the processing. Therefore, besides the total channel length variation, the position of the transition of doping concentration (from highly to lightly doped regions of the channel) was varied to fit the experimental result of the GC SOI transistor with L_{LD}/L=0.30. It has been found that this variation is about ± 10nm. The same variation was applied to the GC SOI transistor with L_{LD}/L=0.18, reaching a good agreement with experimental data, as shown in Figure 9. A conventional SOI device with L=1μm and a GC SOI device with L=2μm and L_{LD}/L=0.50 were also simulated and their resulting $\sigma_{I_{DS}} / I_{DS,mean}$ curves are also shown in this figure. It is worthwhile noting that, despite the similarity between the effective channel length of the 1μm-long conventional device and the GC one with L=2μm and L_{LD}/L=0.50, the latter presents larger mismatching, due to the additional variation of β, caused by the variation of the position of the transition between the highly and lightly doped channel regions.

Simulations were also performed in saturation, with V_{DS}=1.5V and imposing the same length variations used in the linear region. The resulting $\sigma_{I_{DS}} / I_{DS,mean}$ curves are presented in Figure 10. We clearly observe that matching improves when moving from weak to strong inversion, which is in agreement with the results obtained in the previous section. However, contrarily to the modeled results, in weak and moderate inversion, $\sigma_{I_{DS}} / I_{DS,mean}$ does not tend to the imposed channel length variation. This difference may be explained by the $\sigma_{V_T} / V_{T,mean}$ influence, which has shown to be larger at high V_{DS} due to DIBL effect, and has been neglected in the model-based analysis.

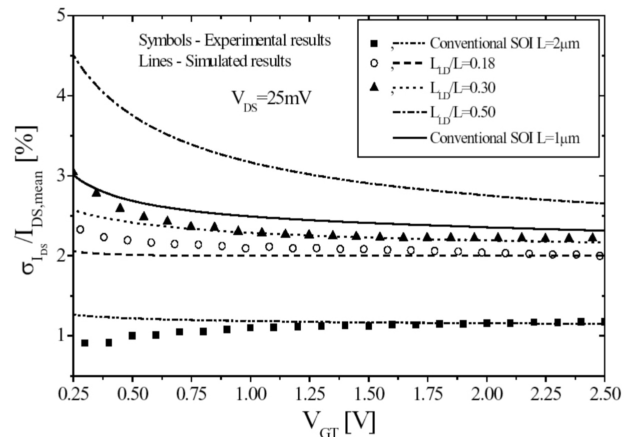

Figure 9. Comparison between measured and simulated standard deviation of the drain current as a function of the gate voltage overdrive in linear region (V_{DS}=25mV).

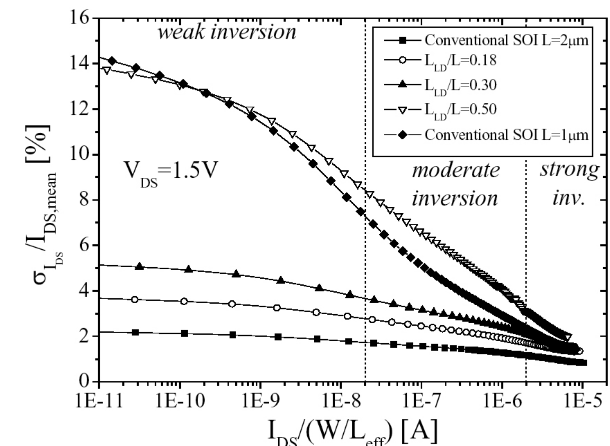

Figure 10. Simulated drain current standard deviation as a function of the normalized drain current in saturation region (V_{DS}=1.5V).

6. CONCLUSIONS

An overall evaluation of the mismatch behavior of graded-channel SOI transistors has been presented in this paper. Experimental results showed that, besides the reduction of the average threshold voltage as the relation L_{LD}/L increases, its standard variation is larger in GC SOI devices, both due to the effective channel reduction. In addition, it has been shown that the threshold voltage standard deviation is proportional to the inverse square root of the product of transistor width and effective length. Besides, the measured current variation has shown to be worsened by the presence of an undoped region in the channel.

Analytical model results were used to investigate the physical components responsible for the increased mismatch in GC transistors. From the modeled results, it was shown that, in linear region and neglecting the threshold voltage variation, the drain current mismatch is dominated by the current factor variation. However, in saturation, it tends to decrease as devices approach strong inversion regime, due to the increase of the saturation voltage variation, which attenuates the current factor deviation.

Two-dimensional simulations were adjusted to the measured data, showing that, besides the mask channel length variation that may occur during the device processing, GC devices present an additional component in the variation of current factor, which is likely to be related to the lateral diffusion of dopants from the highly doped to the lightly doped region. The adjustment of simulations to the experimental data indicates that this variation is in the order of ± 10nm only. This variation also changes the effective channel length, worsening its deviation with respect to conventional SOI with similar mask channel length.

ACKNOWLEDGEMENTS

The authors would like to acknowledge FAPESP and CNPq for the financial support.

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