Parameters Extraction from C-V Curves in Triple-Gate FinFET

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ABSTRACT

Methods to determine the effective oxide thickness (EOT), fin height (H_{fin}) and fin doping concentration (N_{fin}) through gate to drain/source capacitance as a function of the front and the back gate voltage curves in triple-gate nMOS FinFET are presented. The proposed methods were validated through three-dimensional numerical simulations and experimental measurements showing that these methods can be also applied in triple-gate nMOS FinFET devices as a powerful tool for experimental validation.

Index Terms: FinFET; CV curve; Electrical Characterization; Effective Oxide Thickness; Fin Height.

1. INTRODUCTION

Miniaturization of MOSFET devices to nanometric dimensions reduced the oxide thickness. This reduction allows a significant tunneling current (1) flowing through the oxide layer. Materials with high dielectric constant (high-*k*) have been studied to reduce the tunneling current densities and it was proposed the use of gate stacks with a high-*k* dielectric on top of the SiO_2 layer (2). The poly depletion effect can be avoided changing the polysilicon by TiN gate material (3, 4). Alternative MOS device architectures have been explored recently. Non-planar multiple gate SOI transistor, as triple-gate FinFETs appears to be one of the most promising structures. The reason is their high immunity to short channel effects and their excellent compatibility with planar CMOS process (5).

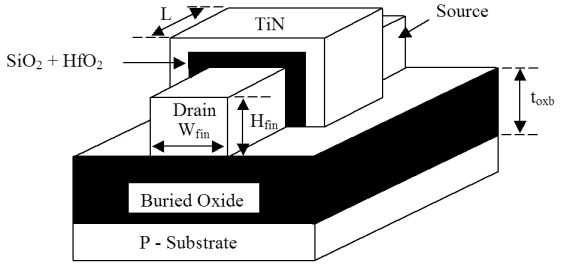

Figure 1. Schematic representation of a FinFET indicating the main geometrical dimensions.

Triple-gate nMOS FinFET structure is presented in Figure 1. TiN is the metal gate, SiO_2 + HfO_2 is the oxide gate stack and the dimensions are EOT as the Effective Oxide Thickness, H_{fin} as the fin height, t_{oxb} as the buried oxide thickness, W_{fin} as the fin width and L as the transistor channel length.

Figure 2a shows the front gate to drain/ source capacitances (C_{GDS}) and Figure 2b represents the two

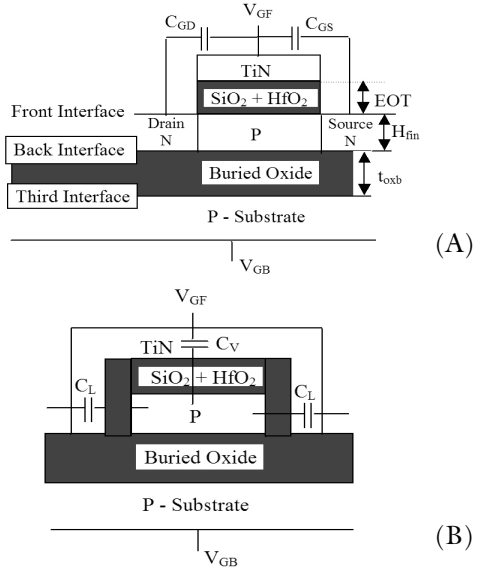

Figure 2. Crosses-section of a Triple-gate nMOS FinFET representing: a) the front Gate to Drain/Source Capacitances (C_{GDS}) and b) the lateral (C_L) and vertical (C_V) Capacitances.

lateral capacitances (C_L) that should be considered in triple-gate structures (8). If the W_{fin} is large enough, the triple-gate transistors tend to present a similar behavior to that of the single gate structures allowing the neglecting of lateral capacitances.

In this paper we present the application of single gate SOI MOSFET methods (6) in triple-gate nMOS FinFETs in order to determine the effective oxide thickness (EOT), fin height (H_{fin}) and fin doping concentration (N_{fin}). The methods are applied in capacitance-voltage curves (C-V) that are one of the most commonly used techniques for extracting the MOSFET device parameters (7). Three-dimensional numerical simulations and experimental results are used to validate the methods, achieving a good agreement.

2. CV PARAMETER EXTRACTION METHODS

A. Determination of the Effective Oxide Thickness (EOT) and Fin Height (H_{fin})

Figure 3 shows the high frequency C_{GDS} as a function of V_{GF} curves for different values of V_{GB}. It can be seen that the C_{GDS} is dependent on V_{GB}, which is affected due to the interaction between front and back interfaces (10).

When V_{GF} is positive enough, the front interface is inverted and the capacitance C_{GDS} tends to the front gate oxide capacitance defined as C1. If the front interface is depleted or accumulated (V_{GF} < 0.25V), the capacitance C_{GDS} depends on the values of V_{GB} due to the coupling between the front and back interfaces depletion. Increasing V_{GB} to high positive values, the back interface is in inversion and the capacitance C_{GDS} tends to be the series association of the front gate oxide and the fin ($C_{fin} \cong \varepsilon_{Si}.W_{fin}.L\ /H_{fin}$) capacitances, defined as C2. On the other hand, for small value of V_{GB}, there is no inversion layer in the back interface; therefore, C_{GDS} drops to practically zero, defined as C3 (parasitic capacitance).

EOT is obtained by equation 1 using C1 and C3 and considering the lateral capacitance (C_L) negligible (large width). It is necessary to subtract the parasitic capacitance (C3) of the C1.

$$EOT = \frac{\varepsilon_{0X}}{C1 - C3} W_{fin} L \quad (1)$$

Assuming that C2 is the series association of C_{oxf} (C1) and C_{fin} capacitance, it is possible to isolate C_{fin} and calculate H_{fin} by equation 2. In this case, the parasitic capacitance should be subtracted from C1 and C2.

$$H_{fin} = \frac{(C1 - C3) - (C2 - C3)}{(C1 - C3)(C2 - C3)} W_{fin} L \quad (2)$$

B. Determination of the Fin Doping Concentration (N_{fin})

The fin doping concentration (N_{fin}) can be determined interactively through equation 3 with similar approach used by Nicollian and Brews (7). In this equation ϕ_{MS1} is the metal gate-semiconductor work function difference, $V_{FB1,inv2}$ is the flat band voltage with the back interface inverted, kT/q is the thermal voltage, n_i is the intrinsic concentration of carriers, q is the electron charge and C_{oxf} is the front gate capacitance per unit area ($C_{oxf}=\varepsilon_{ox}/EOT$). EOT is previously calculated by equation 1 and H_{fin} by equation 2.

$$N_{fin} = \left(-\Phi_{MS1} + \frac{Q_{ox1}}{C_{oxf}} + 2\frac{kT}{q} \ln \frac{N_{fin}}{n_i} \left(\frac{C_{fin}}{C_{oxf} W_{fin} L} \right) + V_{FB1,inv2} \right) \frac{2C_{oxf}}{q H_{fin}} \quad (3)$$

Through the curve of the second derivative of C_{GDS} in respect to V_{GB} (Figure 4) it is possible to

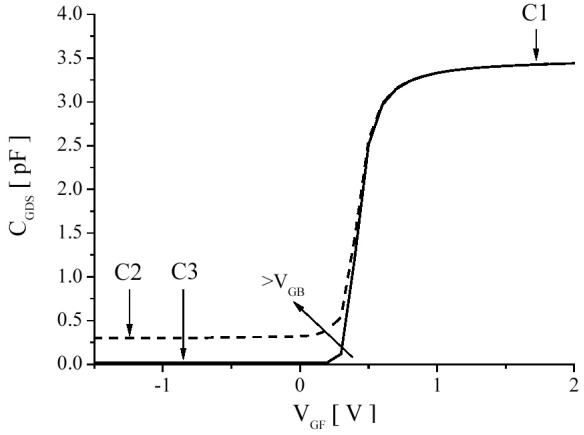

Figure 3. C_{GDS} vs. V_{GF} curves for several values of V_{GB} in triple-gate nMOS FinFET.

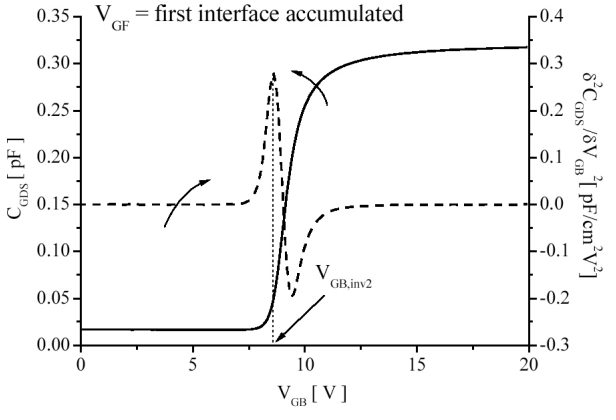

Figure 4. C_{GDS} as a function of V_{GB} and its second derivative for a V_{GF} that leaves the first interface accumulated.

obtain the back gate voltage that starts the inversion in the second interface ($V_{GB,inv2}$) by measuring the V_{GB} from the maximum peak. This curve is obtained applying a front gate voltage (V_{GF}) that leaves the first interface accumulated.

With this back gate voltage ($V_{GB,inv2}$) the C_{GDS} as a function of V_{GF} curve, presented in Figure 5, is obtained and the $V_{FB1,inv2}$ can be extracted from the first maximum peak of its second derivative curve.

C. Simulation results

ATLAS three-dimensional numerical simulations (9) were performed to verify the proposed methods. The triple-gate nMOS FinFETs structures analyzed in this paper were simulated with the following parameters: W_{fin}=20 μm, L=10 μm, TiN gate material with work function Φ_M = 4.7 eV, EOT=2 nm, t_{oxb}=145 nm, H_{fin}=60 nm, different fin doping concentration, substrate doping concentration N_{ab}=1x10^{15} cm^{-3}, LDD extension doping concentration N_D=N_S=1x10^{19} cm^{-3} and with front Q_{ox1} and back Q_{ox2} charge oxides negligible.

Simulated C_{GDS} as a function of V_{GF} curves are presented in Figure 6 for several values of V_{GB} and it can be observed the increase of the minimum capacitance for higher V_{GB} that is a result of second interface inversion.

Figure 7 shows the simulated C_{GDS} as a function of V_{GB} curve for V_{GF}=-1 V with the front interface accumulated. The capacitances C2 and C3 can be also extracted by this curve. When V_{GB} is sufficiently high, the back interface is inverted and the capacitance C_{GDS} is C2. With negative values of V_{GB}, the back interface is accumulated and the capacitance C_{GDS} is C3.

Table I show the values of C1, C2, EOT and H_{fin} obtained from the proposed method applied on simulated curves for different values of EOT and H_{fin} with N_{fin}=2x10^{17} cm^{-3} and V_{GF}=-1.0V. Results indicate that these methods have a maximum error of 2.0% on EOT and 7.4% on N_{fin} for the worst case.

Table II show $V_{FB1,inv2}$ obtained from the second derivative of C_{GDS} in respect to V_{GF} and N_{fin} determined by the proposed method for different val-

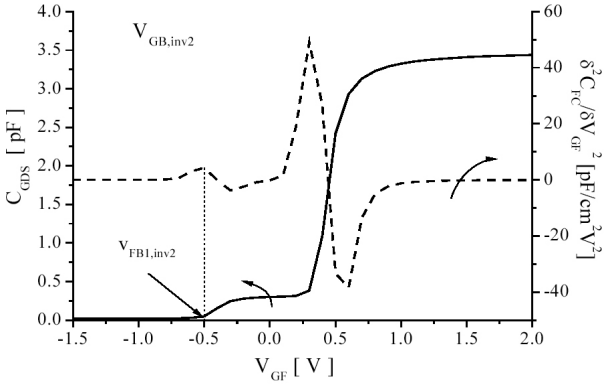

Figure 5. C_{GDS} and $\delta^2C_{GDS}/\delta V_{GF}^2$ vs. V_{GF} curves for a $V_{GB,inv2}$ that start the inversion in second interface.

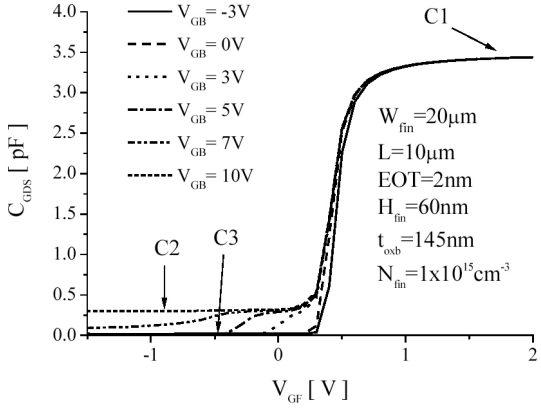

Figure 6. C_{GDS} vs. V_{GF} simulated curves for several values of V_{GB} in triple-gate nMOS FinFET.

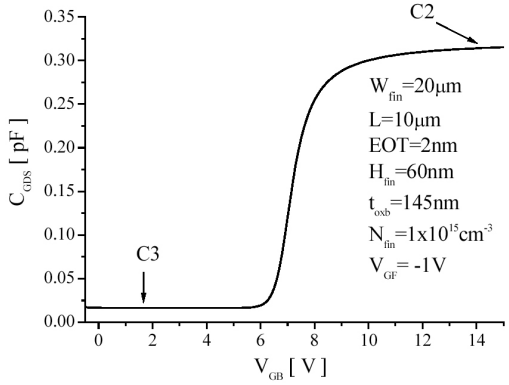

Figure 7. C_{GDS} vs. V_{GB} simulated curve with V_{GF}=-1 V (front interface accumulated) in triple-gate nMOS FinFET.

Table I. Values of EOT and H_{fin} determined by the proposed methods for different simulated values of EOT and H_{fin}.

EOT (nm) Simul	H_{fin} (nm) Simul	C1 (pF)	C2 (pF)	C3 (pF)	EOT (nm) Method	Error %	H_{fin} (nm) Method	Error %
1	60	6.78	0.35	0.014	1.02	2.0	58.57	2.4
2	60	3.41	0.31	0.018	2.02	1.0	64.81	7.4
3	60	2.26	0.32	0.013	3.05	1.7	58.24	3.0
2	50	3.38	0.37	0.019	2.04	2.0	52.90	5.8
2	70	3.40	0.28	0.018	2.03	1.5	72.91	4.2

Table II. The values of N_{fin} determined by the proposed method for different imposed values of N_{fin}.

N_{fin} (cm^{-3}) Simulated	$V_{FB1,inv2}$ (V)	N_{fin} (cm^{-3}) Method	V_{GB} (V)	Error %
1x10^{17}	-0.51	1.17x10^{17}	8.0	17.0
2x10^{17}	-0.55	2.03x10^{17}	10.6	1.5
3x10^{17}	-0.60	3.30x10^{17}	12.6	10.0

ues of N_{fin} (H_{fin}=60nm, EOT=2nm and t_{oxb}=145nm). Fin doping concentration less than N_{fin}=1x10^{17} cm^{-3} showed a higher error because the considerations used for N_{fin} determination (eq. [3]) cannot be used anymore. Another imposition of the method is that it can only be applied to fully depleted structures.

Collaert et al. reported (11) that in multiple gate SOI MOSFETs with fin doping concentration (N_{fin}) less than 2x10^{17} cm^{-3} the threshold voltage becomes independent of N_{fin} exceeding the conventional $2\phi_F$ definition of the threshold voltage. Based on this study, the methods were not applied for fin doping concentration (N_{fin}) less than 2x10^{17} cm^{-3}.

Figure 8 present the C_{GDS} vs. V_{GB} curve and its second derivative with V_{GF} = -1 V for different fin doping concentrations. When N_{fin} is increased, a higher back gate voltage (V_{GB}) is necessary to invert the back interface.

The sensitivity of the proposed methods is analyzed in Table III for H_{fin}=60nm, W_{fin}=20μm, L=10μm, EOT=2nm, t_{oxb}=145nm, N_{fin}=2x10^{17} cm^{-3}, V_{GF}= -1V with Q_{ox1}=Q_{ox2}=0. The maximum error on EOT, H_{fin} and N_{fin} determination is 5.4, 8.1 and 36.5%, respectively, which are acceptable errors for these parameters in many applications.

In order to analyze the interfaces operation mode, the potential in the middle of the channel was simulated for V_{GB}=8 V, N_{fin}=1x10^{17} cm^{-3} and different values of V_{GF}, as shown in Figure 9. It is possible to see that for values of V_{GF} lower than V_{GF} = -1.0 V, the front interface is strongly accumulated

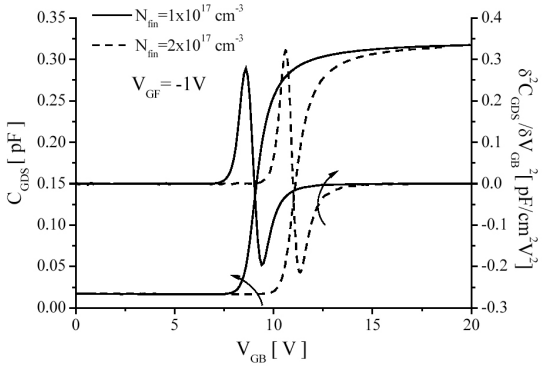

Figure 8. C_{GDS} and $\delta^2C_{GDS}/\delta V_{GB}^2$ vs. V_{GB} simulated curves with V_{GF} = -1 V for different fin doping concentration.

Table III. Maximum error on EOT, H_{fin} and N_{af} determination as a function of some electrical and process parameter.

Measurements / Parameters	EOT %	H_{fin} %	N_{fin} %
$V_{FB1,inv2}$ ± 5 %	–	–	36.5
$V_{GB,inv2}$ (0.5 V step)	–	–	36.0
EOT ± 0.2 nm	–	–	17.7
H_{fin} ± 1 nm	–	–	0.5
C1 ± 5%	5.4	<0.5	–
C2 ± 5%	–	8.1	–
C3 ± 5%	–	<0.5	–

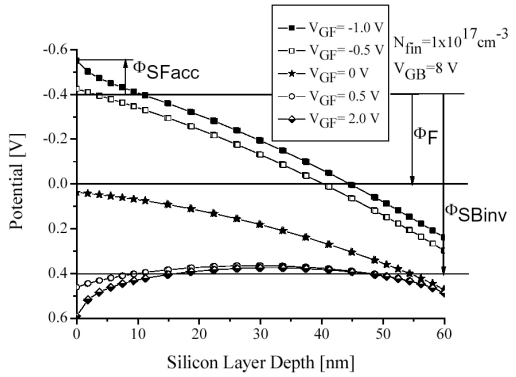

Figure 9. Potential in function of the silicon layer depth in the middle of the channel for V_{GB}= 8 V, N_{fin}=1x10^{17} cm^{-3} and different values of V_{GF}.

(front interface surface potential in accumulation Φ_{SFacc}). Simultaneously the back interface is depleted and C_{GDS} can be considered as C3. Increasing the front gate voltage (V_{GF}= -0.5 V), the front interface starts the "accumulation for depletion transition" (near $V_{FB1,inv2}$), while the back interface is near the inversion (fin/buried oxide interface surface potential in inversion Φ_{SBinv}), resulting in C_{GDS} =C2. With V_{GF}=0.5 V the front and back interfaces are inverted (the surface potential is described as two times level of Fermi ϕ_F), and no difference can be seen in C_{GDS} that is tending to C1.

D. Experimental Results

The proposed methods were verified against experimental measurements of triple-gate FinFETs. They were fabricated starting from SOI nMOSFETs undoped wafers (N_{fin}=1x10^{15} cm^{-3}) with 145 nm buried oxide thickness, following the process described in Ref. (10). The top silicon layer thickness, which is the fin height (H_{fin}), is patterned with 60 nm. After the silicon film definition, a 1 nm thick interfacial thermal oxide is grown, followed by the atomic layer deposition (ALD) of 2 nm HfO_2, resulting in a effective oxide thickness of EOT≅2.0 nm. The gate stack is completed with a 5 nm thick TiN ALD film and a 100 nm polysilicon layer. The measured devices have channel length of 10μm, width of 5, 10 and 20μm. The high frequency C-V curves were performed with HP4280 LCR Meter at 1 MHz using the HP4140 Picoamperimeter to polarize the substrate (V_{GB}).

Figure 10 present the curves of C_{GDS} as a function of V_{GF} for different values of V_{GB} in a triple-gate FinFET with channel width of W_{fin}=20μm. A level appears in C-V curves, near the depletion region, as the back gate voltage increases. The curve of C_{GDS} as a function of V_{GB} curve with V_{GF}= -0.5 V (leaving the first interface accumulated) is shown in Figure 11 were the capacitances C2 and C3 can be seen.

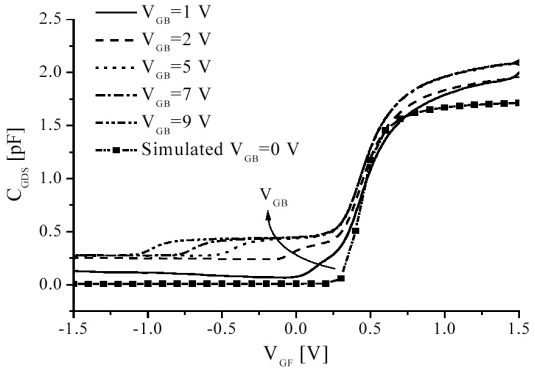

Figure 10. Experimental C_{GDS} as a function of V_{GF} curves for different values of V_{GB}.

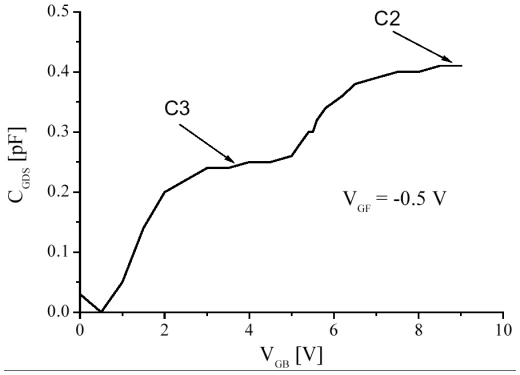

Figure 11. C_{GDS} vs. V_{GB} experimental curves with V_{GF}=-0.5V.

Table IV present the values of EOT and fin height calculated by the proposed methods, for different channel widths. The maximum error found was 1.99% for the effective oxide thickness and 1.52% for the fin height. The parameters obtained are close to the expected for this technology. Channel width less than 3μm presented capacitance values very small make difficult its measure, as a conclusion narrow W_{fin} can be a limitation for the proposed methods.

Unfortunately, the fin doping concentration (N_{fin}) could not be calculated from the experimental curves because the fin is undoped ($N_{fin} \cong 1x10^{15}$ cm^{-3}) and it is out of range for this method as exposed previously. These methods can also be easily extended to triple-gate pMOS FinFET.

Table IV. Experimental values of EOT and H_{fin} determined by the proposed method for several values of channel width (W_{fin}).

W_{fin} (μm)	C1 (pF)	C2 (pF)	C3 (pF)	EOT (nm) Method	Error %	H_{fin} (nm) Method	Error %
20	3.75	0.55	0.24	1.96	2.00	60.91	1.52
10	1.97	0.39	0.23	1.99	0.50	59.39	1.02
5	1.09	3.06	2.27	1.99	0.50	59.58	0.70

3. CONCLUSION

This work presented a technique to determine the effective oxide thickness, fin height and fin doping concentration in triple-gate nMOS FinFET devices. Three-dimensional numerical simulations were used to validate these methods, and good results were achieved. The proposed methods were applied to experimental data, providing coherent results.

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