Stress Analysis on Ultra Thin Ground Wafers

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ABSTRACT

Grinding wafers is a well established process for thinning wafers down to 100 μm for use in smart cards and stacking chips. As a result of the mechanical process, the wafer backside is compressively stressed. In this paper, authors investigate the influence of the backside induced stress in Si wafers thinned down to ~20μm by means of an IR time-of-flight like technique. Such aggressive thinning is a requirement for high density vias interconnect, stacked die packaging and flexible electronics. We found that the thinning process used did not add significant stress value on the thinned wafer.

Index Terms: Stress, Stoney's Formula, Grinding, Wafer Thinning

1. INTRODUCTION

As consumer products push technology to more powerful and more portable devices, increasingly compact integration of different subsystems is required. Interconnecting these subsystems and packaging them turns out to be a major challenge. For instance, to integrate memory, processor and RF communication, different substrates can be involved. The long interconnect length between the several blocks will introduce delay and parasitic effects that limit overall circuit performance. Also, the density of the interconnection lines scale with the perimeter of the die, while the number of circuit I/O's increases exponentially with circuit complexity according to the "Rent's rule"[1].

In order to overcome these limitations 3D integration techniques have been proposed, stacking the several integrated subsystems in a single packed device, to form e-cubes, Systems in Package (SiP) and through-Si vias [1-3]. Such stacking requires the vertical dimension of the chips to be reduced, as to reduce the total thickness of the chip stack to less than 1 mm and to allow packaging as a single device. This approach, allows to built interconnection lines through the Si die using micro fabrication techniques (as apposed to wire-bonding), connecting a top die to the underneath systems. This greatly reduces the interconnect length and increases interconnect density to values as high as 10k/mm^2. To achieve such a high density, aggressive thinning of the Si wafer must be performed to allow the construction of small and high aspect ratio (AR) vias.

However, this aggressive thinning process introduces a new problem. In order to reduce the wafer thickness, a (mechanical) grinding process must be performed. This process induces defects on the ground wafer backside and creates a compressively stressed damaged layer [4-6]. Although this layer is very thin, its induced stress can be enough to significantly bend an unsupported thin substrate (Figure 1).

In this paper authors present an analysis using Stoney's formula [7], of the average stress induced by the thinning process in a Si wafer (200 μm) mounted onto a carrier and thinned down to 20 mm residual thickness. The carrier is used to give mechanical support for the 20 μm wafer so it can be handled during and after the grinding and measurements [8]. A brief overview of the grinding process and of the history of Stoney's formula is also presented.

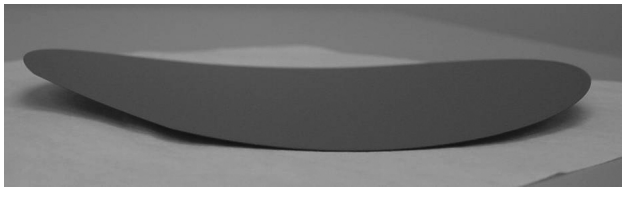

Figure 1. A 6" Si wafer thinned to 110 μm presents a bow of more than 1 cm because of the stress in the SSD caused by rough grinding.

A. Wafer thinning by grinding

Wafer grinding is a very common process in the microelectronics industry for controlling the thickness and thickness variation during wafer fabrication. After the initial slicing from the ingot, follows a series of steps to achieve the mirror like, low roughness surface required for device fabrication. One of these steps involves mechanical removal of the rough wire sawing profile and flattening of the surface, which can be done by lapping or grinding. A final polishing step (mechanical and/or chemical) follows to obtain a defect-free surface finish [5-6].

Because of the speed, the relatively low amount of damage induced and the lack of polishing slurry required for processing [8] the grinding process has also been chosen for fulfill the requirements of thin dies for smart cards and system stacking, e.g. memory for cell phones. Backside grinding after the CMOS fabrication is largely used by the microelectronics industry to achieve die thicknesses that are now moving to 50 μm [9].

A production grinder tool normally has 2 spindles/grinding wheels. These wheels are made by diamond grits embedded in a bonding matrix, which can either be metallic, vitrified or a resin. The main characteristic of a grinder wheel is its mesh, that is related to the density of diamond particles embedded and thus, with the size of these particles. The higher the mesh, the smaller the grit size, the smaller the roughness and the smaller the sub-surface damage (SSD). The bonding matrix also affects SSD, but only in secondary order [10].

A typical grinding process consists of 2 steps. The first grinding step is performed with a rough grinding wheel (small mesh) in order to remove the bulk of the Si at high speed (in the order of a few μm per second). Yet, it causes deep SSD due to the brittle nature of the Si wafer in combination with the big grit size. This damage layer is typically confined to the first 20 μm below the ground surface. A fine grinding step is then performed to remove this damaged layer and provide a mirror like surface. Although the fine grinding is used to remove the SSD from the rough grinding, it also introduces its own damage, though in a much smaller range, normally a few microns deep or even below 1 μm.

The higher/deeper the damage level, the higher the stress will be in the SSD and this is reflected on the thin wafer as well. For instance, Figure 1 shows a 110 μm thick 6" Si wafer after a rough grinding step (no fine grinding). The SSD layer is thick and stressed enough to cause the wafer to bow more than 1 cm. This introduces an undesired effect if we think on flexible electronics applications (UTCF – Ultra Thin Chip on Flex substrate) aiming for biomedical application, such as patches for corporal temperature monitoring where no stiff substrate is present. The stress concentration on such a thin chip can easily lead to early breakage of the die during handling and even impedes the fabrication of such systems. So the stress and the SSD must be reduced as much as possible aiming for off-carrier applications.

Another concern arises when grinding below 100 μm of residual thickness. In this thickness range, the Si becomes flexible (Figure 2) and a tape or another wafer (either Si or Glass) is used as carrier to provide mechanical support for the thin wafer. The device wafer can be bonded to the carrier by means of a temporary adhesive layer (wax, resin or adhesive tape) or by using electrostatic force. Several products are available for this, depending on the requirements of the thinning process and following process steps [8].

B. Characterizing stress by Stoney's Formula

Stoney's formula was first presented in 1909 [7] as a rule for the curvature on layered foils where the top layer (film) presents a different stress level from the layer underneath (substrate). The main achievement of this formula is that it allows estimating the average stress in a film onto a substrate without knowing any property of the film but its thickness. The initial assumptions done for the formula includes: (i) both the film and substrate thicknesses are small compared to the lateral dimensions; (ii) the film thickness is much less than the substrate thickness; (iii) the substrate material is homogeneous, isotropic, and linearly elastic, and the film material is isotropic; (iv) edge effects near the periphery of the substrate are inconsequential and all physical quantities are invariant under change in position parallel to the interface; (v) all stress components in the thickness direction vanish throughout the material; and (vi) the strains and rotations are infinitesimally small. [12]. In the broad range of applications that Stoney's formula is

Figure 2. a 200 mm wafer after thinning down to 50 μm becomes flexible.

used, some of these assumptions are not valid any more, particularly the thin film approximation becomes problematic. Several corrections have been proposed throughout the years in order to take this into account and some of these are summarized in Table I.

In the most common form, Stoney's formula is written as follows [7, 11-12]:

$$\sigma_{st} = \frac{1}{6}\frac{E}{(1-\nu)}\frac{t_s^2}{t_f R} = \frac{4}{6}\frac{E}{(1-\nu)}\frac{t_s^2 B}{t_f L^2} \quad (1)$$

With the following notation:
» E' = Biaxial elastic modulus; E'= E / (1 - ν)
- E = Young's modulus
- ν = Poisson's ratio
» t = Thickness
» B = Maximum bow; B = L^2 / (8R)
» L = scan length
» R = Radius (or the curved wafer)
» K = Curvature; K = 1/R
» σst = Stress (in Pa)
» s (subscript) = Substrate
» f (subscript) = Film/coating

Freund et al. [12] also presented some boundary conditions, captured in a dimensionless parameter S, in order to avoid non-linear effects from large curvatures. The S parameter takes into account the scan length used for the bow measurement besides the physical parameters, and basically states that the S parameter must be <0.3 in order to avoid non linear effects.

$$S = K_n [1 + (1 - \nu_s) K_n^2] \quad (2)$$

Where K_n = ¼ L^2K / t_s is a normalized curvature.

Other approaches have been presented for multilayered films [15] or take into account solely parameters of the covertures [14], but these are out of the scope of this paper.

TABLE I. correction factors for the Stoney's formula. δ and η stand for thickness and Biaxial Elastic Modulus ratio, respectively. ($\delta = t_f / t_s$; $\eta = E'_f / E'_s$)

Author	Correction factor (to be multiplied by σ_{st})	Ref
Freund	$[(1+\delta) / (1+ \delta\eta(4 + 6\delta + 4\delta^2) + \delta^4\eta^2]^{-1}$	[12]
Klein	$(1 - \delta + \delta^2) / (1 + \delta)^3$	[13]
Zhang (Townsend)	$(1 + \eta\delta^3) / (1 + \delta)$	[13, (14)]
Atkinson (Vilms/Kwerps)	$1 / (1 + \delta)$	[13, (14)]
Brenner/Sendoroff	$1 + 4\delta\eta - \delta$	[14]

2. EXPERIMENTAL

Two experiments were conducted on this paper. One to verify if and how much the bonding process affects the thickness measurement and one to verify how much stress the overall grinding process induces on a ultra-thinned wafer.

To assess the bonding influence on the measurements, a bare Si wafer was bonded on a carrier and thinned down to 200 µm. The thin wafer was then measured on carrier and after releasing from the carrier using the SEMDEX301 from ISIS Sentronics. This tool uses an IR light source (λ = 1300nm; 20 µm diameter spot) to make a time-of-flight measurement on the position of the interfaces of the wafer stack, in such a way that both thickness and bow can be measured simultaneously. The results of measurements on- and off-carrier are then compared.

To asses the stress induced because of the grinding process, four 200 mm Si carrier wafers were prepared with thickness of 600 µm (2 wafers) and 700 µm (2 wafers). The carriers were prepared in such a way as to reduce thickness variation and stress. 200 mm diameter, 725 µm thick (100) blanket Si wafers, from now on referred to as device wafers, were bonded onto the carriers using a wax glue layer before the grinding process. The grinding was performed in a two step procedure: first a rough grinding (#325) removes the bulk of the device wafer thickness (685 µm removed); then a fine grinding step using a Poligrind® wheel from DISCO Corp. removes 20 µm of the remaining Si. The final thickness of the device wafer after the grinding is 20 µm. Internal gauges from the grinding tool control the amount of Si removal during process.

For the bow measurements, a 40 mm scan (0.5 mm step) was performed on the 20 µm device wafers while on the carrier using the SEMDEX301. The scan length was determined from the S parameter and the dimensions involved for this experiment.

Figure 4 shows the wafer map difference between the results of a thin wafer measured both on- and off-carrier. We calculated that the average thickness of the thin wafer decreases from 197.6 µm when it's still mounted on carrier to 197.0 µm when the carrier is removed and the wafer is cleaned. From these measurements, the adhesive/carrier influence on the device wafer thickness measurement implies in an offset of +0.6 µm thick on average for the wafer mounted on carrier. This value will introduce less than 3% variation on the stress values obtained by Stoney's for-

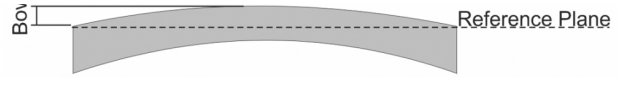

Figure 3. Bow measurement on a sample

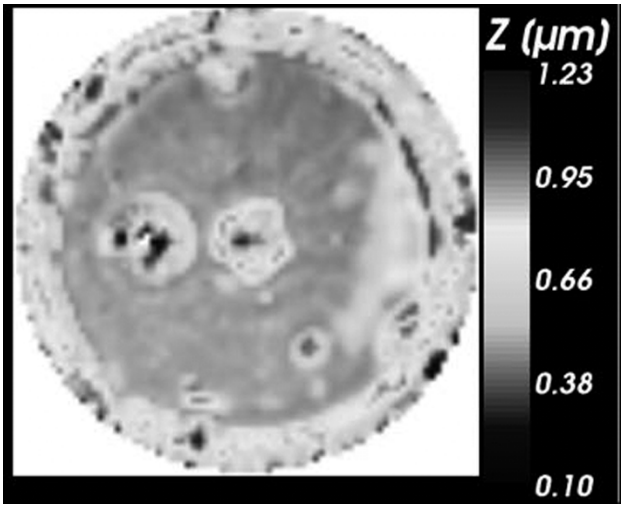

Figure 4. Difference between the measurements performed on- and off-carrier. This layer is ≅ 0.6 µm thick on average.

mula. Such a small deviation will thus not be taken into account on the following analysis.

An example of the scan measurements of the ultra thin wafer on carrier used on the second experiment (stress analysis) is presented in Figure 5 below. The measurements were performed using the SEMDEX301 and both thickness and bow values are extracted in one single scan.

Both the carrier and the device wafer have a total thickness variation (TTV) below 2 µm, so thickness variation on the samples can be discarded. In order to account for the stress induced for the overall processing on the 20 µm thin wafers, a comparison with the initial bow of the stand alone substrate must be done, so the stress on the device wafer is calculated as [16]:

$$\sigma_{st} = \frac{4}{3} \frac{E}{(1-\nu)} \frac{t_s^2}{t_f L^2} (B - B_0 \qquad (3)$$

Where B_0 is the initial bow of the carrier. The measurement results are presented on Table II and the calculated stress value is on Figure 6.

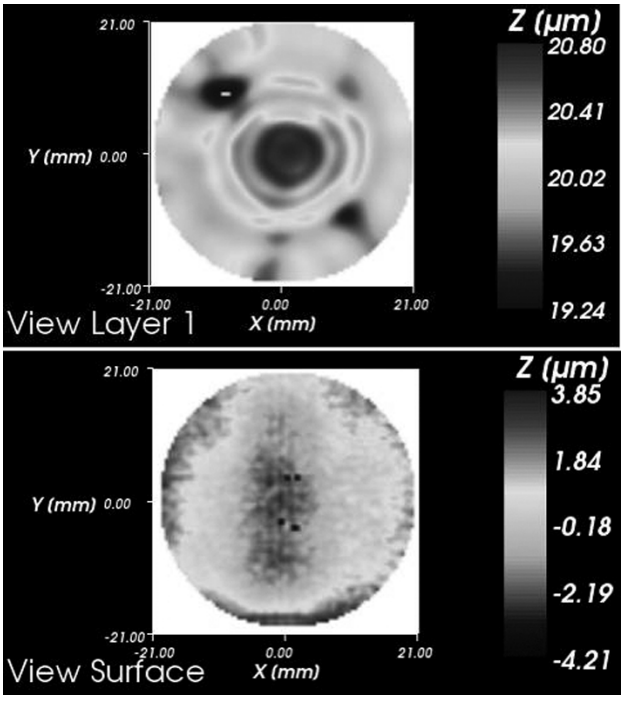

Figure 5. SEMDEX301 measurement showing thickness (top) and surface (bottom) scan view from sample #62. The bow value was extracted along the x direction on the center of the wafer (y=0).

Table II. thickness and bow measurements result. The substrate results were extracted before the device wafer bonding and thinning while the device wafer results were extracted after thinning while still on carrier. All values are in µm. Scan length = 40 mm.

Sample	Substrate (carrier)		Film (device wafer)	
	Thickness (t_s)	Bow (B_0)	Thickness (t_f)	Bow (B)
61	602.3	- 1.60	20.2	- 4.19
62	602.8	- 1.86	20.1	- 4.15
71	704.0	- 1.75	21.5	- 3.03
72	704.0	- 1.76	21.2	- 3.30

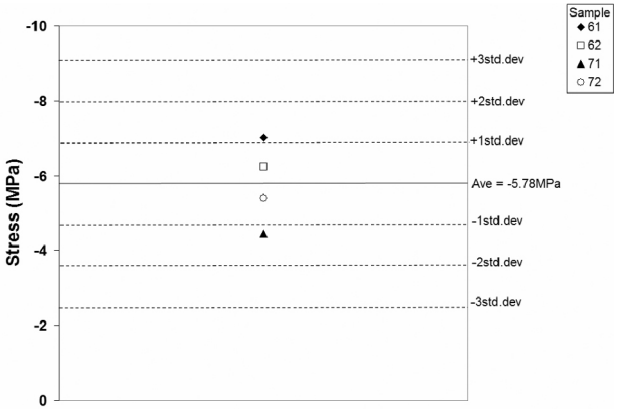

Figure 6. Stress calculated using Stoney's formula and the values from Table II.

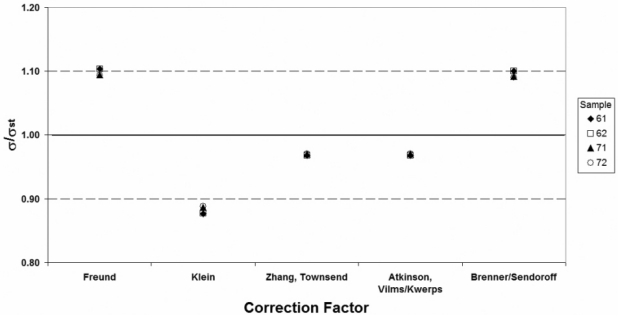

Figure 7. Correction factors calculated from equations in Table II. For the considerations of this paper, we assumed $\eta = E'_f / E'_s = 1$.

3. DISCUSSION

A. Influence of the adhesive layer on the thickness measurement

From the thickness measurements on- and off-carrier (figure 4), the wax/carrier influence on the device wafer thickness was calculated as an offset of +0.6 µm thick on average for the measurement performed on carrier. Thus, the adhesive layer is actually measured as part of the thin Si wafer, with n = 3.699 instead of its actual refractive index of 1.46. Correcting the results shown on Figure 4 to the actual adhesive refractive index, we find that the difference is a layer with average thickness of 1.42 µm. Hence, as the signal from the device wafer bottom surface and carrier wafer top surface cannot be deconvoluted by the SemDex301 because the signals are less than 70 fs apart (resolution defined by the supplier), the signals from these two reflections overlap and the measurement 'sees' a new interface positioned at half thickness of the adhesive layer which is ~ 3µm thick (Figure 8).

B. Grinding induced stress on ultra thin wafers on carrier

From Figures 6 and 7, we can clearly see that the average stress on the device wafer after thinning with the fine Poligrind® wheel is virtually non-existent, indicating that the damage caused by the grinding process is very shallow. An early indication of this can be deduced from the mirror-like surface obtained from the grinding process (Figure 9). In case of flexible electronics applications, a stress relief etch and/or polishing still follows the grinding. [14, 15].

Such small stress is an important characteristic when dealing with thin dies, because the carrier is only a temporary support used just for processing. When all processes are finished, the die must be transferred to its final destination, where the interconnections with the other circuits will be made. If the stress on the thin die is too high, this can result in failure or a change in characteristics of the devices built on the front side of the wafer. In one particular application, the thinned die has still to be transferred to a polymer covered sub-

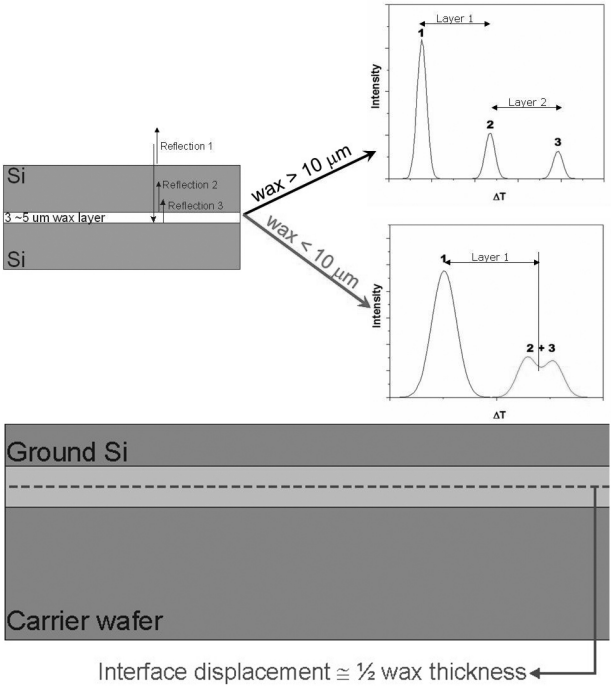

Figure 8. Since the wax layer thickness is beyond the tool resolution, the SemDex301 mixes the reflections of the close interfaces of the device and carrier wafer (top), creating a false new interface positioned at ½ adhesive layer thickness (bottom). Because of the different refractive indexes of Si and the adhesive layer, the ~1,5 µm displacement (1/2 adhesive thickness) shows up as a 0.6 µm offset on the thin Si measurements performed on carrier.

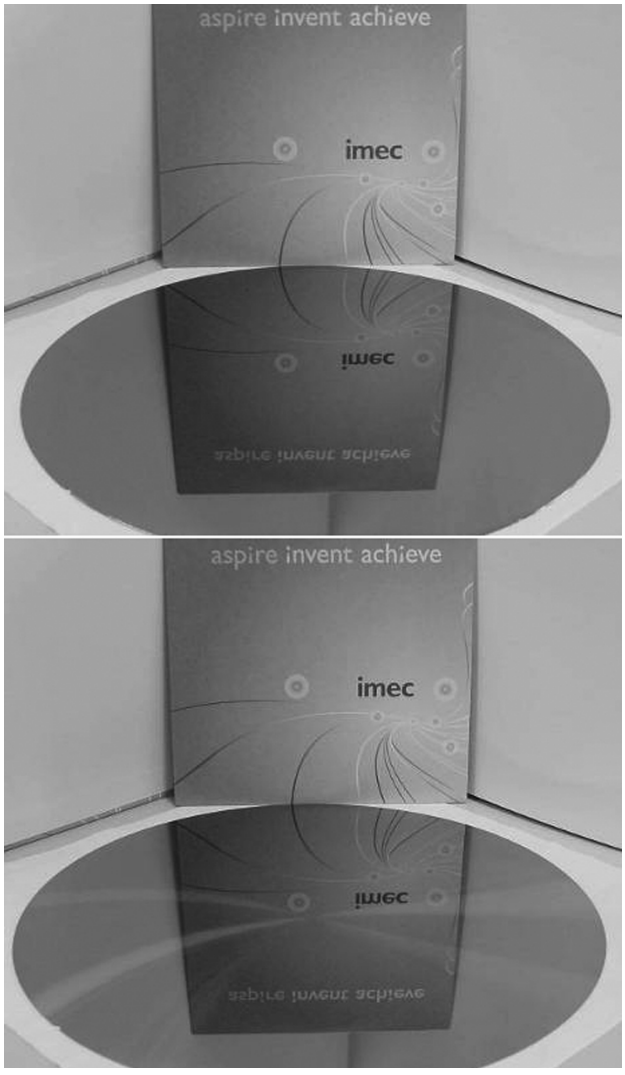

Figure 9. Surface finishing after the fine (back-)grinding process (bottom). At the top, a new polished Si wafer is presented as comparison.

strate (Figure 10) where the high density interconnections can then be microfabricated, eventually culminating in an Ultra Thin Chip Stack (UTCS) structure [19]. The temporary nature of the adhesive used for the thinning on carrier, makes it easy to transfer the thinned chip to the final location on a UTCS substrate, while keeping the low average stress level [8, 10].

However, low stress in the thinned wafer does not necessarily exclude high local stresses. Because of the mechanical nature of the grinding process, microcracks and scratches are introduced into the ground surface, creating a stacked structure like shown on Figure 11 [6]. Depending on the grit size used, a certain damage depth and defect density is created in the SSD that can reach several microns inside the wafer. The cracks/scratches make the SSD layer to be compressively stressed and the stress amount is directly related to the defect density created by the grinding process [4, 6]

So, the stress values obtained above are actually an average value of the highly stressed SSD and the low stressed bulk of the thin device wafer. All the stress is concentrated in the SSD layer located close to the surface of the wafer and the amount of defects and depth of this layer are responsible for the stress we found [4, 17-18].

Measurements are ongoing for characterizing both thickness and stress value of the SSD layer itself instead of the average stress on the thin die and how it affects an unsupported thin wafer/die.

4. CONCLUSIONS

We analyzed wafer thickness measurement results obtained by the SemDex301 tool which uses the equivalent of a time-of-flight of a NIR pulse as measurement probe. For thickness measurement of a thin wafer on carrier, the standard bonding procedure employed at IMEC creates a false interface at half thickness of the glue layer, which introduces an offset on the as-measured thickness, showing the Si wafer 0.6 µm thicker than it actually is. This happens because the bonding material is thinner than the tool resolution for the considered refractive index and the internal interfaces of the stack cannot be resolved separately. This offset will introduce a small deviation of only 3% on the stress value calculated by Stoney's formula and was discarded.

We found that the average stress induced on 20 µm thinned blanket Si wafers on carrier because of the thinning process is in the range of 1 to 10 MPa and it is compressive. Even applying several corrections for Stoney's formula presented in literature the average stress on the thinned wafer is still below 10 MPa. This proves the stresses induced by the applied thinning process are negligible and therefore the thinning process (down to 20 µm) should not affect significantly the devices built on the polished side of the thinned wafer.

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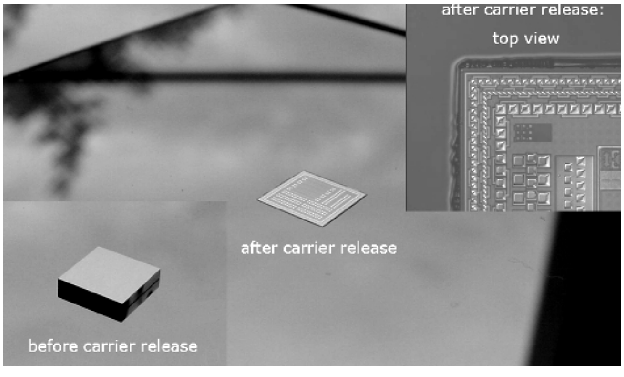
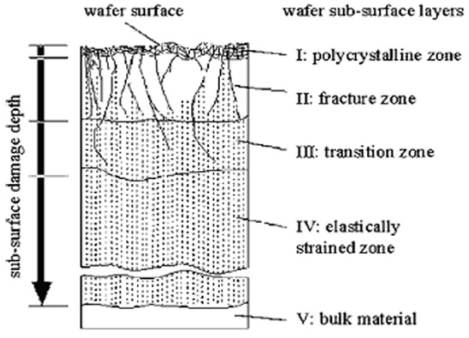


Figure 10. transfer of 20 µm thin die from the temporary carrier (inset on bottom left) to the final mounting substrate covered with a polymer layer. After the backside thinning, the die is placed faced-up for building the interconnections.



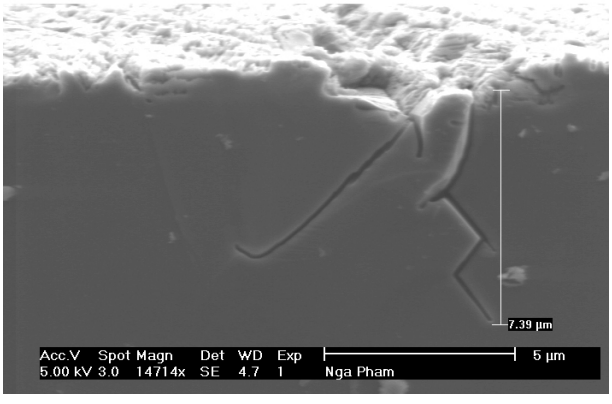


Figure 11. SSD stack [5] (top) and crack introduced because of the rough grinding (left).

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