Gate Oxide Thickness Influence on the Gate Induced Floating Body Effect in SOI Technology.

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ABSTRACT

In this work, we explore the gate oxide thickness influence on the Gate Induced Floating Body effect (GIFBE). This study was performed through two-dimensional numerical simulations and electrical measurements. The available devices are from 130nm and 65nm Silicon-On-Insulator (SOI) MOSFET technologies. The GIFBE and threshold voltage are evaluated as function of the gate oxide thickness reduction and an overlap tendency of the first and the second transconductance peaks is observed.

Index Terms: Gate Induced Floating Body Effect; Gate oxide thickness; SOI technology; Body potential and Gate current.

1. INTRODUCTION

With the technological evolution and the continuous device miniaturization, several undesirable effects have appeared for the new technologies. One of these effects is the Gate Induced Floating Body Effect (GIFBE) that can also be called the Linear Kink Effect (LKE) (1-3). The gate oxide thickness (t_{oxf}) reduction and the associated increase in the electric field applied across the gate oxide lead to an increase of the transistors' gate leakage current. This higher gate tunneling current is responsible for the appearance of the floating body effect.

When the gate oxide thickness is thinner than 5nm, the predominant tunneling current is the direct one (4, 5). The direct gate tunneling current components are: electron conduction band (ECB), electron valence band (EVB) and hole valence band (HVB), as presented in figure 1 (6). Although the ECB is more important than the others, this component has no influence on the GIFBE. The other components represent a small portion of the gate current, but they are responsible for the GIFBE appearance (3, 7).

This floating body effect occurs mainly in the SOI partially depleted (PD) devices without body contact. However, this effect can also occur in the fully depleted (FD) one, since the body bias is negative enough to accumulate the substrate. Besides these situations, there is another possibility for the GIFBE occurrence. The GIFBE still occurs in the conventional MOS transistor if the MOS is operating with a high resistance connected to the substrate.

The goal of this work is to evaluate the gate oxide thickness influence on the GIFBE in PD and FD SOI devices. The achieved results were performed through electrical measurements and two-dimensional numerical simulations.

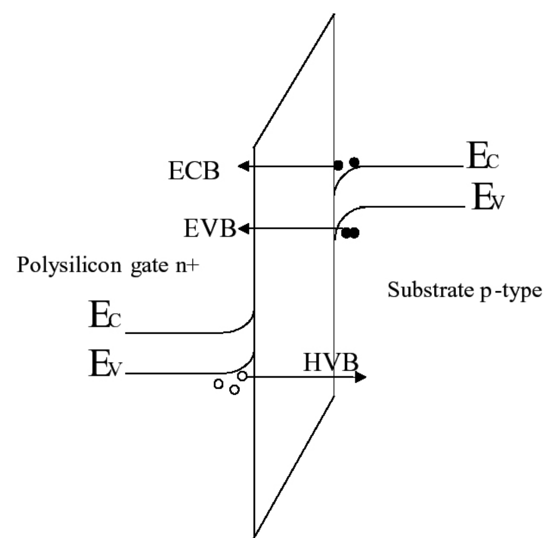

Figure 1. The energy band diagram illustrating the tunneling current components present in a SOI nMOSFET with a thin gate oxide.

2. DEVICE CHARACTERISTICS

The studied devices belong to different technologies: 130nm and 65nm SOI CMOS technology.

From the 130nm SOI CMOS technology, FD and PD SOI nMOSFETs with a gate oxide thickness of 2.5nm were studied. The silicon film and buried oxide thicknesses are 100nm and 390nm for PD SOI and 30nm and 200nm for FD ones. The body concentrations are $5.5x10^{17}cm^{-3}$ and $1x10^{18}cm^{-3}$ for PD and FD SOI, respectively.

For the 65nm technology only the FD devices are explored and their characteristics are: gate oxide, silicon film and buried oxide thicknesses of 1.5nm, 15nm and 150nm, respectively.

The measurements were performed at room temperature and the experimental curves were extracted using an Agilent 4156C semiconductor parameter analyzer.

The two dimensional numerical simulations were done using the Atlas program (8) considering the mobility dependence on the electric field and doping concentration, the gate tunneling current, Shockley-Read Hall recombination and Auger recombination models. The simulated devices have the same characteristics as the measured ones, except for the width (W). As the simulations are two dimensional, the results are extracted per W unit. In the simulations, the gate oxide thickness has been varied in a range from 1nm to 3nm.

3. ANALYSIS AND DISCUSSION

A. Simulation Results

As the devices are scaled down, the gate oxide is reduced. The gate oxide reduction causes a higher gate tunneling current and consequently it is responsible for the higher EVB and HVB components. When electrons are removed from the body neutral region and holes come to this region, resulting in a body potential increase, the threshold voltage is reduced and the GIFBE appears as the transconductance second peak. This floating body effect begins when the body potential increase in the neutral region becomes exponential.

Aiming to analyze only the gate oxide thickness influence on the GIFBE, simulations were performed keeping all the parameters constant except t_{oxf}. Figure 2A shows the normalized transconductance (g_m) as a function of gate voltage for different front gate oxide thicknesses. The transconductance was normalized by the channel length and the channel width dimensions and by the front gate oxide capacitance per area unit (C_{oxf}).

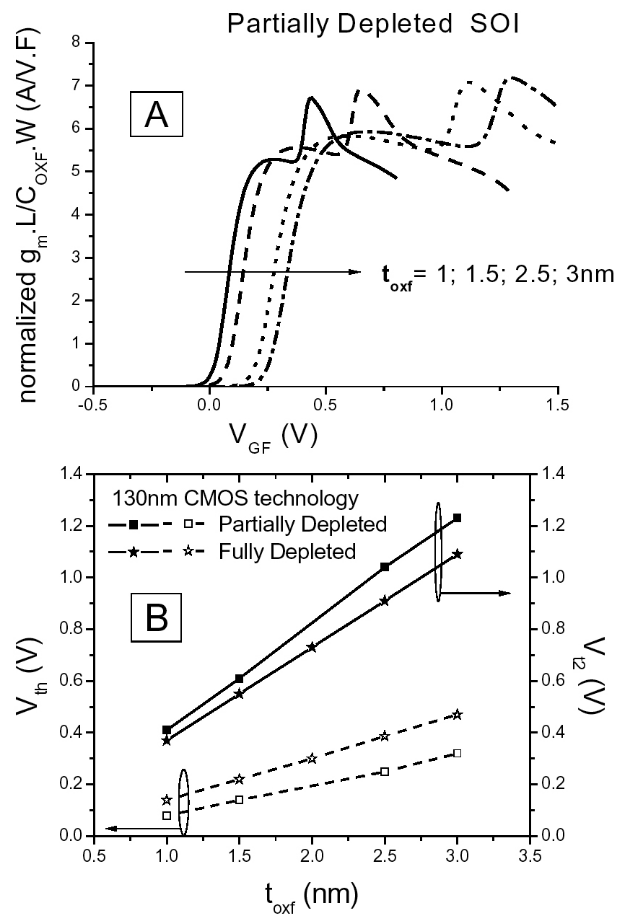

Figure 2. Normalized transconductance as a function of gate voltage for different gate oxide thickness (A) and threshold voltage (V_{th}) and GIFBE threshold (V_{t2}) variations versus the gate oxide thickness (B).

From figure 2, it is possible to note that, when the front gate oxide is reduced, both the threshold voltage reduces and the GIFBE occurs at a smaller gate voltage. Although the presented curves in Fig, 2A were obtained for PD SOI devices, the same behavior was observed for FD SOI transistors with the second interface accumulated.

The transconductance derivative was extracted for all measurements and simulations. From these curves, we obtained from the first peak, the threshold voltage value (V_{th}) and from the second peak, the GIFBE threshold (V_{t2}). Figure 2B presents the simulated threshold voltage and the GIFBE threshold as a function of the front gate oxide thickness. When the focus is the threshold voltage, the difference between the V_{th} values obtained for the PD and FD devices can be explained by the back gate bias. In order to accumulate the second interface of the FD transistors, a negative bias of -20V was applied to the substrate.

From figure 2B can be noticed that both V_{th} and V_{t2} are reduced when the t_{oxf} is scaled down, but when one compares the V_{th} and V_{t2} behaviors, it is easy to see that the GIFBE threshold reduction with

the gate oxide thickness is more pronounced than the threshold voltage reduction. From this comparison, it can be noticed that as the t_{oxf} is scaled down, the difference between the first (V_{th}) and the second peak (V_{t2}) becomes lower.

The nanometer devices usually have a HALO implantation to reduce short channel effects, although it is known that the presence of HALO causes a rise in the effective body concentration. To account for this effect new simulations with different concentrations were performed. The analyses were done considering the body concentration equal $5x10^{17}$ cm^{-3} and $1x10^{18}$ cm^{-3}. Figure 3 presents the transconductance curves as a function of the gate voltage for PD and FD SOI nMOSFETs for two different concentrations and for two different t_{oxf}, i.e., 3nm (3A) and 1.5nm (3B).

Figure 3A shows that the transconductance second peak occurs earlier for fully depleted devices than the partially depleted ones. It occurs because for fully depleted devices the second interface is already accumulated, since the GIFBE occurs through a small gate tunneling current variation. Although the GIFBE appears earlier for FD devices, the gate voltage, at which the floating body effect occurs, does not change with the body concentration. In case of PD devices it can be noticed that despite of the higher threshold voltage for the transistor with higher body concentration, the GIFBE occurs at a smaller gate voltage when compared to the transistor with body concentration equal to $5x10^{17}cm^{-3}$. Figure 3B shows the same analysis performed for devices with the smallest gate oxide thickness studied (1.5 nm) and from these curves it is possible to note the same behavior that was obtained for larger t_{oxf}. The obtained results for devices with intermediate gate oxide thicknesses also revealed the same behavior explained above as can be concluded from the data shown in table I.

The transconductance curves and the body potential behavior as a function of gate voltage for PD SOI nMOSFETs is presented in figure 4. It can be observed that the gate voltage, for which the body potential becomes exponential, is smaller for devices with a higher body concentration and thinner gate oxides causing an earlier occurrence of GIFBE. For the FD devices the curves of body potential in the neutral region also become exponential earlier with t_{oxf} reduction. However, when one compares devices with the same t_{oxf} and different body concentrations, the body potential becomes exponential for the same gate voltage. Independent on the gate oxide thickness and the body concentration, when the body potential increases by 20mV the threshold voltage reduction becomes more important than the mobility degradation associated with the vertical electric field, and consequently the onset of GIFBE.

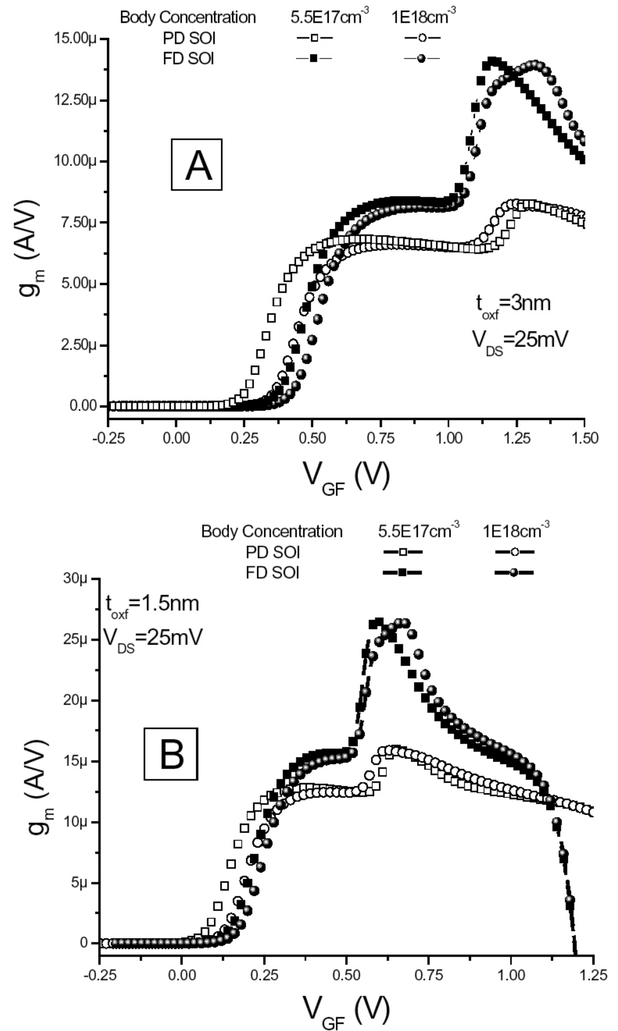

Figure 3. Transconductance versus gate voltage for different body concentrations for FD and PD SOI nMOSFETs with a front gate oxide equal to 3nm (A) and 1.5nm(B).

Table I: V_{th} and Vt_2 for different gate oxide thicknesses and different body concentrations.

t_{oxf} (nm)	Partially Depleted				Fully Depleted			
	Na= $1.10^{18}cm^{-3}$		Na= $5.5.10^{17}cm^{-3}$		Na= $1.10^{18}cm^{-3}$		Na= $5.5.10^{17}cm^{-3}$	
	V_{th} (V)	V_{t2} (V)	V_{th} (V)	V_{t2} (V)	V_{th} (V)	V_{t2} (V)	V_{th} (V)	V_{t2} (V)
1.0	0.11	0.38	0.07	0.41	0.15	0.37	0.14	0.37
1.5	0.19	0.58	0.14	0.61	0.24	0.55	0.21	0.55
2.0	0.27	0.77	0.20	0.82	0.33	0.73	0.30	0.73
2.5	0.41	0.96	0.25	1.04	0.43	0.91	0.38	0.90
3.0	0.43	1.17	0.32	1.23	0.52	1.1	0.47	1.09

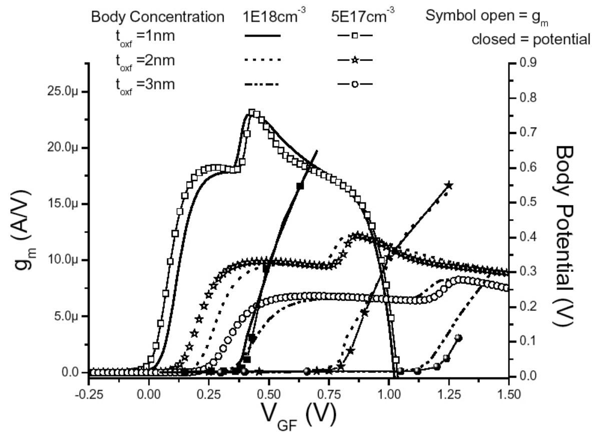

Figure 4. Transconductance behavior and body potential behavior as a function of gate voltage for different t_{oxf} and body concentrations in PD SOI nMOSFETs.

Although it is known that the threshold voltage varies with the body concentration, a constant threshold voltage was assumed in the simulations. The transconductance behavior as a function of gate voltage for devices with different t_{oxf}, different body concentrations, and a constant threshold voltage are shown in figure 5A.

In the simulations, the V_{th} was kept constant by varying the first interface surface doping concentration. From figure 5A, where the simulations are performed for partially depleted devices, it is possible to note that V_{t2} becomes still closer to V_{th} with a reduction of t_{oxf}, when keeping the threshold voltage constant. For devices with 1nm front gate oxide, it is already possible to see an overlap between the two g_m peaks.

It can be noticed that the difference between the first and the second transconductance peaks becomes smaller at the same time that the gate oxide thickness becomes thinner, independently of the body concentration of the devices. When the overlap occurs the difference is zero. For PD devices the overlap occurs for t_{oxf} equal to 1nm.

Knowing that V_{th} for FD devices is higher due to the negative back gate voltage and considering that V_{t2} occurs earlier as shown in figure 3, the difference of both parameters ($V_{t2} - V_{th}$) is still lower for FD devices and the overlapping tendency must happen even for thicker front gate oxide thickness.

B. Experimental Results

The experimental results support the simulation ones, indicating the same V_{t2} tendency as predicted by the simulations when t_{oxf} is reduced, as can be concluded from the data given in table II.

It is known that, differently from the numerical simulations, for real devices the scale down

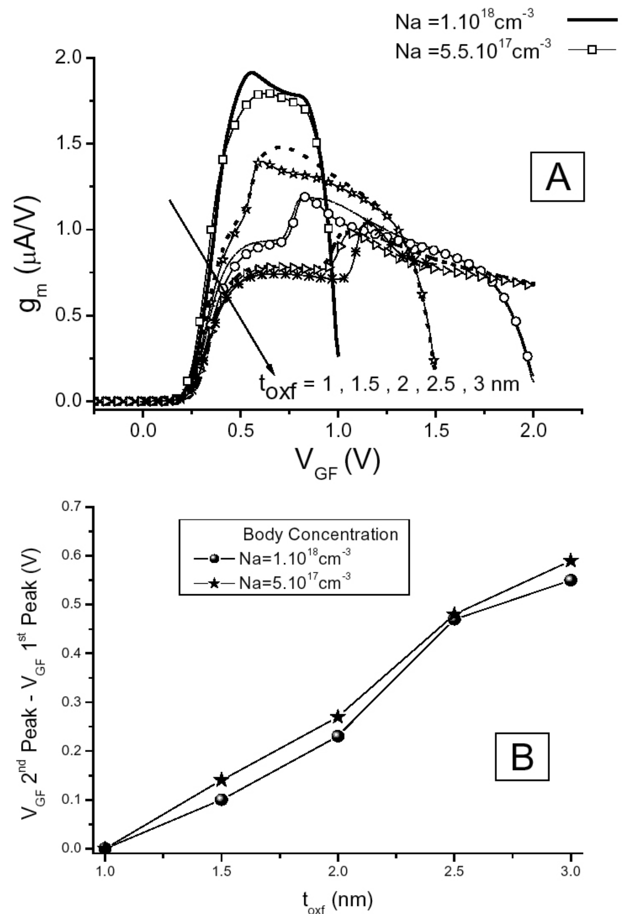

Figure 5. Transconductance versus gate voltage for PD devices with V_{th} constant and different t_{oxf} and body concentrations (A) and transconductance peaks difference as a function of the gate oxide thickness(B).

occurs in all dimensions and not only for t_{oxf}. Moreover, the doping concentration is increased with the purpose of keeping the threshold voltage at an acceptable value. As a result a greater back gate bias to accumulate the back interface is needed for the 65nm FD SOI technology, when this technology is compared to the 130nm one. A greater back gate voltage, in turn results in a higher threshold voltage.

As the t_{oxf} is reduced, the tunneling current increases and the GIFBE occurs earlier. Therefore, with the threshold voltage increasing and V_{t2} diminishing, the transconductance peaks will overlap.

Table II . Expermental V_{th} and V_{t2} data for 130nm and 65nm technologies.

	130nm technology (t_{oxf} =2.5nm)		65nm technology (t_{oxf} =1.5nm)
	PD SOI	FD SOI	FD SOI
V_{th}	0.32	0.500	0.530
V_{t2}	1.1	1.075	0.990

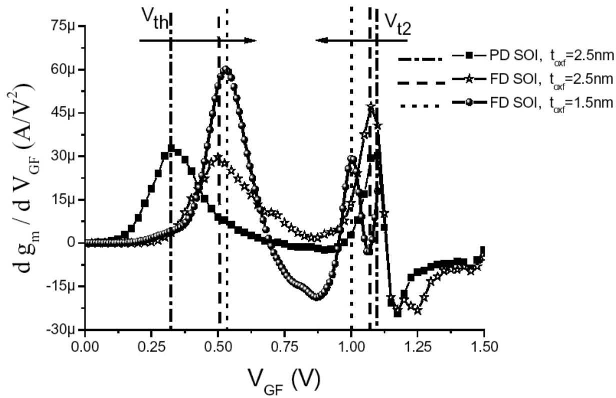

Figure 6. Experimental transconductance derivative as a function of gate voltage for 130nm (toxf=2.5nm) and 65nm (toxf=1.5nm)_ technologies.

Figure 6 presents the experimental transconductance derivative as a function of gate voltage for 130nm and 65nm technologies. The first peak of these curves represents the V_{th} and the second one, the V_{t2}. It can be noticed that, V_{th} becomes closer to V_{t2} when the device is shrunk, in agreement with the g_m peaks overlap tendency, which was suggested previously.

4. CONCLUSIONS

The gate oxide thickness influence on the Gate Induced Floating Body Effect was analyzed in this work. It has been observed that with t_{oxf} reduction, the GIFBE occurs earlier, due to the increase of the gate tunneling current. Firstly, simulations were adjusted to the experimental data from the 130nm SOI CMOS technology. Afterwards further simulations were performed varying t_{oxf} and the effective doping concentration in the body neutral region. The obtained results pointed out that the GIFBE occurs at a lower gate voltage when the gate oxide is reduced and the doping concentration increased. In addition, as the V_{th} reduction is smaller than the second peak shift, both g_m peaks tend to overlap.

GIFBE occurs because when the body potential increases by 20mV, the threshold voltage reduction becomes more important than the mobility degradation with vertical electric field.

In order to neglect the threshold voltage dependence on gate oxide thickness, simulations were also performed keeping V_{th} constant. From the analysis of these simulated results, an overlap between the two g_m peaks was observed.

With the technology scaling and the increasing use of FD devices, the threshold voltage is increasing and V_{t2} is diminishing, which confirms the g_m peaks overlap tendency. Experimental data validate the simulated tendency.

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