A 40 MHz 70 dB Gain Variable Gain Amplifier Design Using the g_m/I_D Design Method

Fernando Paixão Cortes and Sergio Bampi

Universidade Federal do Rio Grande do Sul (UFRGS), PGMICRO – Microelectronics Program, Porto Alegre-RS, Brazil
e-mail: fpcortes@inf.ufrgs.br

ABSTRACT

This paper addresses the design and post-fabrication measurements of a 40 MHz CMOS Variable Gain Amplifier (VGA) with a 0 to 70 dB gain control range, using the g_m/I_D design methodology. The VGA architecture is based on a differential pair stage with an automatic continuous-time offset cancellation circuitry, providing an input offset voltage tolerance up to 50 mV. The 3-stage VGA was designed and fabricated through MOSIS service in an IBM 0.18 µm CMOS process. The VGA dissipates 2.6 mA from a 1.8 V supply, with 34,840 μm^2 circuit area, excluding bond-pads.

Index Terms: Amplifier, CMOS analog design, RF front-end, Variable Gain Amplifier (VGA).

1. INTRODUCTION

Variable gain amplifiers (VGA) can be found in several applications and are used to maximize the dynamic range of these systems. They play the important role of stabilizing the amplitude of a signal of interest under various conditions, providing constant-amplitude signal in the signal path.

In wireless communications systems, the amplitude of the receiver and transmitter signals varies greatly. For this reason, like in digital cellular receivers, the system requires about 80 dB of dynamic gain variation and splits into RF and IF/baseband stages. Thus, to cover such a wide dynamic range, CMOS-based VGAs require at least 3 or 4 gain-varying stages.

This paper addresses the design of a 40MHz VGA that composes a RF front-end for a multi-band analog interface. The CMOS VGA architecture is based on a differential pair stage with an automatic continuous-time offset cancellation circuitry. The 3-stage VGA was analyzed and designed in CMOS 0.18 µm technology using the g_m/I_D design method.

This paper is organized as follows. Section 2 briefly discusses the RF front-end as a part of the mentioned analog mixed-signal interface. Section 3 discusses the VGA architecture based on a differential pair stage with an automatic offset cancellation circuitry. Section 4 addresses the design and implementation of the 3-stage VGA using the g_m/I_D method. Section 5 describes the measurement results of the discussed VGA, and Section 6 presents our conclusions.

2. AN RF FRONT-END FOR A MULTI-BAND ANALOG INTERFACE

In [1], a general analog signal interface architecture targeted to mixed-signal SOC applications was developed and implemented. Basically this interface is composed by a fixed analog cell (FAC), which translates the input signal to a processing frequency, and a digital block, that processes the acquired signal. The complete system (Figure 1) is described as follows: the input signal enters the variable gain front-end stage, which translates this signal to the processing frequency, providing gain control to adjust its dynamic range; the selected signal is sampled by the continuous-time bandpass sigma-delta ($\Sigma\Delta$) modulator and then processed by the digital block; the frequency synthesizer block generates the local oscillator (LO) signal that enters the front-end stage.

The front-end stage is critical to this system performance. The primary purpose of this stage is simply to convert an input signal to a processing frequency, where the input signal and bandwidth are allowed to vary from DC to high frequencies. In our design we more specific aimed the FM [2], TV tuners [3] and digital cellular [4] frequency bands. The main system

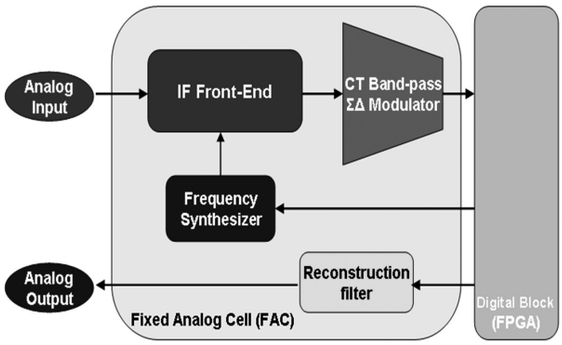

Figure 1. The multi-band analog interface.

design issues, where the final system specifications were derived and verified through system level simulations, are discussed in [5].

As a result, a dual-conversion heterodyne architecture was chosen for the front-end stage. The complete architecture (Figure 2) is described as follows. The input signal enters an up-conversion mixer, which translates this signal to a first processing intermediate frequency of 1.4 GHz (fp1), outside the input frequency band. A simple on-chip LC tank is then applied to the signal, providing initial suppression of harmonic mixing and image components. A down-conversion mixer translates the signal to a second processing frequency (fp2) of 40 MHz, and a variable gain amplifier (VGA) provides gain adjustment. The selected signal is then ready to be sampled by the ΣΔ modulator stage in the FAC, and then processed by the digital block of full mixed-signal interface, where final channel selection and image cancellation can be made.

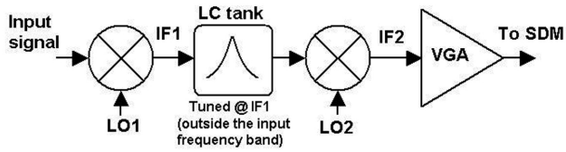

Figure 2. Dual-conversion heterodyne front-end.

3. CIRCUIT DESCRIPTION

Figure 3 shows the VGA basic cell architecture, an operational transconductance amplifier (OTA), based on [4] [6]. It comprises a NMOS input differential pair (M1-M2) with four cross-coupled transistors in cascade to control the gain (M3-M4-M5-M6), two PMOS transistors as active loads (M7-M8), and a common mode feedback circuitry (M9-M10). Vc and Vr are used to control the gain. When the cross is turned off, Vr = 0.6 V and Vc = 0.1 V, the gain is maximum. When Vr = Vc = 0.6 V, the cross coupling is maximum and the gain is about 0 dB.

In order to prevent the VGA from being saturated due to its high gain and high input offset voltage, an offset cancellation circuitry is employed. It consists of a negative feedback with a lowpass filter. M16 and M17 are working in their linear region as two resistors. These resistors together with the two capacitors form the lowpass filters that block the input signal in the feedback path in order to guarantee that the gain is not affected. M14 and M15 are used to convert the voltage feedback signal to current, which is added to the input signal.

Compared to other recent CMOS VGAs implementations, in which the gain variation is obtained by varying either the source degeneration transistors or the bias current, this simple topology consumes less power and area, using a continuous-time automatic offset cancellation technique.

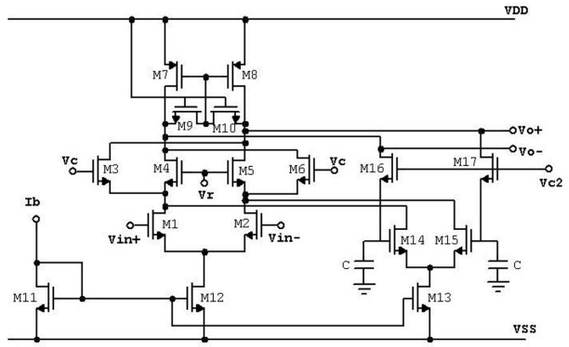

Figure 3. VGA basic cell with offset cancellation based on [6].

4. VGA DESIGN AND IMPLEMENTATION

The complete VGA is realized by cascading three identical stages of the basic cell of Figure 3. The maximum gains at 40 MHz for each cell and for the whole VGA are specified to be 23 dB and 70 dB, respectively. The VGA was analyzed and designed in IBM 0.18 μm CMOS process using the g_m/I_D design method.

A. The g_m/I_D design method

The design methodology based on g_m/I_D characteristic, proposed by [7], allows a unified synthesis methodology in all regions of operation of the MOS transistor. In this method, the relationship between the ratio of the transconductance g_m over DC drain current I_D and the normalized drain current $I_D/(W/L)$ is considered as a fundamental device design characteristics to be explored in the design space. The relationship between them represents a unique characteristic for all transistors of the same type (NMOS and PMOS) in a given technology. Once the value of the g_m/I_D ratio is chosen to fit operation region of the device, the W/L of the transistor can be determined in the curve.

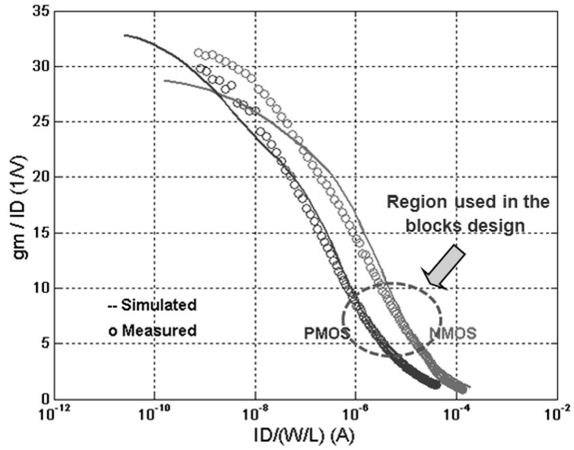

Figure 4. Simulated (BSIM3v3 model) and measured g_m/I_D curves for NMOS and PMOS transistors for IBM 0.18 µm CMOS process.

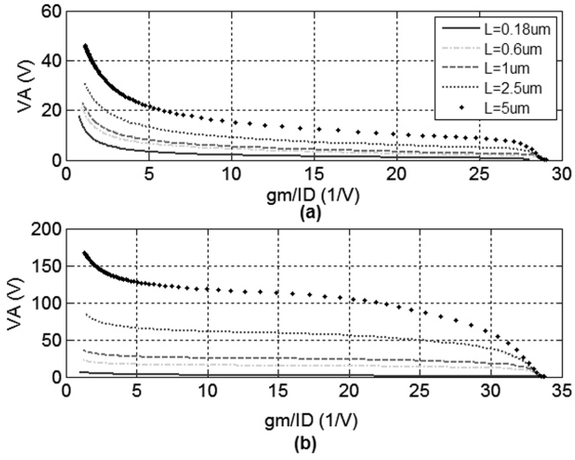

Figure 5. Simulated (BSIM3v3 model) and measured g_m/I_D curves for NMOS and PMOS transistors for IBM 0.18 µm CMOS process.

Figure 4 shows the g_m/I_D vs. $I_D/(W/L)$ simulated and measured curves (NMOS and PMOS) for the IBM 0.18 µm CMOS process. The test structures in our chip test were used to collect device characteristics and parameters. Figure 5 shows the other parameter which is important in our design methodogy, specifically the Early voltage dependence on the g_m/I_D for several transistor sizes (varying transistor lenghts, NMOS in curve *a)*, PMOS in curve *b)*, for the same technology). The data in Fig. 5 was obtained by simulations using the BSIM3v3 model provided by the foundry. One can see that the Early voltage (VA) decreases as the transistor leaves strong inversion and enters moderate inversion levels. The gain behavior of the VGA is impacted by the choice of the transistor length. The transistor lengths in Table 1 were chosen by the Early voltage sought for each transistor.

B. The g_m/I_D design method

The g_m/I_D design method was applied to the synthesis of the VGA cell. The complete design procedure is demonstrated as follows:

- Considering signal level and power specifications, the bias current in each stage was set to 500 µA;
- The g_m/I_D ratio of the input differential pair and the cross-coupled transistors were set to 8 and 4, respectively, in order to achieve the maximum gain requirement of 24 dB at 40 MHz;
- The current mirror and the load transistors should operate in strong inversion to guarantee good matching and noise properties. Thus, g_m/I_D ratio was set to 8;
- For the CMFB circuitry, in order to guarantee stable bias conditions, the transistors must operate in the linear region (strong inversion - g_m/I_D ratio of 3);
- In order to obtain a tradeoff among power, area, noise and output offset, the g_m/I_D ratio of the negative feedback transistors was set to be the same as the input differential pair, where the DC gain is about 0 dB. The lowpass filter cutoff frequency was set to be around 40 MHz;
- The transistor lengths L are determined by a tradeoff between area and DC gain requirement (due to the dependence of the Early voltage on the transistor length).

In our design, the simulated g_m/I_D curves were considered, since the experimental data was not yet collected by our team from fabricated chips. The designed values for the transistors sizes and circuit components are shown in Table 1. Note that minimum L were not used due to the Early voltage requirements, as seen in Fig. 5.

Table I. VGA basic cell component summary.

Component Name	Value	g_m/I_D
M1, M2 (W/L)	12*(2µm/0.6µm)	8
M3, M4, M5, M6 (W/L)	8*(5µm /1µm)	4
M7, M8 (W/L)	32*(12µm /1µm)	8
M9, M10 (W/L)	(0.22µm /8µm)	-
M11, M12, M13 (W/L)	10*(27µm /1µm)	8
M14, M15 (W/L)	12*(2µm /0.6µm)	3
M16, M17 (W/L)	(1.5µm /2µm)	3
C	500fF (MIM HK cap 16 x 15.5 µm2)	-

C. 3-Stage VGA implementation

The 40MHz variable gain amplifier (VGA) comprises three operational transconductance amplifiers (OTA) in cascade, so that more than 70 dB of gain variation can be achieved. Figure 6 shows the block diagram of the overall 3-stage VGA, where a buffer stage is added for the convenience of measurements. Thus, the buffer is designed as a differential

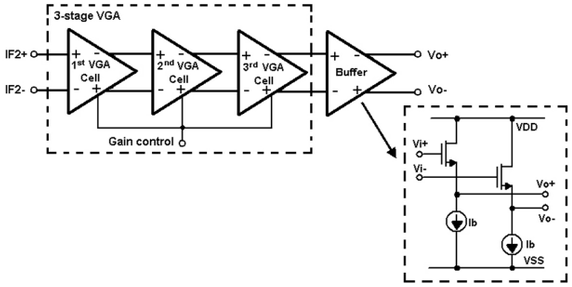

Figure 6. Complete block diagram of the 3-stage VGA.

source-follower considering a 5 pF load (in order to drive instrumentation with 50 Ω inputs).

The circuit layout design was completed using Cadence Virtuoso Design Editor Environment in IBM 0.18 µm CMOS process with 6 metal layers. Each OTA cell was laid out in cascade, resulting in the 3-stage VGA final layout showed in Figure 7.

The input differential pairs and current mirrors were implemented using a common-centroid configuration. The capacitors were implemented as a single HiK-dielectric MIM (metal-insulator-metal) capacitors (C = 500 fF), considering the available component library of the IBM 0.18 µm process design kit. In the buffer stage, a triple well source follower buffer transistor was used, allowing the transistor bulk to be tied to the source.The architecture is fully differential and layout as symmetrically as possible to minimize the mismatch in the signal paths. The total area of the implemented circuit is 34,840 μm^2.

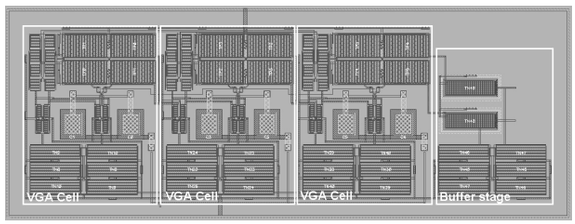

Figure 7. 3-Stage VGA final layout.

5. MEASUREMENT RESULTS

The 3-stage VGA, together with several analog/RF blocks and some test structures, was fabricated in a test chip in IBM 0.18 µm CMOS process through MPW MOSIS of ISI-USC in the USA. The chip was packaged in a 64-pin QFN package, with a total area (including pads) of 6.8 mm^2. The die micrograph is shown in Figure 8. The die includes other modules and test structures not discussed in this paper, like 3 different RF mixers, VCOs, test structures for transistor arrangements, as well as ring oscillators. The performance measurement results are shown together with post-layout electrical simulations in this section for comparisons. The test setup of the 3-stage VGA is illustrated in Figure 9.

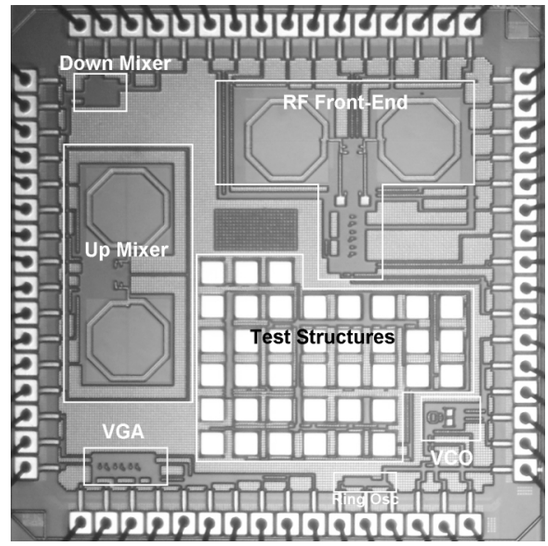

Figure 8. System chip die micrograph.

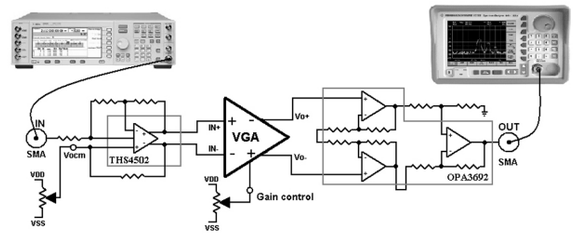

Figure 9. VGA test setup.

The measured frequency response of the VGA is shown in Figure 10. The gain at 40 MHz is 70 dB, and the maximum gain is about 72 dB at 38 MHz. The input signal generator was set to -80 dBm in order to avoid saturation.

Measurement of the gain control range of the VGA at 40MHz is shown in Figure 11. As the control voltage decreases, the gain of the VGA increases. The maximum measured gain is about 70 dB. The gain varies

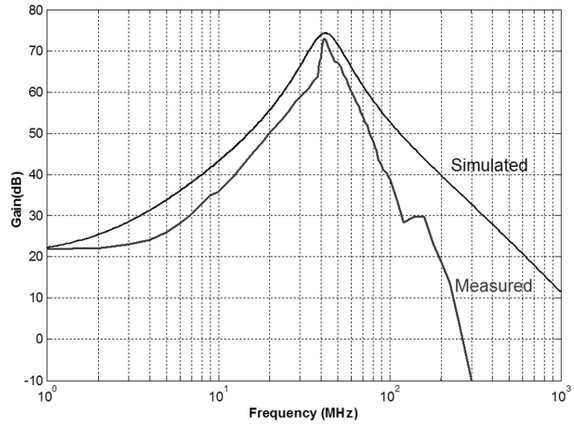

Figure 10. Measured and simulated frequency response of the VGA.

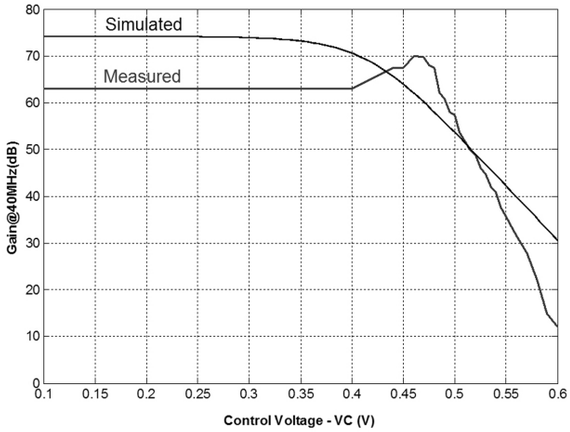

Figure 11. Measured and simulated gain control range of the VGA.

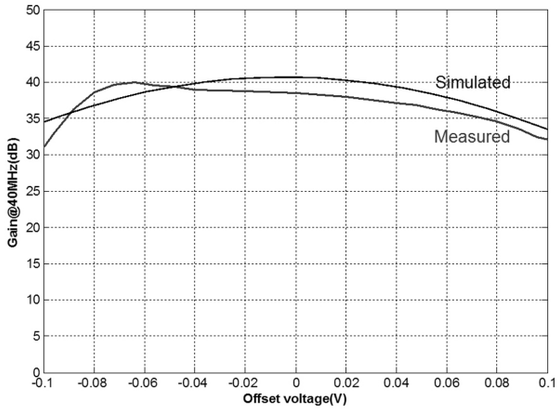

Figure 12. Measured and simulated gain variation due to the input offset voltage of the VGA at 40MHz.

Table II. VGA measured performance summary.

	Post-layout Simulation IB=1.5mA, CL=5pF	**Measurement IB=1.5mA, PCB load**
Gain control range (dB)	0 - 75	0 - 72
Offset cancellation (mV)	60	50
NF (dB)	26	-
OIP3 (dBm)	6.7	-
Output Swing (mVpp) (@35dB gain)	600 (0dBm)	600 (0dBm)
Total power cons. (mW) (including buffer)	18.6	15.21

continuously from 0 to 70 dB, corresponding to a control voltage (Vc) from 0.4 V to 0.7 V. Further decrease of the control voltage completely turns off the cross-coupling transistors, and the gain becomes constant.

Figure 12 shows the VGA gain as a function of the input offset voltage, with a 35 dB gain. With offset cancellation, the circuit is quite insensitive to the input offset voltage. The maximum tolerable offset voltage of the VGA, defined as the offset voltage in which the gain decreases by 1 dB, is measured to be 50 mV.

Table 2 summarizes the 3-stage VGA measured performance, comparing with post-layout simulations. Results show that the VGA has a continuous gain control range of 70 dB, quite insensitive to the offset voltage, consuming 2.75 mA (without buffer) from a 1.8 V supply. Due to limitations in the test equipments, linearity and noise measurements are not herein presented.

A comparison with other VGA implementations in given in Table 3. The discussed VGA design using the g_m/I_D method achieves best performance in terms of decibel linear variation, power consumption, and chip area.

Table III. Comparison of the discussed and previously reported VGAs.

Ref.	**Technology**	**Number of stages**	**Operation frequency (MHz)**	**Gain range (dB)**	**Power consumption (mW)**	**Application**
[8]	0.18µm CMOS process	2 (plus control stage)	32 - 1050	68 to 95	6.5 (1.8V supply)	CDMA receiver
[6]	0.5µm CMOS process	3	70	0 to 70	15 (2.5V supply)	GSM receiver IF-Baseband strip (VGA+ Mixer+IF Filter) for a GSM receiver
[9]	0.25µm CMOS process	3	71	10 to 90	12 (2.5V supply)	
[10]	0.18µm CMOS process	5	470 - 870	-17 to 16	22 (1.8V supply)	DTV Tuner
[11]	0.25µm CMOS process	4	30 - 210	-35 to 55	27.5 (2.5V supply)	CDMA receiver
This work	0.18µm CMOS process	3	40M	0 to 70	4.7 (1.8V supply)	RF front-end

6. CONCLUSIONS

A 40 MHz 70 dB gain 3-stage VGA design, as a part of an RF front-end suitable for a multi-band analog interface, has been presented in this paper. The VGA basic cell architecture is based on a simple OTA with an automatic continuous-time offset cancellation circuitry, providing an input offset voltage tolerance up to 50 mV and a continuous gain control range from 0 to 70 dB, proving to be suitable for the analog inteface application. The 3-stage VGA was designed using the g_m/I_D method and fabricated in IBM 0.18 µm CMOS process. The VGA dissipates 2.6 mA (without buffer) from a 1.8 V supply while occupying a 34,840 µm² of chip area.

ACKNOWLEDGEMENTS

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