Study of the Metal Filling Impact on Standard Cells and their Associated Interconnects Using Ring Oscillators: Definition of the Metal Fill Corner Concept

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ABSTRACT

The objective of this paper is to evaluate the delay impact of staggered metal filling on the standard cells and their associated local interconnect on several metal levels. A Design of Experiment (DOE) is used to define a large range of filling pattern shapes and positions. This set of filling patterns is then inserted in a Ring Oscillator (RO). From the filled RO simulations, the RO delay is expressed as a function of the filling pattern features. The maximal timing error between the model and the simulation is 1.3%, validating the model. The filling impact on RO delay magnifies the one introduced by the front-end process variations (PVT). Consequently, the filling influence is introduced for the minimal, typical and maximal corners, defined now with Process (P), Voltage (V), Temperature (T) and Filling density (F) characteristics.

Index Terms: Metal filling, Ring oscillator, Interconnect, Design of Experiment, Corner.

1. INTRODUCTION

In advanced very-large-scale integration (VLSI) circuits, the planarity of each metal layer and interlayer dielectric (ILD) is essential to avoid significant yield losses. The primary technique used to attain high levels of planarity is chemical-mechanical polishing (CMP). Several studies of CMP process impact on electrical parameters [1] and planarity [2] are available. In order to reduce the pattern-dependant variation of thickness in the CMP process, each metal layer must have a density included in a range fixed by the technology process. This can be achieved by inserting metal fills in the space between metal shapes of the same layer. However, addition of dummy fill increases the coupling and total interconnect capacitance, leading to timing performance degradation. Multiple efficient interconnect capacitance extraction using floating dummy fill methods have been proposed to quantify this impact. An efficient algorithm based on boundary element method for three-dimensional capacitance extraction is proposed by [3], while [4] studies dummy fills impact on delay, capacitance and crosstalk noise using electrical field. Results about modeling the floating condition of dummy fills using a design of experiment methodology are presented in

[5]. Moreover, dealing with the coupling capacitance due to metal filling is a complex problem, especially because several ways of filling can be found in the industry. While [6] demonstrates metal filling impact on circuit performing a full-chip RC extraction, reference [7] studies the capacitance deviation due to both dummy fills and modifications of interconnect geometry. Filling guidelines for one metal layer are exposed in [8] in order both to increase metal density and to reduce dummy fills impact. Trying to manage the balance between high metal density and small coupling capacitance is a real challenge. Filling methods are presented in [9] to both reduce interconnect capacitance and number of dummy fills. Reference [10] presents a methodology to select an optimal metal-fill patterning, taking into account ILD thickness variation and coupling capacitance. However, there are no existing results on statistical study of metal fill patterning variations impact on delay in order to allow designers to predict filling impact on the timing of their cell.

In this context, the objective of the paper is to evaluate the delay impact of staggered metal filling on the standard cells and their associated local interconnect considering several metal levels. A DOE approach is used to develop an analytic model. Its

inputs are filling characteristics and its output is the prediction of the timing deviation of the RO due to filling impact. Section 2 presents the RO test structure description, including the way metal filling generation is performed. Section 3 describes the DOE methodology used to generate the analytic model for filled RO. A statistical analysis of filling impact on interconnects for several metal levels is proposed in section 4. Section 5 presents an estimation of the filling impact versus process front-end variation while section 6 focuses on the corner definitions including filling dependencies. Finally, section 7 gives some conclusions.

2. RING OSCILLATORS OVERVIEW

To estimate the filling impact on standard cells and associated local interconnect, Ring Oscillator (RO) circuits are designed with specific area to control the filling insertion.

A first test structure called RO_C is devoted to the study of the impact of metal 2 filling on the standard cells. The RO_C architecture is based on the interconnection of 41 instances of drive strength 2 inverters with a filling insertion area, as shown in Fig.1.
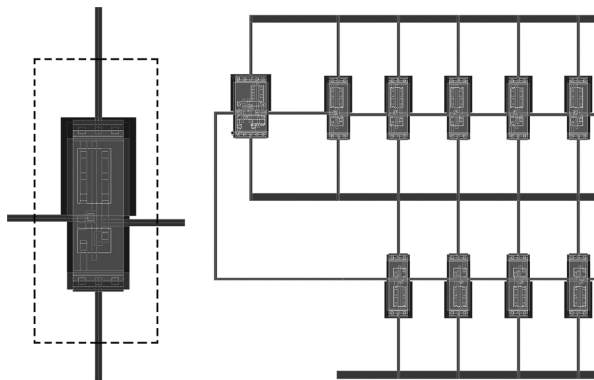

Figure 1. RO_C structure: 41 inverters connected by a small metal interconnect. The filling pattern is added in the area delimited by the dashed line. This structure is dedicated to the study of metal 2 filling impact on standard cells.

The filling insertion area is defined to guarantee that the complete set of relevant coupling capacitances between the filling pattern and the inverter are considered.

A second test structure based on RO, called RO_I, is designed to study the impact of the filling (metal level n+1) on the local interconnect (metal level n). The RO_I architecture is based on the interconnection of 61 inverters with drive strength 2. Contrary to RO_C structure, the filling insertion area is defined on the interconnect line as presented Fig.2.
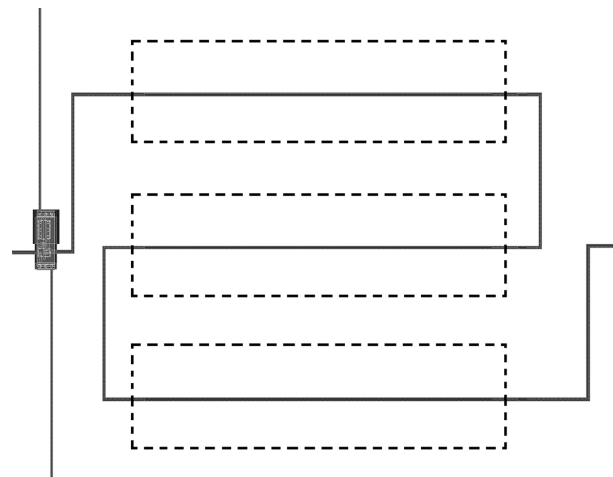

Figure 2. RO_I structure: 61 inverters connected by a long metal interconnect. The filling pattern is added in the area delimited by the dashed line. Then the structure is instantiated 3 times to create the serpentine shape. The RO_I structure is dedicated to the study of metal filling impact on standard cells interconnects.

Between two inverters, a serpentine built with 3 instances of metal interconnect with filling insertion area is designed. The filling insertion areas are defined to guarantee that the capacitances between each metal line of the serpentine have no influence.

The technology used to design both RO is a 130 nm with Cu FSG back-end. The RO simulations are performed on post-layout extracted netlists. Assura RCX (Cadence) is used to extract all the parasitic elements on the whole circuit with a step of 1 attoFarad. Transient simulations are run with Eldo (Mentor Graphics) because of the effectiveness of its DC convergence algorithm in presence of floating filling shapes. The simulations periods are about 100 ns under the following conditions:
• Process is nominal
• Vdd = 1.2V
• Temperature is 25°C

The output signal is post-processed through a Fast Fourier Transform (FFT) to obtain the individual harmonics (Fig.3).
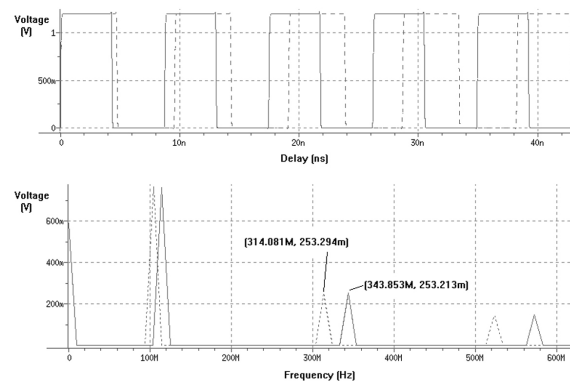

Figure 3. Effect of metal 2 filling on the standard cells for the RO_I structure in time and frequency domains. The solid line stands for the reference structure (without filling). The dashed line stands for a structure with inter-layer filling above interconnects.

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The filled RO timing characteristics are represented by 9 values: the delay, the fundamental gain and the gains and frequencies of the 1st, 2nd and 3rd harmonics.

3. METAL FILLING PATTERN DEFINITION

To be able to quantify the influence of the metal filling on the standard cells and their associated interconnect, a complete set of filling patterns has to be simulated. The choice of the filling patterns size (width and length), position, spacing and density can lead to generate a huge number of test cases. To overcome this limitation, a DOE approach is used to generate the filling pattern size and position as presented in Fig.4. H and W are respectively the height and the width of a filling block, and vary from 0.8µm to 3µm. H_v and W_v are respectively the height and the width of the space between filling blocks. H_i and W_i are the coordinates of the instantiation point of the filling pattern. Complete sets of metal filling patterns are defined for both the RO_C and the RO_I structures. From the simulations of each complete DOE, a polynomial model is established that gives the timing characteristics of a filled RO (9 values) as a function of the fill patterns size and position (6 variables). Since the coupling capacitance effect is non-
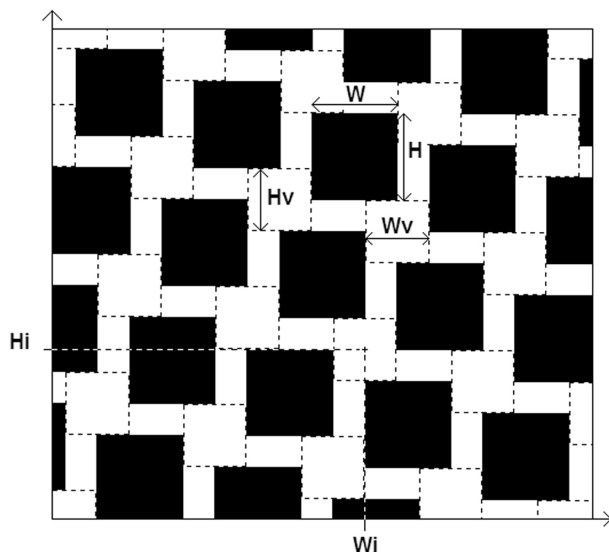

Figure 4. The 6 DoE variables: size of a dummy fill (*H,W*), size of the virtual fill between 4 dummy blocks (H$_V$,W$_V$), instantiation point (H$_i$,W$_i$).

linear, direct and square contributions of variables are parts of the model. In order to increase the accuracy and due to the large number of variables (6), coupled effects of inputs are also taken into account. The polynomial model is given as follows in Eq.1:

$$\forall k \in [1,9],$$
$$y_k = \sum_{1 \le i \le 6}(a_{k,i}X_i + a_{k,ii}X_i^2) + \sum_{1 \le i \le 6}\sum_{i < j \le 6}a_{k,ij}X_iX_j \quad (1)$$

$\forall k \in [1,9], \forall (i,j) \in [1,6]^2$, y_k is one of the outputs, $a_{k,i}$ and $a_{k,ij}$ are the coefficients of the model related to output k and X_i is one of the input variables.

Both models are validated by comparing the simulated filled RO responses and the computed ones for different filling densities. The Fig.5 presents the comparison of delays obtained with the model and with simulations for the RO_I case.

For each density, the filling patterns with the maximal and minimal impact on delay are considered. The worst timing characteristics difference is 1.3%, for the high density and maximal impact configuration, thus validating both models.
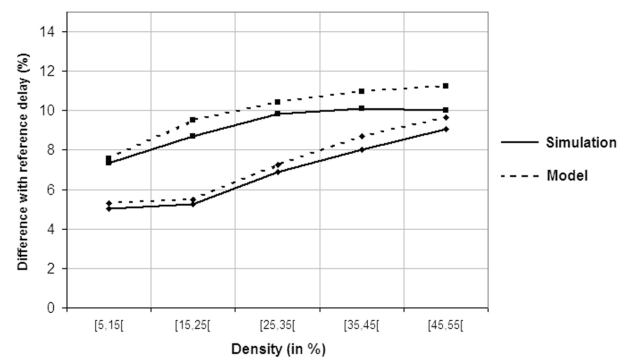

Figure 5. Comparison between simulation results and the model results. The solid line shows the simulation results, and the dashed line stands for the model predictions.

4. STATISTICAL ANALYSIS OF FILLING IMPACT ON METAL 1 INTERCONNECTS

The following studies focus on a statistical analysis of delay variation due to filling pattern characteristics on interconnects for the metal level directly related to standard cell interconnections (i.e. metal 1). The first one consists in evaluating the impact of intra-layer fill pattern position and size on the RO delay. To do so, 1000 fill patterns are randomly generated and 1000 filled RO delays computed by the polynomial model. The Fig.6 presents the difference between the unfilled RO and filled RO delays, expressed in percent, for intra-layer case.
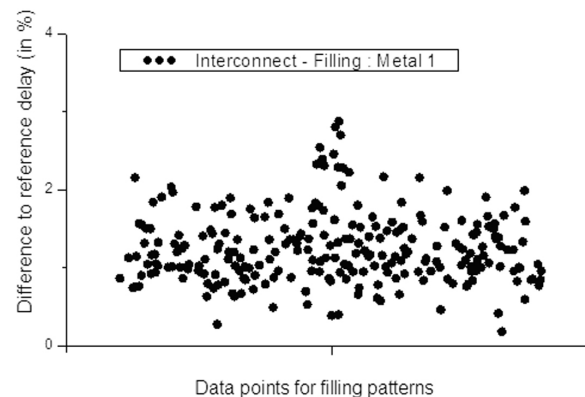

Figure 6. Dispersion of the delay impact of metal 1 filling on metal 1 interconnects (intra-layer case).

$$\forall k \in [1,9],$$
$$y_k = \sum(a_{k,i}X_i + a_{k,ii}X_i^2) + \sum\sum a_{k,ij}X_iX_j$$

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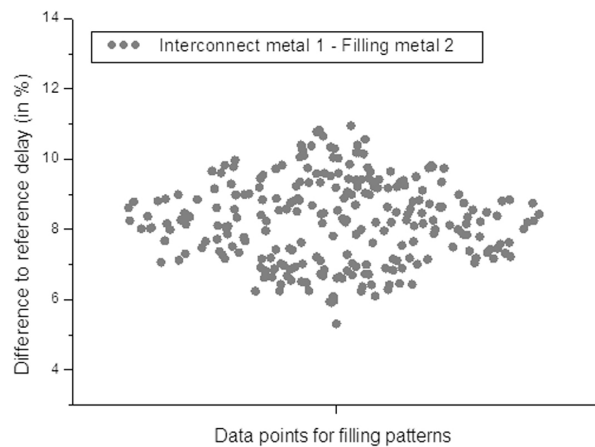In a similar way, the Fig.7 presents the results obtained for the inter-layer case.

Figure 7. Dispersion of the delay impact of metal 2 filling on metal 1 interconnects (inter-layer case).
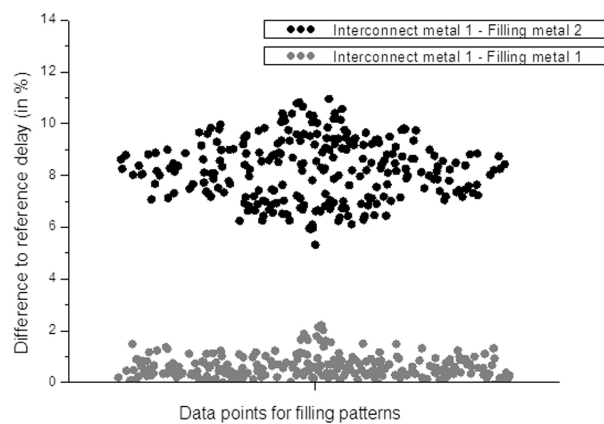

Figure 8. Comparison between dispersions of delay impact on metal 1 interconnect induced by metal 1 and metal 2 filling.
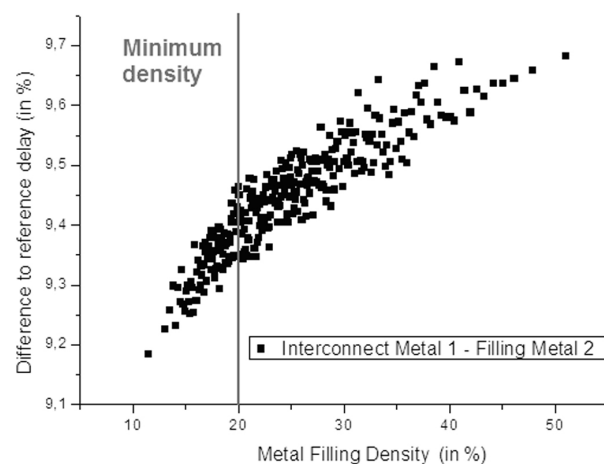

Figure 9. Dispersion of the impact of metal 2 filling on metal 1 interconnect versus metal 3 filling density.

Figure 8 shows that for a metal 1 interconnect, the impact of metal 1 filling is clearly lower than the metal 2 filling impact. This can be explained by two facts. The first is that the coupling capacitance is higher between two metal shapes separated by an interlayer dielectric layer than between two metal shapes at the same metal level. This is due to the standard spacing between interconnect and a filling block that was defined enough high to reduce the coupling capacitance impact. The second point is the importance of the fringe capacitance, because the height of interconnect is higher than its width. The Fig.9 presents the difference between the unfilled RO and (Interconnect metal 1 + Filling metal 2) structure delays, expressed in percent versus the filling density for 50k different filling patterns.

## 5. FILLING IMPACT VERSUS PROCESS VARIATIONS

Designers have to guarantee the performances of the circuits and allow a margin to ensure the circuit robustness versus process variations. The goal of this section is to quantify in which way the filling may influence the margin allowed by the designer versus process variation for cell design and local interconnects.

Filled RO timing models are generated under nominal process condition. So to be able to use the timing model in a front-end process variation context, one must be sure that the process variations have no influence on filling impact. To validate this point, the following studies are performed:

- A Monte-Carlo analysis on process parameters is run on a filled RO.
- The same Monte-Carlo analysis is run on the RO without filling.
- The timing impact of the filling is computed with our model.

The parameters impacted by the Monte-Carlo analysis are length, width of transistors, carrier mobility (impacts Vt, Isat, etc).The two Monte-Carlo analyses are represented Fig.10, where it clearly appears that the distance x in delay separating the results for the RO without filling and the one with filling corresponds to the timing impact computed with the model.

This study validates the fact that the impact of front-end process variations and the one of the filling pattern are independent. In order to show the influence of filling patterns on the delay versus front-end process variation, Monte-Carlo analyses are performed on unfilled RO and then the filling impact computed with our timing model is added. The filling delay impact is computed for a set of 100 different filling patterns, using a pseudo random pulling on the pattern characteristics (size, position, and spacing). Using the analytical model, it was easy to define the 6 inputs (filling pattern characteristics) corresponding
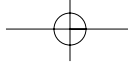
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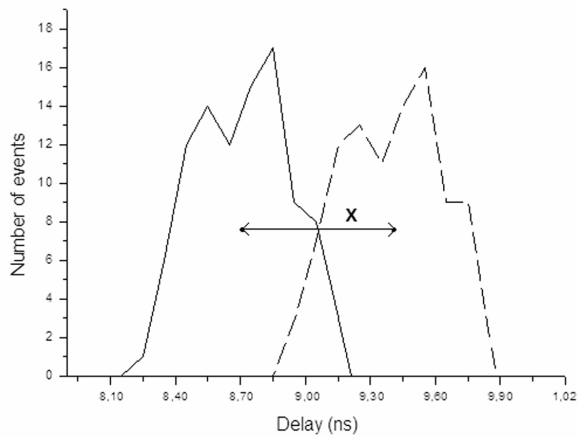*Remy, Coll, Picot, Mico & Portal*

Figure 10. Comparison between timing dispersion due to process variation on the reference RO and the filled one: The solid curve shows the results for reference RO (without filling), and the dashed one is for the RO with M2 filling on interconnects. The filling curve is shifted from the reference of a delay that is exactly equal to what the model predicts.
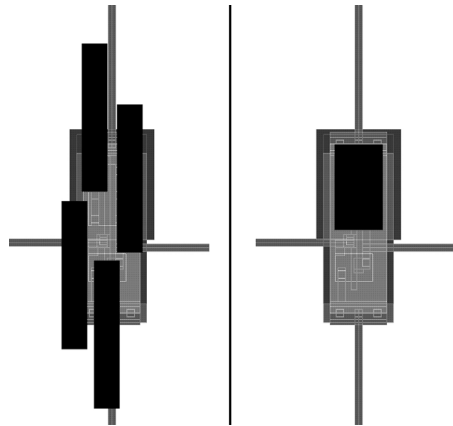

Figure 11. Inverter with most (on the left) and less (on the right) critical filling patterns, in terms of impact on delay. The metal 2 filling shapes are represented in black.

to minimum or maximum model output (delay). The least and the most critical filling patterns in terms of impact on delay for standard cells are shown in Fig.11).

In all the cases, the filling pattern generation is performed with our timing model by changing the 6 input variables.

The Monte-Carlo analysis for the unfilled ROC, the filling pattern delay shift and the Monte-Carlo analysis of the filled ROC are presented Fig.12.

It clearly appears that the filling influence on the standard cell is very limited. Considering the resulting Monte-Carlo analysis of the filled RO_C, the filling patterns introduce an increase of the delay mean value of 0.54%, below 1% for the spread and of 2.3% in the worst case.

The Monte-Carlo analysis for the unfilled RO_I, the filling pattern delay shift and the Monte-Carlo analysis of the filled ROI are presented Fig.13 and errors bars are drawn on Fig.14 in order to show the spread across the random runs.
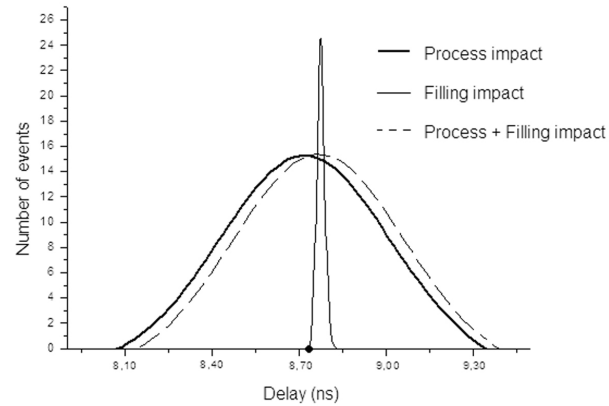

Figure 12. Comparison between timing dispersion due to process variations and to metal filling on RO_C structure: The three Gaussians represent the dispersion of the impact on timing. Gaussian events are shown in Y axis. The bold solid one, the thin solid one and the dashed one respectively stand for process impact, filling impact and (process + filling) impact. The black dot shows the delay of the reference RO (without filling on standard cells).
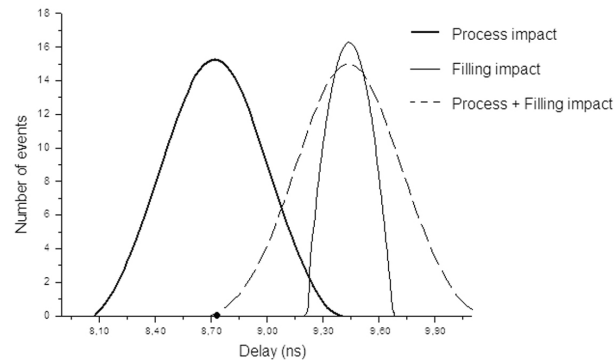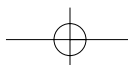

Figure 13. Comparison between timing dispersion due to process variations and to metal filling on RO_I structure: The three Gaussians represent the dispersion of the impact on timing. Gaussian events are shown in Y axis. The bold solid one, the thin solid one and the dashed one respectively stand for process impact, filling impact and (process + filling) impact. The black dot shows the delay of the reference RO (without filling on interconnects).

The inter-layer filling influence on the local interconnect metal 1 is important. Considering the resulting Monte-Carlo analysis of the filled ROI, the filling patterns introduce an increase of the delay mean value of 8.2%, of 4.1% for the spread and of 11.67% in the worst case.

The inter-layer filling influence on the local interconnect metal 1 is important. Considering the resulting Monte-Carlo analysis of the filled RO_I, the filling patterns introduce an increase of the delay mean value of 8.2%, of 4.1% for the spread and of 11.67% in the worst case.

These studies show that considering the standard cell with their associated metal 1 interconnect, filling increases the delay. Moreover, depending on the filling characteristics, the spread of delay is also changed. Consequently, standard cell designers have to validate the cell robustness for worst delay and larger windows, considering a large set of pattern filling in
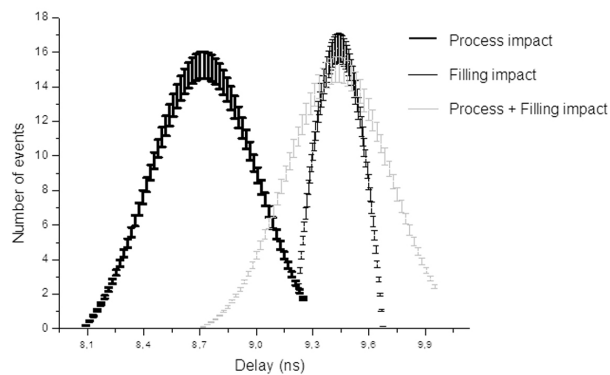
Figure 14. Error bars for the comparison between timing dispersion due to process variations and to metal filling on ROI structure: The three curves are the same as Fig.13, plotted with error bars to show the spread across the random runs.

addition to the process variations. Since the filling is often generated after the cell design step, this can allow preventing timing deviation and soft defects.

6. FILLING INSERTION IN THE CORNER DEFINITION

Designers have also to evaluate the standard cell performances for different corner cases, defined by the Process, Voltage and Temperature (PVT) conditions. The considered corners are defined below:

- Min. corner - P = best case, V = 1.32V, T = -40°C.
- Typ. corner - P = nominal case, V = 1.2V, T = 25°C.
- Max. corner - P = worst case, V = 1.08V, T = 100°C

The section 5 results show that the filling influence on the standard cells with their associated interconnects should be taken into account when estimating standard cell performances. In order to increase robustness of cells versus variations of filling impact on timing, metal fill-patterning effect must be included in the simulation flow. In this aim, the concept of PVTF corners is introduced, with F standing for filling density. In the corner definition, PVT stands for the extreme variations that may occur for example for a given cell. In our case the F corner stands for the extreme filling context around a given cell, but doesn't stand for filling pattern variation. The corners are defined, including the filling patterns for a full range of densities (5 to 55 %), as follow:

- Min. corner - P = best case, V = 1.32V, T = -40°C, F = best case.
- Typ. corner - P = nominal case, V = 1.2V, T = 25°C, F = nominal case.
- Max. corner - P = worst case, V = 1.08V, T = 100°C, F = worst case.

with "F = best case" standing for filling patterns with the lower influence on delay, "F = nominal case" standing for filling patterns with the mean influ-

ence on delay and "F = worst case" standing for filling patterns with the most influence on delay.

The delay shift introduces on each corner by the filling patterns, considering a range of 5 to 55% of density, are presented Fig.15, Fig.16 and Fig.17 respectively for the Min. corner, the Typ. corner and the Max. corner. Fig.18 shows the three curves in a same graph for comparison.

These curves show an increase of the spread of timing deviation across process corners due to metal fill. This is directly linked to the three filling corner parameters that are chosen to have little impact for the Min corner, medium impact for Typ corner and high impact for Max corner. This spread variation across process corners also proves the necessity to add the metal filling impact to the variability factors.

Using these corners PVTF, the standard cells timing performance estimation can be performed considering a complete set of filling patterns context possibilities.
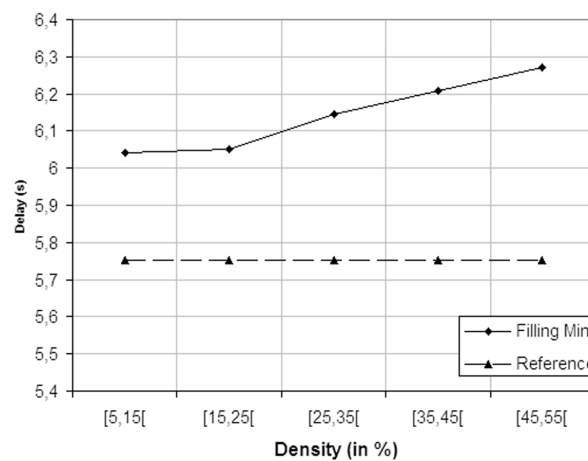

Figure 15. Impact of minimal filling pattern versus density ranges for Min corner. The dashed line shows the reference delay. The solid thin curve stands for filling pattern that implies minimum impact on timing.
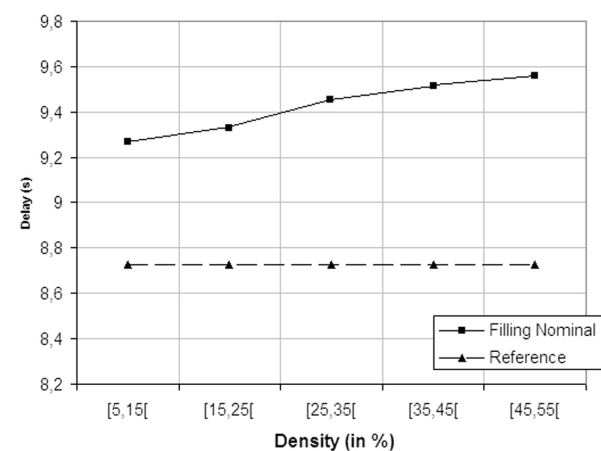

Figure 16. Impact of nominal filling pattern versus density ranges for Typ corner. The dashed line shows the reference delay. The solid thin curve stands for filling pattern that implies nominal impact on timing.

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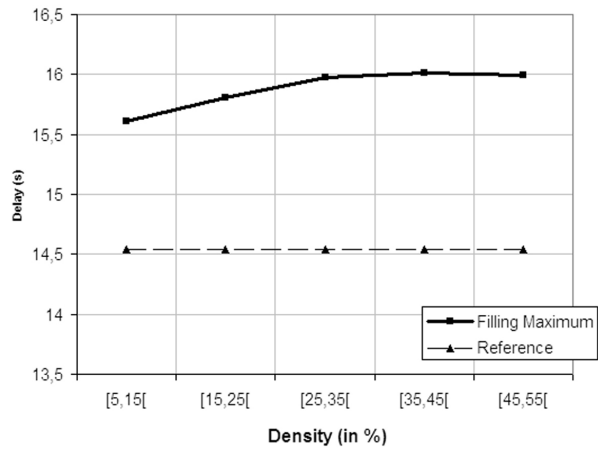*Remy, Coll, Picot, Mico & Portal*

Figure 17. Impact of maximal filling pattern versus density ranges for Max corner. The dashed line shows the reference delay. The solid bold curve stands for filling pattern that implies maximal impact on timing.
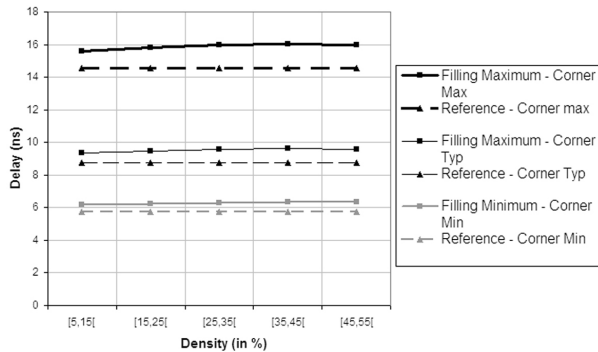

Figure 18. Comparison between filling impact (Minimum, Typical, and Maximum) on delay for respective corners (Min, Typ and Max).

7. CONCLUSION

The main objective of this paper is to study the delay impact of staggered metal filling on the standard cells and their associated local interconnects. In this aim, a polynomial model expressing filled RO timing as a function of the filling patterns characteristics is developed using a DOE approach. The model is first successfully validated and then used to study the influence of the filling context versus process variations for the standard cells delay. It clearly appears that the filling context magnifies the delay variations introduced by the process variations. Consequently, a concept of filling corner is introduced to allow designer to evaluate standard cell performances taking into account the filling context. Since metal filling is often inserted after the cell design step, using PVTF corner will allow designer to simulate their cell before filling generation, choosing best, nominal or worst cases of filling impact. These cases are defined using results given by the analytic model. This methodology increases the robustness of cells versus delay impact induced by filling patterns inserted variations.

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