An Integrated Switch in a HV-SOI Wafer Technology, With a Novel Self-Protection Mechanism

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ABSTRACT

An integrated switch to control electrical stimuli in implantable medical devices is presented. First a self-biased protection mechanism to avoid V_{GS} reaching maximum rated value is presented. Then, using a HV-CMOS technology this technique is incorporated in a fully integrated switch, to control 0 to 16V, and 0 to 30 mA, pulses for implantable stimulators. Because of the low supply voltage V_{DD} between 2 to 5V, and safety considerations in implantable devices, special level shifters, drivers, and a voltage multiplier, that drive a large 40000µm/3µm dual-in-series PMOS switch, were necessary for the circuit. The circuit was fabricated in a HV 0.6µm CMOS technology in SOI wafer for transistor isolation, and tested. Measurement results that closely fit the expected performance of the circuit are presented.

Index Terms: High voltage CMOS, HV technology, medical devices.

1. INTRODUCTION

Modern CMOS technology usually incorporates thick oxide possibility to allow certain transistor gates to be driven by higher voltages. In a deep submicron technology a thick oxide may allow 5V inputs, and in the so called High Voltage (HV) technologies the limit is extended to 12 or 20 Volts. While gate to source (V_{GS}) and bulk (V_{GB}) voltage is limited by the gate oxide strength, in a typical HV CMOS transistor the drain may support up to for example 60 Volts (drain to source or to gate V_{DS} , V_{GD}) [1].

In HV mixed mode circuits, low voltage logic regularly drives high voltage transistors. Level shifters like the one in Fig.1, are a known, useful, circuit block that translate between different digital voltage levels, but both below the maximum rated V_{GS}. To translate larger voltages, a bit more complex circuits can be employed [1] that normally rely in current signalization and assume a fixed high-side voltage (that is not present in every circuit).

In this paper a novel circuit technique will be presented to deal with large voltages using CMOS transistors. The idea can be summarized as follows: consider a PMOS transistor, to turn it off the gate and the source can be connected to each other; to turn it on the gate is pushed as much as possible to the most negative voltage in the circuit V_{SS} (V_{SS} can be a negative voltage). The idea is to include a control loop that stops pushing the gate to the negative voltage if V_{GS} voltage becomes close to the maximum rated for the technology. In this way the PMOS is safely operated, but at the same time is turned on with a maximum V_{GS} voltage to achieve a minimum on-resistance, which is normally desirable.

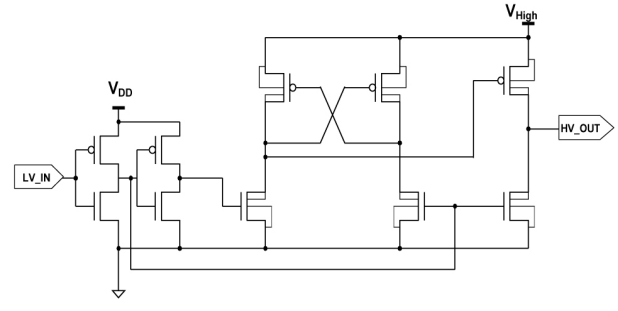

Figure 1. A know CMOS level shifter translates a LV (0-VDD) digital signal, into a HV one (0-VHigh) with no static power consumption

In the following section, the circuit technique will be applied to a PMOS integrated switch that is part of an implantable medical device. Most implantable medical devices, are electrical stimulation systems, that deliver either current or voltage pulses to the patient according to different requirements. Stimuli section of the circuit may consist of the basic elements shown in Fig.2: a stimuli generator (either a voltage or current source), electrodes which connect the tissue to the device, a switch that toggles the electrical connection of the electrodes, and a control

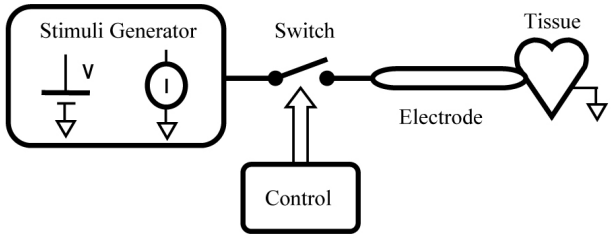

Figure 2. Typical stimuli section of implantable medical device.

block that decides when and for how long a stimulus should be applied

Stimulation can be done either by applying a voltage in the tissue from a few hundreds of mV to well over 10 V or driving a current through the tissue, ranging from a hundred µA to tens of mA [2]. Because of the large voltages involved, a HV 0.6 µm CMOS technology in SOI wafer [3] was selected to allow switching up to 16V stimuli. The use of a SOI wafer in a CMOS process allow to fabricate single or multiple MOS transistors isolated in silicon 'islands', separated from the wafer by the buried oxide layer, and in between them by oxide trenches. The SOI wafer helps to fulfill safety requirements of medical devices (at a single transistor failure DC current must not flow to the tissue)[2][4][5], at the same time that prevents latchup on a wide range of operation conditions.

A. A novel V_{GS} overvoltage protection circuit.

The circuit in Fig.3 shows a PMOS switch M1, which may be a large output driver transistor that connect the voltage V_{IN} to V_{OUT}. While V_{DS1} (V_{IN}-V_{OUT}) may be large for example up to 50-60V, V_{GS1} is limited to a much lower value, 5V in standard CMOS, 18V in the target technology. To turn on M1, a driver may connect its gate to V_{SS} (the most negative voltage in the circuit) but there is a risk of gate oxide damage if V_{GS1} (Gate-Source voltage of M1) exceeds maximum rated. To overcome this problem a voltage control loop is proposed. V_{CTRL} is a low voltage logic signal varying between a low supply voltage V_{DD} (i.e. 3 V) and V_{SS}; when $V_{CTRL} = V_{DD}$ M2 is turned on if $I_{Ref} = 0$, V_{G1} is pushed to V_{SS} and M1 is turned on. But as I_{Ref} increases, the voltage drop in R1 increases as well, and M2 impedance dramatically increases (up to cut-off) and V_{G1} may reach an equilibrium voltage well above V_{SS}. I_{Ref} is a function of V_{GS1} voltage because of the n diode-connected Mdi transistors, which copy their current to the V_{G2} node through Mci transistors. As V_{GS1} increases, I_{Ref} increases in a strongly-non linear way, and an equilibrium V_{GS1} voltage close to the voltage drop of the stacked Mdi diodes is achieved. V_{GS1} voltage during M1 conduction is a function of n, the number of stacked Md transistors, their threshold voltage and M2, R1, characteristics. These circuit elements shall be designed according to rated V_{GS} voltage for the technology and corner cases. When $V_{CTRL} = V_{SS}$, M2 transistor is opened and R2 pushes V_{G1} to V_{IN} thus M1 is opened. R2 has been placed to illustrate circuit operation but may be substituted by a more complex circuit to avoid static current consumption when M1 is turned on, or to increase speed. Note that this control loop draws some current when M1 is turned on (that can be minimum with a careful design), but may operate regardless of V_{IN} ranging to an arbitrarily large value. A modified version of the circuit in Fig.3 will be employed in the following section, to implement a stimuli delivery switch for implantable medical devices.

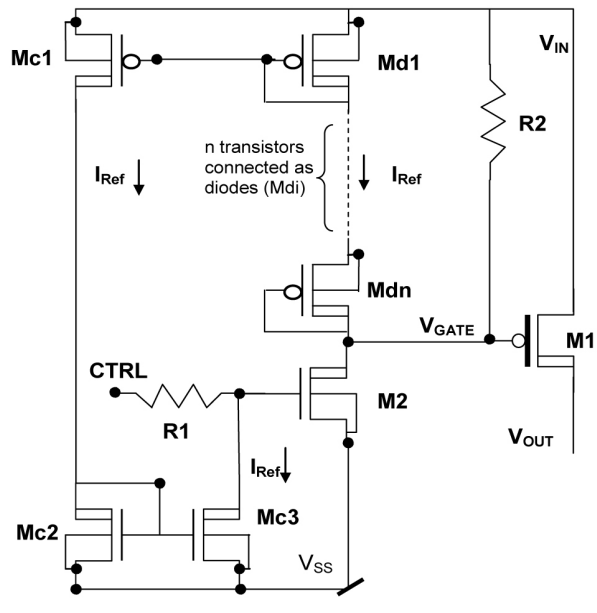

Figure 3. Proposed control loop for VGS over-voltage protection.

Finally, it should be pointed that in regular switching applications M1 size is very large thus the use of the extra circuit elements count is valid. In the example of section 2 a large M1 (W/L = 40000µm/3µm) dual transistor is employed, and the control loop area is an order of magnitude smaller.

B. HV-Technology

Introducing new process layers, a HV CMOS technology allows the fabrication of devices that can support elevated voltages. Regular 5V core CMOS can also be fabricated, as well as double poly capacitors and high-resistivity poly resistors in the target process. In Fig.4 a HV NMOS transistor (named nhv) vertical cut is shown. Nhv has the usual structure of a HV transistor, incorporating a thick gate oxide that enables up to 18V V_{GS}, V_{GB}, and the drain diffusion is growth into a N-Well to complete a diffused drain to support elevated V_{DS} voltages. To help the interpretation of the circuits in this work (different kinds of

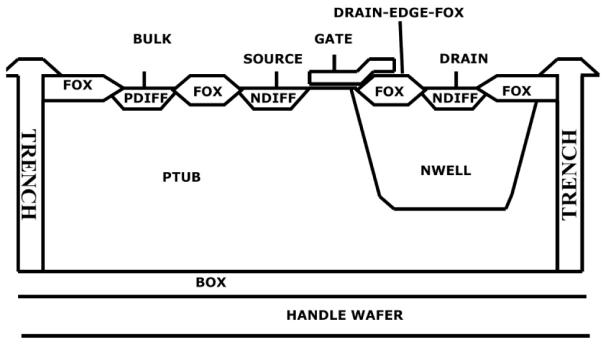

Figure 4. Vertical cut view of a typical HV NMOS (nhv).

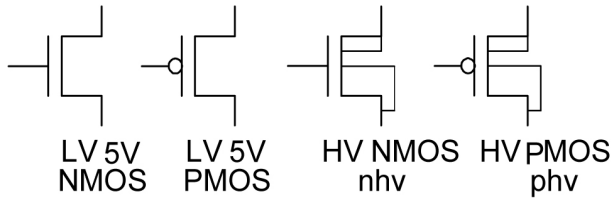

Figure 5. Symbols for the different kinds of transistors used: LV NMOS and PMOS, and HV NMOS (nhv) and PMOS

HV, LV, transistors are used) in Fig.5 the symbols used for each type of transistor are shown. HV transistors are not symmetrical, the drain which is designed to withstand the highest voltage, is marked with a double line.

2. AN INTEGRATED SWITCH FOR IMPLANTABLE MEDICAL DEVICES

The circuit to be designed is simply a switch that can connect/disconnect the electrodes from the electric pulse generator in Fig.1. In Fig.6 a detailed scheme is shown, a microcontroller commands this special switch through the Ctrl signal.

Initial specifications follow:

- The switch must operate correctly with commutation voltages V_{IN} from 100 mV to 16V.
- It must work with a low voltage (LV) side supply V_{DD} from 2V (end of life of a lithium-iodine pacemaker like battery) up to 4.2V (a fully charged rechargeable medical grade battery) [6], [7].
- The switch must have an ohmic resistance of 5Ω or less, in all ranges of operation. To fulfill this requirement in conjunction with V_{IN} close to 0, a voltage inverter that generates V_{SS} = -V_{DD} below ground was included (using an external capacitor). SOI wafer technology greatly simplifies handling a V_{SS} below circuit GND.
- The switch must be symmetrical, V_{IN} and V_{OUT} nodes can be exchanged with no further modifications in the circuit.
- A null (below 20nA) static current consumption when not stimulating is mandatory.
- Parasitic current spikes during on/off time must be minimum, as well as current spikes through the switch when it is open and the tissue voltage varies. The latter will be denoted as crosstalk, and may be present in the case of multiple stimulation channels.
- Safety: the failure of a single circuit element (for example a punctured MOS gate) must not cause a DC current flow through the tissue larger than a few micro-amps because otherwise it may be a risk for the patient.

A. Circuit Design

In this section the subcircuits used in this design will be presented. The complete circuit is shown in Fig.7, with two main PMOS transistors M1, M2, in series and their driving circuitry. The use of two transistors allow the stimuli to pass or not into the tissue, in both directions (the designed switch is symmetrical). The transistors were designed to have an impedance below 5Ω.

The circuit consists of:

- Two Negative Level Shifters (LSN1(2)).
- Two Special Level Shifters (SLS1(2)).
- Two PMOS transistors acting as switches (M1,M2).
- Two Negative Drivers (NegD1(2)).
- One Generator of V_{SS} (Gen_V_{SS}) (uses external capacitor).
- Two Drivers (DRV1(2)).
- One Control loop (LOOP).

In Fig.8 the LSN subcircuit is shown, that is a variation of the one in Fig.1 [1]. The LSN subcircuit

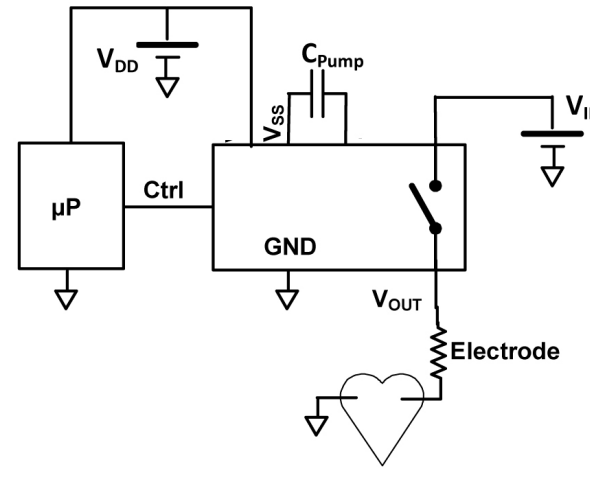

Figure 6. Typical application scheme for designed switch. A µController commands the delivery of stimuli to bio-logical tissue.

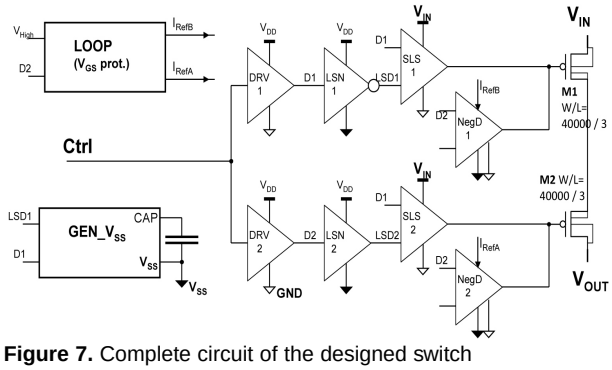

Figure 7. Complete circuit of the designed switch

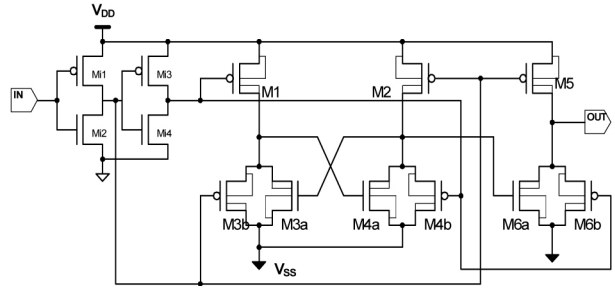

Figure 8. Negative level shifter. HV transistor sizes are: M1, M2 60µm/3µm; M3, M4 10µm/3µm ; M5, M6 20µm/3µm.

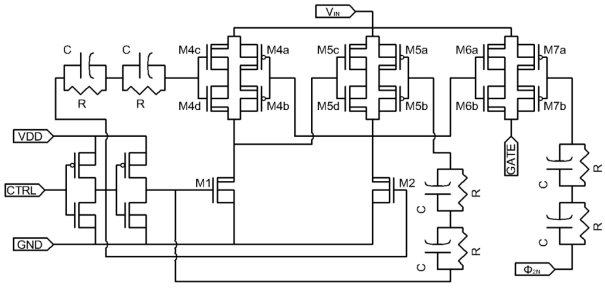

Figure 9. Special Level Shifter schematic. R=650kΩ, C=5pF. Transistors sizes (µm): LV: 100/3; M1, M2: 60/3; M4, M5: 10/3; M6, M7: 400/3.

receives a digital signal between 0-V_{DD} and transforms it into a V_{SS}-V_{DD} signal. This signal is needed by the SLS and NegD subcircuits. Its two states are:

- High state: When IN = '1', the transistors M2, M3, M6, are opened and transistors M1, M4, M5, are closed. This ensures OUT = V_{DD}.
- Low state: When IN = '0', the transistors M2, M3, M6, are closed and transistors M1, M4, M5, are opened. This ensures OUT = V_{SS}.

In Figure 9 the Special level shifter SLS is shown. This subcircuit connects its output, GATE, with the input, V_{IN}, when the CTRL signal is a logical 0. If CTRL is a logical 1, GATE is left in third state. ϕ_2N signal is generated by the LSN used as an inverter. The SLS subcircuit is very similar to the LSN, but with a few differences:

- All transistors connected to V_{IN} (M4, M5, M6, M7) are implemented with two transistors connected in series but flipped. This configuration with two diodes connected in opposite directions, prevents current circulation through those transistors in case of voltage peaks in V_{IN} (remember V_{IN} is connected to tissue and its voltage may vary).
- The only connection to the output GATE is V_{IN} through M6/M7, which is controlled by CTRL, setting GATE to high impedance (third state) when CTRL=1.
- Because V_{IN} can vary from 16V to 100mV, M4, M5, M6, M7 are connected like HV transmission gates, ensuring operation in all the voltage range.
- Because M4, M5 and M7 gates are connected to V_{DD} when no stimulus is present, if any of this transistors oxide is punctured (single failure), there will be a direct current path into the tissue that must be avoided for safety reasons (the return current is assumed to GND because the non-active electrodes as well as the medical device case are connected to GND when not delivering a stimulus). The connection of these gates through an RC circuit, limits this current to an acceptable level (two capacitors are used to withstand the HV in case of failure).

The actual switch is implemented by two PMOS transistors with W=40000µm L=3µm (minimum length for HV transistors) connected in series but flipped (M1, M2 in Figure 7), to prevent conduction through Bulk-Drain diode if the switch is off and $V_{IN} > V_{OUT}$. Such large transistors were necessary to achieve a total conduction impedance close to 5Ω when the battery is almost discharged (V_{DD} = 2V).

Fig.10 shows the Negative Driver (NegD) subcircuit. The Negative Driver connects its output GATE to V_{SS} (depending on the control loop current I_{Ref}) when the CTRL signal is a logical 1. If the CTRL signal is a logical 0, the GATE is left in third state. CTRLLS is generated by a LSN and it is in phase with CTRL. When $I_{Ref} \approx 0$, and CTRL = '1', the transistor M2 is closed and Gate is connected to V_{SS} through M1 and M2, but if I_{Ref} is large enough, M2 will be open and GATE will be connected to GND through M3 and the diode. The diode also ensures that when $I_{Ref} \approx 0$ no conduction between GATE and GND occurs. To summarize, NegD connects GATE to a low voltage when CTRL = '1' and leaves it in third state otherwise. The low voltage is either V_{SS} if $I_{Ref} \approx 0$ or GND. Note that this is a variation of the circuit proposed in Section 1.A that allows the use of a relatively large negative V_{SS} to drive the gate of the main PMOS.

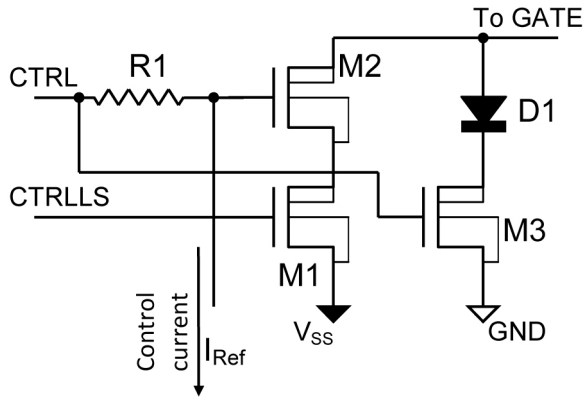

Figure 10. Negative Driver Schematic. Transistors sizes: M1, M2, M3 600µm/3µm; R1=683k .

Both the LSN and the NegD require a negative voltage (V_{SS}). This voltage is generated on-chip by the Gen_Vss subcircuit shown in Figure 11, which uses an external pump capacitor C_{pump} to generate V_{SS} = (-V_{DD}). Since a negative V_{SS} is only needed when stimulating, V_{SS} is only generated (pumped to a negative value) when CTRL= '1'. CTRLLS is derived from a LSN using an inverted output. Two states are considered in the operation of Gen_Vss:

- V_{SS} = 0 state: When CLK (CTRL) = '0' the node CAP is connected to V_{DD} through Mi2 and the node V_{SS} is connected to GND through M1 and M2. Th C_{pump} is charged to V_{DD}. The diode helps only at the circuit's start-up.
- V_{SS} = -V_{DD} state: When CLK = '1' the node CAP is connected to GND but the capacitor has no discharge path, so the node V_{SS} acquires a negative voltage (–V_{DD}). The DRV subcircuits are standard LV ones.

Finally in Fig.12, the control loop subcircuit of Fig.7 is presented. This subcircuit generates the current I_{Ref} for the NegD blocks. The loop copies the current through the M0 branch to the output transistors M2 and M3. If there is no stimulation, CTRL = '0' and M0 is open so I_{Ref} = 0. When CTRL = '1', M0 is closed, but only if V_{High} is high enough to make forward current flow through the 6 stacked Mdi's diodes-connected transistors, does current actually flow through M0. Therefore the I_{Ref} current is only generated if CTRL = '1' and V_{High} is high enough. Note that this is a variation of the control loop proposed in Section I.A, where the reference voltage is measured to fixed ground instead of V_{GATE}.

C. The complete switch

The topology of the complete switch is shown in Fig.7. Stimuli current conduction is done through transistors M1, M2. To open the switch, CTRL = '0', SLS1 connects M1's gate to V_{IN} and SLS2 M2's gate

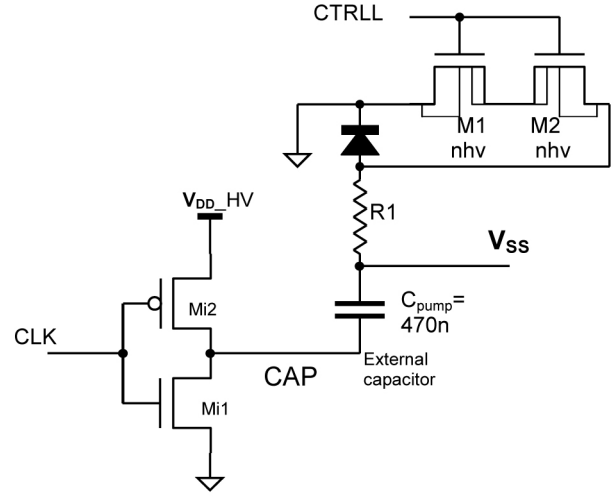

Figure 11. V_{SS} generator circuit, pumps V_{SS} to (-V_{DD}). Transistors sizes: Mi1, Mi2: 200µm/3µm; M1, M2: 60µm/3µm; R=100 .

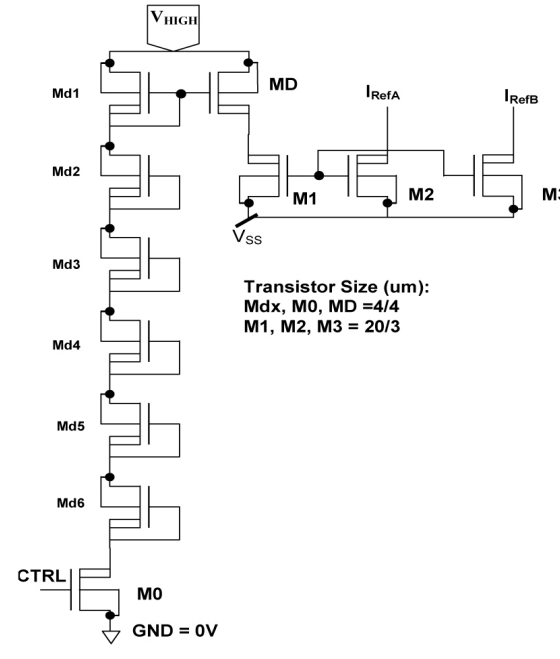

Figure 12. Loop subcircuit schematic. This is a modification of the circuit proposed in Fig.3.

to V_{OUT}. Because V_{IN} and V_{OUT} may vary in a wide range (in fact input/output can be exchanged) only in this way a V_{GS} = 0 is guaranteed in all conditions and effectively open the transistors. In this case V_{SS} = GND and no static current is consumed.

When the switch must be closed (CTRL = '1'), the SLS are not activate (SLS's outputs are in high impedance) and both NegD connect the gates to either GND or V_{SS} to ensure the transistors are closed. The negative voltage V_{SS} is necessary because the stimulus voltage can be very small (0.1V). On the other hand, for example when the stimulus voltage is very high (16V) and V_{SS} = -4V the V_{GS} ~ 20V and can damage the oxide. To overcome this problem, V_{High} must be connected to the highest voltage, either V_{IN} or V_{OUT}. Along this work

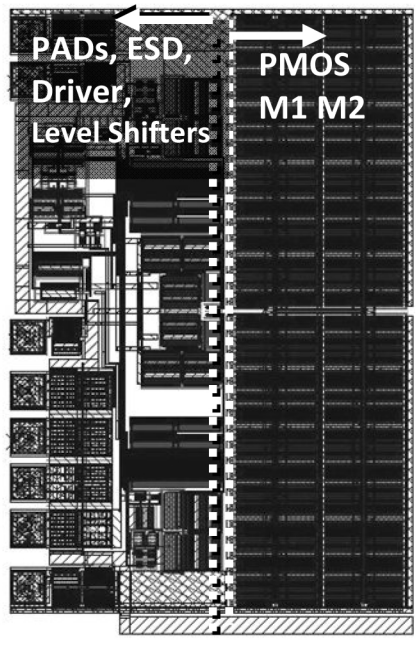

Figure 13. Complete circuit Layout

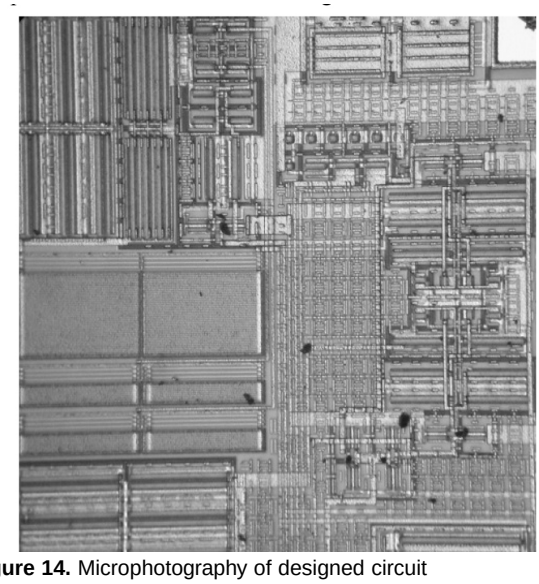

Figure 14. Microphotography of designed circuit

V_{High} will be assumed to be connected to $V_{IN} > V_{OUT}$. The subcircuit 'Loop' in Fig.7 was designed to generate a high enough current (I_{Ref}) to close the path to V_{SS} in NegD when $V_{High} > 12V$. In this way the circuit is protected for any voltage input while ensuring low impedance when the stimulus voltage is low.

To sum up the complete switch has two states:

- Open state: When CTRL = '0', SLS1 open M1 and SLS2 opens M2. V_{SS} = GND and no static current is consumed.
- Closed State: When CTRL = '1', Gen_Vss generates $V_{SS} = -V_{DD}$, NegD1 closes M1 and NegD2 closes M2. If VHIGH > 12V, I_{Ref} closes the path to V_{SS} and M1 and M2 gates are connected to GND, otherwise they are connected to V_{SS}.

In Fig.13, a complete layout of the switch is shown. It should be noted that in effect the two PMOS transistors (M1 and M2 in Fig.7) occupy half the circuit silicon area.

The other half is divided between driver circuitry, and large ESD protection structures that were custom designed because the voltages in the circuit include negative values (V_{SS}) and from GND to 16V with no fixed reference (V_{IN}, V_{OUT}, V_{High}). Fig. 14 shows a microphotograph of the Special Level Shifter and the V_{SS} generator.

D. Simulations

All simulations were conducted using the BSIM3 model [8] with typical model (TM) parameters unless otherwise stated.

In Fig.15 the simulated impedance of the switch is shown (essentially the on-resistance of series M1, M2, in Fig. 7) using different transistors models provided by the foundry: typical (TM), worst slow (WS) and worst power (WP). This simulation was conducted varying V_{DD} with a 200mV V_{IN} (close to the minimim). Figure 15 shows that in all three cases the impedance of the switch is always below 5Ω(a careful design of the metal wires connecting the transistors to the pads is also necessary to fit this condition, the plot in Fig.15 does not consider wire resistance).

In Fig.16 a second simulation is presented: a transient pulse where V_{OUT} is shown for the two extremes of V_{IN}, with a load impedance of 1kΩ, V_{DD}=4V. The switch works in all the necessary voltage ranges, for all transistors models. A 0.5μs delay was estimated in a worst case scenario.

Finally in Fig.17, the current through the open switch is plotted, when V_{IN} is connected to GND and a square wave of 8V amplitude was applied to V_{OUT}. Only crosstalk current spikes can be observed, caused by the charge change in the gate-drain capacitance of the main PMOS, but no DC current flows to/from

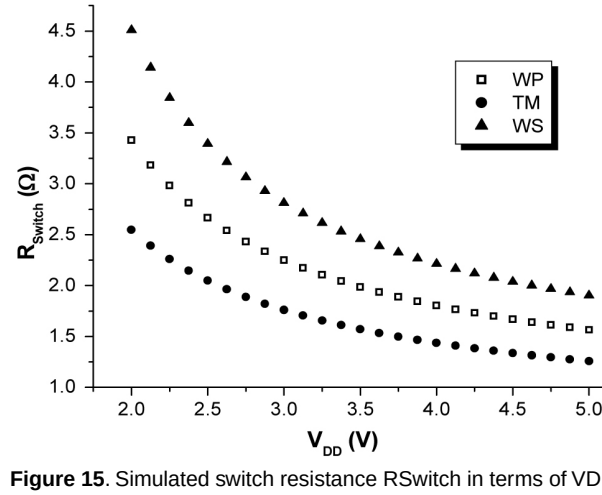

Figure 15. Simulated switch resistance RSwitch in terms of VDD.

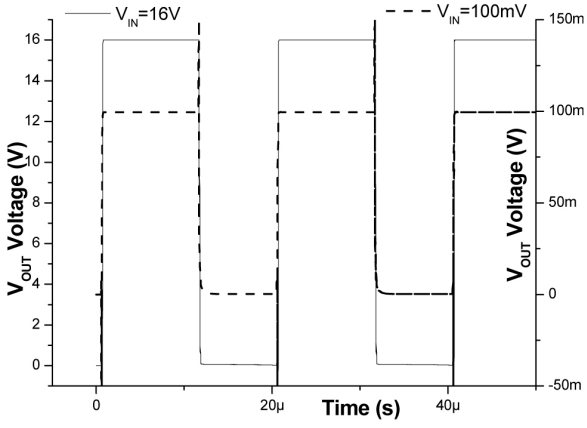

Figure 16. Transient simulation for square pulse in V_{OUT} with V_{IN}=16V, and V_{IN}=0.1V.

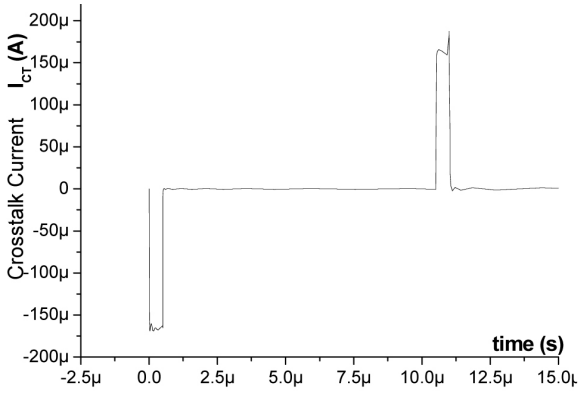

Figure 17. Simulated crosstalk current when the switch is open.

the tissue. The shape of these current spikes strongly depend on the rise time of the square wave, but the net charge ~30pC of the spikes does not.

3. MEASUREMENT RESULTS

The circuit was fabricated in a 0.6μm technology [3] and tested, some results follow. First of all in Fig.18 the measured impedance of the switch is shown for different LV supply V_{DD}, and HV stimuli $V_{IN} = V_{High}$ voltages.

These measurements were obtained using a few hundred ohms load, and a precision multimeter. In comparison to the curves in Fig.15, the measured resistance is larger probably due to an underestimated resistance of the metal wires. Contacts and metal wires total resistance was estimated as less than 2Ω.

The static power consumption of the switch cannot be precisely measured, but is less than 5nA. On the other hand, the dynamic power consumption is shown in Fig.19 while varying V_{DD}, $V_{IN} = V_{High}$ voltages. Dynamic power consumption has two components: the power consumption of the protection loop of Fig.12, and that of current spikes on transitions. But the former is the larger because power does not change to much with the switching frequency.

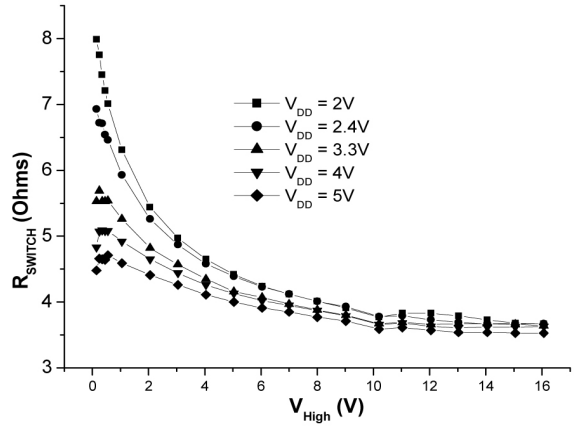

Figure18. Measured switch resistance R_{Switch} as a function of supply and stimulus voltages V_{DD}, V_{High}

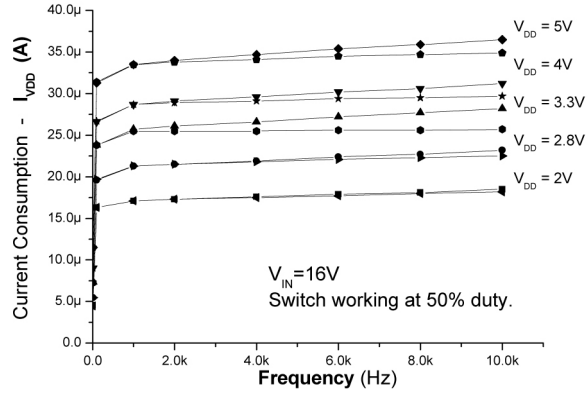

Figure 19. Measured dynamic current consumption of the switch when turned on/off at a given frequency and 50% duty cycle. Note the static power consuption when off is less than 5nA (measured).

The switch shows an excellent transient response, with a measured delay of approximately 600ns for turning on (from LV pulse edge to 50% of output signal) and 300ns for turning off.

However what is also important in the target application, is the impact of charge injection in the commutation of a current source. The simplified circuit and measurement results are shown in Fig.20. Two switches were connected to the same 100μA current source (that is a reasonable lowest value for current stimuli in medical devices) and alternatively turned on and off. The current source was implemented with a discrete operational amplifier and a pass transistor. On the measurement scheme of Fig.20 when the current is switched there is a current spike at the load even in the case of an ideal current source, due to charge injection. The plot shows measured spikes in terms of stimuli (V_{High}) voltages. Because for a larger V_{High} a larger amount of charge is taken from the gate of the main PMOS transistors when switching, the current spikes strongly depend on V_{High}. Up to few hundreds pC injected charge was measured, which closely fits previous calculations. Note the effect of charge injection is only important in the case of low current stimuli, as depicted in Fig.21 where the

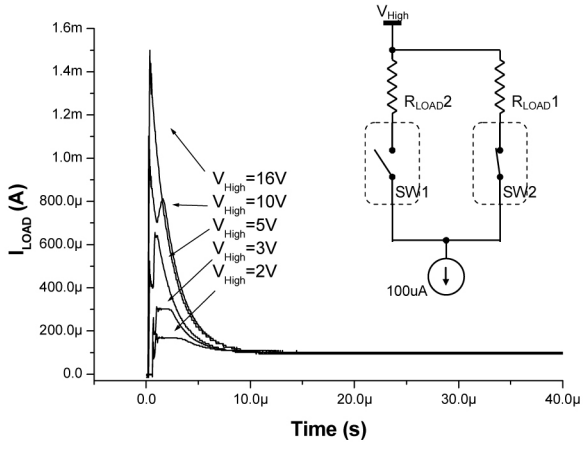

Figure 20. Measured charge injection of the switch when used in series with a current source. As expected, current spikes increase with V_{High}.

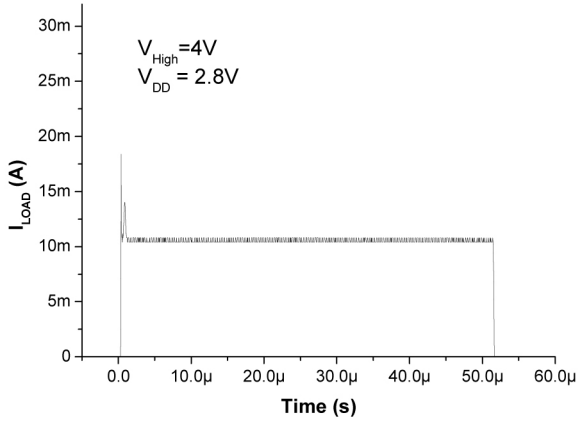

Figure 21. Measured 10mA current pulse using the scheme of Fig.20

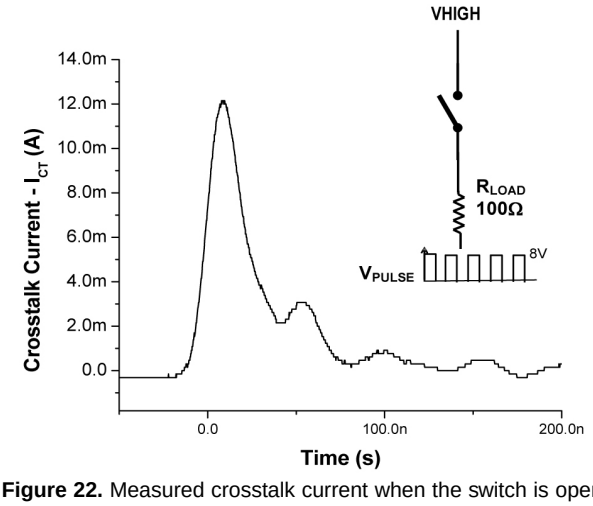

Figure 22. Measured crosstalk current when the switch is open.

shape of a 10mA current pulse obtained with the same measurement setup of Fig.20 is barely affected by charge injection.

Finally, in Fig.22 measured crosstalk is shown for the experimental setup of the picture. An 8V square input is connected at the output when the switch is open, and the transient current through the load is measured. The measured effect of crosstalk as expected is negligible, and the net charge of the measured current spike result a few tens pC after subtracted the (previously) measured charge of the parasitic capacitance of the probes. This value closely fits the simulated in Fig.17.

In Table I the most important measured, and simulated characteristics for the fabricated switch are shown.

Table I. Measured and simulated characteristics for the designed switch.

	Simulated / Calculated	Measured
Power supply VDD	2 – 5V	2 – 5V
Commutation voltage (V_{IN}/V_{OUT})	0 – 16V	0 – 16V
Commutation time	500ns	t_{ON}=600ns t_{OFF}=300ns
Switch resistance R_{switch}	2.5Ω + 2Ω(1)	6.5 Ω
	typ.@V_{DD}=2.7V, V_{High} = 200mV	.VDD=2.7V, V_{High} = 200mV
Crosstalk charge	30pC	< 50pC Typ.
Charge injection when switching		400pC (2) worst case

(1) 2Ω contacts & metal wires
(2) strongly depends on V_{DD}, V_{IN}

4. CONCLUSIONS

A self biased over voltage protection circuit technique was presented that allows driving MOS transistor in their full V_{DS} range above V_{GS} voltage limits. The complete design of an integrated switch, to precisely control electrical stimulation in implantable medical devices using this technique was presented. The circuit was fabricated in a HV, SOI wafer technology, and tested. Simulations and measured results for the circuit, fulfill specifications and safety requirements of modern implantable medical devices.

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