Voltage Controlled Delay Line with Phase Quadrature Outputs for (0.9-4)GHz Factorial Delay Locked Loop Dedicated to Zero-IF Multi-Standard Local Oscillator

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ABSTRACT

This paper presents the design and the measurement results of a novel Voltage Controlled Delay Line (VCDL) dedicated to an original architecture of Delay Locked Loop (DLL): the Factorial Delay Locked Loop (F-DLL). Based on the multiphase ring oscillator technique, the proposed VCDL offers, among others, two outputs in phase quadrature. These last ones allow the F-DLL to be zero-IF compliant and becomes a good candidate for multi-standard local oscillator. The proposed circuit has been fabricated in a 130nm CMOS-SOI technology from STMicroelectronics. Measurement results confirm the low quadrature phase error of the topology (inferior to 5°) and the ability of the F-DLL to synthesize the [0.9-4] GHz band, being suited for GSM up to WIMAX applications, while offering very interesting performances in term of phase noise and settling time.

Index Terms: Multi-standard frequency synthesizer, Factorial Delay Locked Loop, Voltage Controlled Delay Element, CMOS-SOI.

1. INTRODUCTION

Nowadays, RF communication standards for voice and data are widely being developed, particularly in the [1-4] GHz band (GSM, DCS, UMTS, Wi-Fi, Bluetooth, WiMax…). Strict requirements are linked with each application, and as a consequence, constraints are growing for communication terminals. Moreover, according to low-cost and low-power considerations, a RF transmitter should be able to deal with all of the existing standards. In this way, terminals should be completely reconfigurable. Software Defined Radio [1] is the best solution to achieve such a concept, but this kind of architecture is not yet available. Indeed, in such a system, the Analog to Digital Converter (ADC) and the Digital to Analog Converter (DAC) are located just after/before the antenna. But such a solution needs converter data rate to be in the order of 2 GBit/s with 16 bits resolution which is not yet suitable with wireless system low power constraints [2]. An intermediate solution is to use reconfigurable blocks in RF terminals [3]. The most appropriated RX-TX architecture to this latter solution is the zero-IF one. Indeed, it offers advantages in terms of integration and power consumption reduction compared to heterodyne and low IF one.

This paper focuses on one of the most critical block of the chain: the local oscillator (LO). In a RF transmission chain, the role of the LO is to provide the high frequency signal to the mixer. So, its characteristics can really impact in the overall expected performances of the chain. Traditionally, a LO is built using a frequency synthesizer. When designing a frequency synthesizer, several requirements have to be carefully respected which are mainly the output frequency and the phase noise. Table I provides the expected specifications of several standards [4] in the targeted band. As one can notice, specifications depend on the standard and are different one from the others. So, to act at multi-standard, it becomes necessary that the LO output frequency range achieves a 3GHz bandwidth. To respect the phase noise requirements, it should agree with the mask defined by the lowest phase noise that is to say -110dBc/Hz at 200kHz and -129dBc/Hz at 5MHz. Finally, it may provide two outputs in quadrature phase in order to be zero-IF architecture compliant.

Usually, frequency synthesizers are built around Phase Locked Loop (PLL). Unfortunately, this last architecture offers such a large output frequency range only at the price of very poor close-in phase noise. Recently, a new architecture has shown its ability to fulfill multi-standard LO requirements: the Factorial Delay Locked Loop (F-DLL) [5].

Table I. Specifications for local oscillators.

	MOBILE PHONE				*WIRELESS PHONE*
Standard	**GSM**	**DCS 1800**	**PCS 1900**	**UMTS**	**DECT**
Frequency band (MHz)	Rx: 925-960 Tx: 880-915	Rx: 1805-1880 Tx: 1710-1785	Rx: 1930-1990 Tx: 1850-1910	Rx: 2110-2170 Tx: 1920-1980	1880-1897
Channel width	200 kHz	200 kHz	200 kHz	5 MHz	1.7 MHz
Phase noise	-110 dBC/Hz @ 200 kHz	-110 dBC/Hz @ 200 kHz	-110 dBC/Hz @ 200 kHz	- 129dBc/Hz @5MHz	-92dBC/Hz @1.7MHz

	STANDARD DATA SPECIFICATIONS		
Standard	**802.11 b**	**802.11 g**	**Bluetooth**
Frequency band (MHz)	2410-2426 (USA) 2412-2472 (Europe) 2471-2497 (Japan)	2410-2426 (USA) 2412-2472 (Europe) 2471-2497 (Japan)	2402-2480 (USA & Europe) 2473-2495 (Japan)
Channel width	FHSS : 1MHz DSSS : 25MHz	20 MHz	1 MHz
Phase noise	-101dBC/Hz @1MHz	-102dBC/Hz @20 MHz	-129dBC/Hz @20 MHz

Indeed, the F-DLL offers the reconfigurability of the PLL topology and the very good phase noise performances near to the carrier frequency of the DLL architecture [6]. This article emphasizes on the main block of the retained LO architecture: the Voltage Controlled Delay Line (VCDL). Indeed, it ensures, among others, the overall phase noise performances and the output frequency range. However, previous published wideband reprogrammable DLL [7] [8] [9] do not take into account the output quadrature phase requirement of zero-IF architecture. This paper presents an original one which, while maintaining F-DLL phase noise and output frequency range, ameliorates its output quadrature phase performance. In a first part, a comparison of the two main frequency synthesizer architectures for multi-standard application is realized. Then, the F-DLL with its original phase noise performance is described. Thereafter, a previously published wideband VCDL design and the original proposed architecture are presented. Finally, measurement results of the F-DLL designed with the proposed and previously published VCDL realized in 130nm CMOS SOI STMicroelectronics technology are depicted. Experimental results confirm the F-DLL properties (wide frequency band and phase noise) and the low phase quadrature error of the VCDL outputs signal.

2. RF SYNTHESIZER ARCHITECTURES COMPARISON FOR MULTI-STANDARD APPLICATIONS

Traditionally, LO are built around frequency synthesizers. These lasts are usually Phase Locked Loop (PLL) based. A classical charge-pump PLL is composed by of a phase-frequency detector, a loop filter, a charge pump, a voltage controlled oscillator (VCO) and a frequency divider [10], as shown on fig.1a.

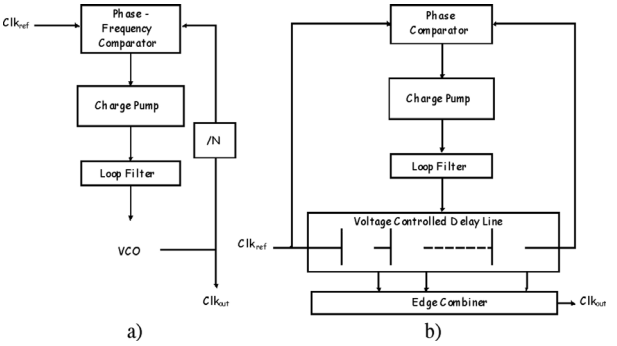

Figure 1. PLL and DLL architecture.

The high frequency signal is generated by the VCO whose phase is controlled by the rest of the loop. Several other topologies of PLL exist like fractional one [11] which main goal is to increase the frequency bandwidth so as to decrease the in-band phase noise. To reach the previously defined requirements in term of frequency output range, it is necessary that the VCO synthesize all the standards of the [0.9-4] GHz band. Two solutions exist to fulfill this requirement. On one hand, the VCO frequency band could be formed by several bands corresponding to each targeted standard. This could be realized by using, for example, switched capacitors in the LC tank.

On the other hand, the VCO frequency range could synthesize directly all the frequencies of the [0.9-4] GHz band. The second solution is better according to a reconfigurable point of view as the VCO could synthesize not only the existing norms but all of the possible future standards within this band. But, the only VCO which offers such a so huge output frequency range is based on ring oscillator topologies [9]. Unfortunately, they could not reach the required phase noise performances. In the ninety's, a new architecture has been brought into play to realize the frequency synthesis: the Delay Locked Loop [10]. It is composed by a phase detector, a loop filter, a charge pump, an edge combiner and the VCO is substituted by a Voltage Controlled Delay Line (VCDL) as it is depicted in fig.1b. The system is locked when the delay in the VCDL is one period of the incoming signal. Then, the output of each delay element is combined to synthesize the high frequency signal. Since each new rising edge of the reference signal triggers a new cycle, the timing random jitter generated by each delay element is cumulated only during one delay line, which offers to the DLL very good phase noise performances near the carrier frequency. This phase noise particularity could make it compliant with the required phase noise performances. Moreover, the VCDL could be built around large timing output range delay elements [11] which make DLL a good candidate for the 3GHz frequency output range. The only negative point is the reconfigurabilty of the architecture as the edge combiner is only

used for one output frequency. But this drawback can be solved by an original architecture which combines the reconfigurability of the PLL and the phase noise performance of the DLL: the Factorial DLL.

3.FACTORIAL DLL AND ITS ORIGINAL PHASE NOISE PERFORMANCE

A. Overview of the Factorial DLL

Figure 2 illustrates the Factorial DLL topology for a multi-standard frequency synthesizer approach [12]. It is made up of three main blocks. First, an *Oscillator* block creates the high frequency signal. Since, the counter is a programmable one, it makes the system to be able to meet the requirements in term of reconfigurability.

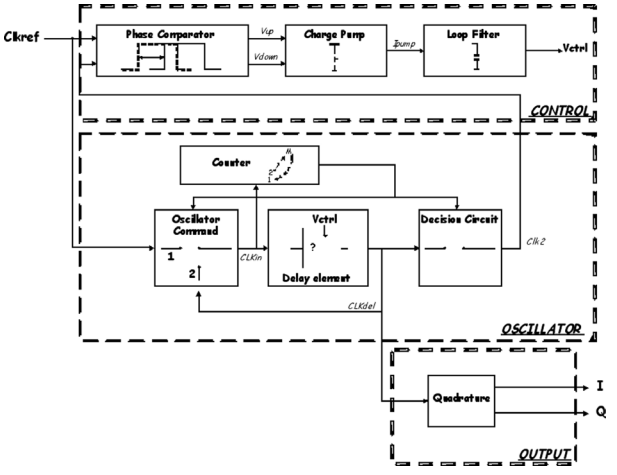

Figure 2. Factorial DLL topology.

Then, a *Control* block ensures the phase control of this synthesized signal. The last block, *Output*, ensures the quadrature phase of the output signal, by dividing-by-2 the synthesized signal. In other terms, this solution forces the *Oscillator* block to work at a frequency two times greater than expected one.

The operation of the F-DLL is as follow. At the beginning, *Oscillator Command* switch is turned on position 1. The rising edge of *CLKref* starts the system. It goes through the *Oscillator Command* and forces it on position 2. Then, this signal is delayed by the *Delay Element* and inversed on its returned path through the *Oscillator Command*. The oscillation is started. Each new synthesized period is counted by the programmable *Counter*. The oscillation goes on until the programmed value of the counter is reached. At this moment, the counter closed, on one hand, the *Decision Circuit* switch. It allows the last falling edge of *CLKdel* to be compared with the next rising edge of the reference signal by the *Control Block*. On the other hand, the *Oscillator Command* is turned on position 1. The oscillation is stopped. The next rising edge of the reference clock will trigger a new oscillation.

B. Phase noise study

To determine the phase noise of the system, it is first important to understand the operation of the F-DLL. Indeed, during one period of the reference clock, the "active" oscillator (*Oscillator Command* + *Delay Element*) could be seen as a ring oscillator. But as each new reference signal period triggers a new oscillation, the random timing jitter is return to zero periodically. Assuming that the phase noise of the system is mainly due to the oscillator noise, the F-DLL output phase noise is dominated by two phenomena: the free running ring oscillator jitter accumulation and the DLL cycling cancelling noise.

1) Jitter behavior of the factorial DLL

In [12], the study of accumulating jitter in a free running ring oscillator has been done. It demonstrates that a perturbation in the phase, during one period of oscillation, changes the starting point of the next one. For independent Gaussian errors, the cycle to cycle jitter variance (s^2_{VCO}) of the oscillator timing error adds themselves and the total error variance (s^2_{tot}), which is the total error variance with respect to an ideal time base, grows linearly as in fig.3a.

In conventional PLL, this variance accumulation reaches an equilibrium value at a time which is inversely proportional to the loop bandwidth (ω_{pll}) as shown on the fig.3b.

In a F-DLL, during one period of the reference, the oscillator acts as a free running one. So, the cycle to cycle jitter variance (σ_{VCDL}) adds from one cycle on the other one. But, as each new cycle of the reference triggers a new oscillation, this accumulation adds no more than one period of the reference and it

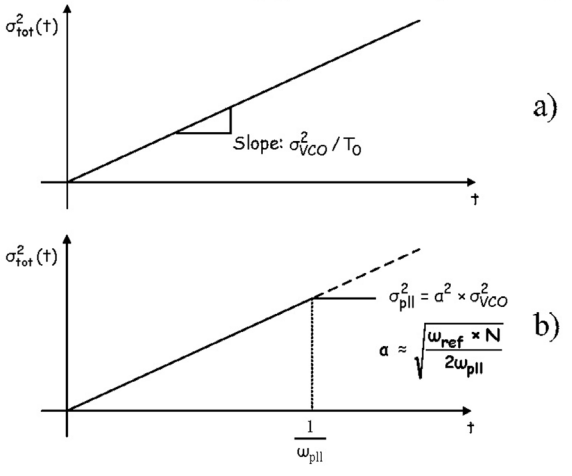

Figure 3. Jitter accumulation in a free running VCO and for VCO in the PLL.

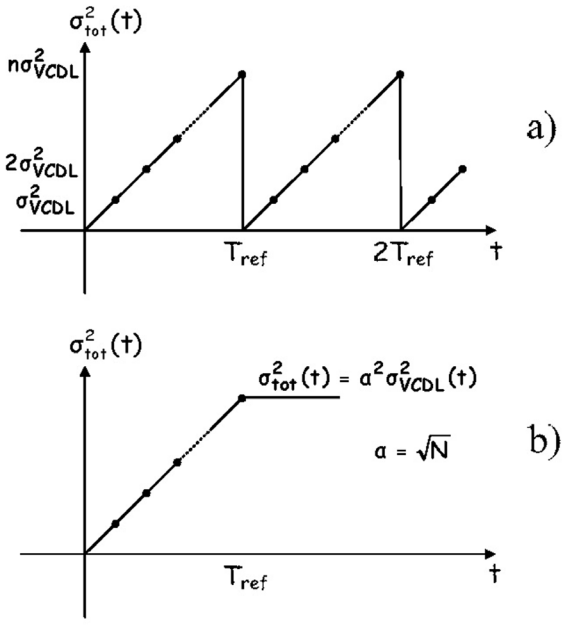

Figure 4. Jitter accumulation in a Factorial DLL.

is cancelled periodically with the reference signal. So, the jitter accumulation in the F-DLL can be drawn like in fig.4a. The total accumulated jitter is N times greater than the cycle to cycle jitter of the oscillator, where N is the multiplication factor of the loop. Figure 4b shows the accumulated jitter of the F-DLL output in the same way of fig.3b. As the reference frequency is greater than the classical PLL loop bandwidth (in the order of 10 to 100), the total variance of the F-DLL is smaller than those generated in a PLL in the same configuration.

2) Phase noise response of the Factorial DLL

For white noise, knowing the accumulating process of the F-DLL, we can deduce its phase noise thanks to equation [14]:

$$S\phi(f)=(f_0/f_{m^2})*(\sigma_{vco}/To)^2 \quad (1)$$

This equation stands that the phase noise grows linearly, with a slope inversely proportional to f_{m^2}, when the offset frequency decreases. In our application, the cycle to cycle jitter is no more accumulated than one period of the reference. So, the phase noise will not increase for an offset frequency inferior to the reference frequency.

Figure 5 presents the simulated phase noise of the free running ring oscillator. As one can notice, the free running phase noise performances never respect the requirements defined previously (continuous line). But, when this oscillator is into a F-DLL, the maximum phase noise is calculated at the reference frequency. Thus, if we choose a reference frequency high enough, the maximum phase noise will be equal

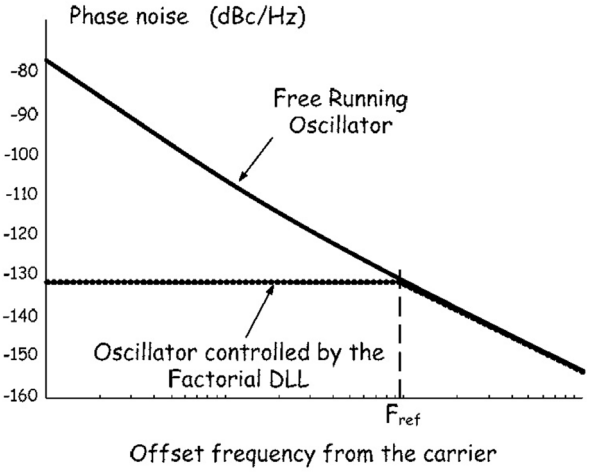

Figure 5. Simulated phase noise.

to -130dBc/Hz (dashed line), and all the phase noise requirements will be fulfilled. So thanks to the F-DLL, a poor close in phase noise circuit can be turned into a compliant multi-standard oscillator.

4. ENHANCEMENT OF THE VCDL

A. Pseudo-NMOS VCDL

Most of traditional VCDL architectures are based on logic gates (CMOS or CML). The gate delay is adjusted by controlling the gate current. Figure 6a presents the F-DLL "active" oscillator used in [11]: the *VCDL* and a part of the *Oscillator Command* block. When the delay line output is connected to one of the NOR input (the other is set to zero) the oscillation could start. Because of the topology chosen to perform the output phase quadrature (frequency division by two), the oscillator has to synthesize the [1.8-8] GHz band. Therefore, the VCDL must have a wide delay range. This is done using a pseudo-NMOS inverter. Indeed, in classical CMOS inverters the PMOS slows down the circuit speed. By using it as a variable resistor, it is possible to synthesize high frequency while maintaining the low frequency synthesized ability of traditional CMOS inverter based voltage controlled delay element (VCDE). As far as the author's knowledge is concerned, it is the only way to realize such a wide continuous frequency range. Figure 6b presents the simulated frequency as a function of the voltage controlled. This last has been performed using 130nm CMOS technology from STMicroelectronics and Cadence Spectre RF tools. One can notice that the frequency range is slightly greater than 1.8 to 8GHz. By dividing this frequency by two, using two paths in phase opposition, two signals in quadrature phase of the 0.9 to 4GHz band could be synthesized. However, this technique has two main drawbacks. On one hand, it forces the oscillator to work at

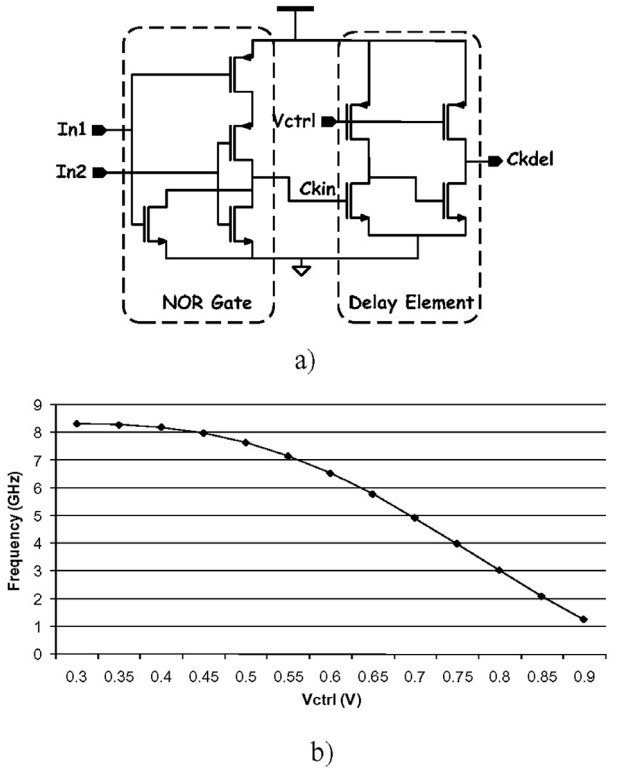

Figure 6. VCDL and its simulated oscillation frequency in oscillator mode.

a frequency higher than needed. Hence, this increases the power consumption of the oscillator. On the other hand, the phase quadrature error is dependent on the input signal duty cycle, which has to be equal to 50 % [10]. However, the delay controlled of the VCDE is only done on one transition of the input, more precisely when the input gate is set to low level. Indeed, with this topology, the adjustable delay is obtained by playing on the discharge of output gate RC constant, where C is the output parasitic capacitances and R the variable PMOS resistor. So, output rising edge will be different from output falling edge which implies a duty cycle different from 50% in particular for low frequency. To limit this effect, an even number of voltage controlled NMOS inverter has been used in fig.6a in order to balance the structure.

Fig.7 presents the simulated quadrature phase error of the output signal and input signal duty cycle according to F-DLL output frequency. Note that the quadrature phase error decreases as the duty cycle approaches 50%. Moreover, as the frequency decreases the phase quadrature error increases. Unfortunately, in order to have acceptable performances of image rejection ratio of the zero-IF topology, it is necessary to have a phase quadrature error lower than 5° [14]. Clearly, this performance needs to be enhanced to allow the F-DLL to be multi-standard zero-IF LO compliant. The ideal solution should be to divide by four the signal to ensure the exact quadrature phase but it is not suitable to synthesize the huge band [3.6-16] GHz.

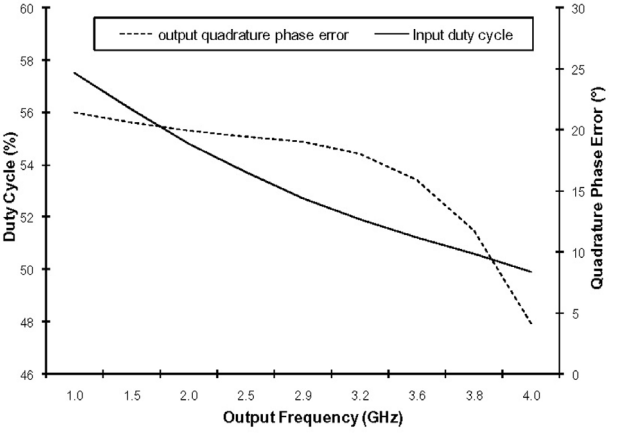

Figure 7. Output phase quadrature error dependances on input duty cycle.

B. Proposed VCDL

The proposed idea lays on the fact that during one period of the reference, the F-DLL oscillator could be seen as a ring oscillator. So, the idea is to take advantages of multiphase ability of ring oscillator to perform the expected output phase quadrature.

1) *Multiphase ring oscillator [15]*

Fig.8 shows the general topology of multiphase ring oscillators with subfeedback loops. The fundamental idea is to use the interpolating inverters (S_N) to compose N intercoupled subfeedback loops. The phase relationship between inverter stages remains unchanged due to the symmetrical structure.

We define *i* as the feedback index. It is an integer ($2 \leq i < N$) representing the number of inverter stages in each subfeedback loop.

The interpolating S_n can be incorporated into the major loop inverter M_n circuitry with a separate input. The topology of fig.8 can be redrawn in fig.9 where the interpolating inverters are used to implement the fast paths (short cuts). We define *x* as the feed-forward index in contrast to the feedback index *i*. It is an integer ($2 \leq x < N$) representing the number

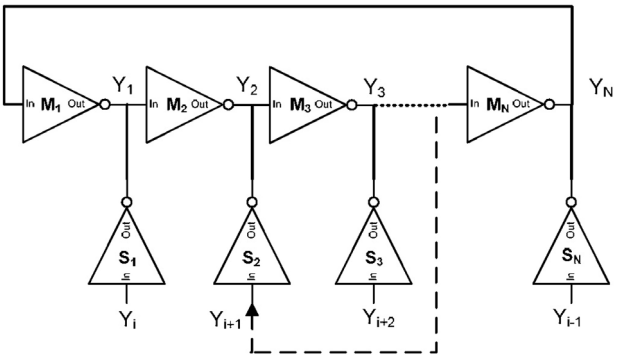

Figure 8. General topology of ring oscillator with subfeedback loops from [15].

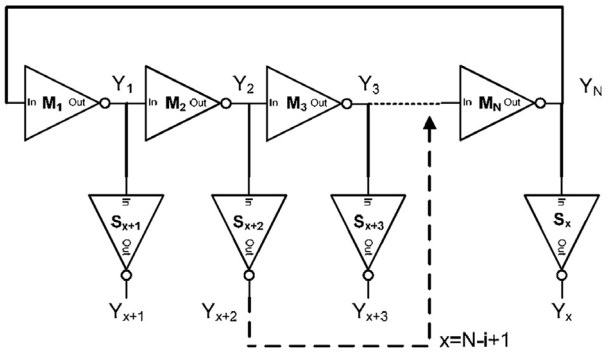

Figure 9. Demonstration of feedforward paths from [15].

of major loop inverters M_n that the interpolating inverters S_n pass over. The topologies of fig.8 and fig.9 are equivalent. The relationship between *i* and *x* is *x=N-i+1*.

2) Proposed VCDL

The proposed topology is based on a four stage single ended ring oscillator (M_n=4) because of the two phases (0° and 90°) are only needed. Figure 10 presents the VCDL architecture. The multiphase ring oscillator is right in the middle (*Oscillator Block*). Four inverters are interpolated to compose the subfeedback loop. With feedback index *i=3*, each subfeedback loop contains three inverters (A-A'-D; A-B-B'; B-C-C'; C-D-D') and producess the fast loop. The main feedback loop with four stages (A-B-C-D) is the slow loop.

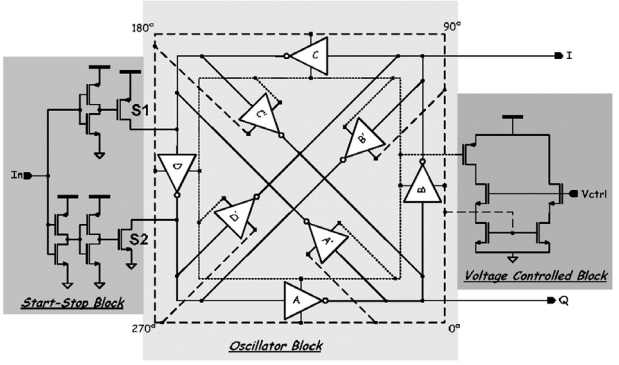

Figure 10. Proposed VCDL.

Each inverter is based on the topology depicted in fig.11. It is composed by a CMOS inverter (M1-M2) compressed between an upper PMOS (Mp) and a bottom NMOS (Mn) which control the current going through the inverter to ensure the delay variability of the cell. The circuit on the right part of fig.10 (*Voltage Controlled Block*) controls the voltage *V+* and *V-* of fig.11 through the controlled voltage provided by the *Control* block of fig.2. To ensure the stop and the restart of the oscillation, which acts as a VCDL, the circuit on the left part has been added (*Start-Stop Block)*. It consists in two switches (S1-S2) between *180°* node and *VDD*, and *270°* node and *GND*. Then, when *In* is

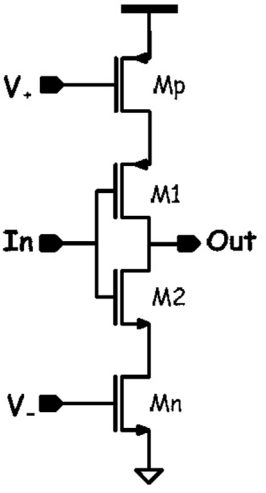

Figure 11. Voltage Controlled Delay Element scheme.

at high level, node *270°* and *180°* are respectively forced to low and high level so the oscillation is stopped. Otherwise, when a new reference rising edge happens, the *Oscillator Command* set *In* to low level. If the inverters and the two switches are well dimensioned, the capacitive coupling through V_{DS} of S1 and S2 creates a voltage spike which starts the new oscillation if there is gain enough on the ring oscillator. Futher, those two switches are also necessary to control the starting state of the nodes. Indeed, controlling the starting state allows the circuit to work as if this new edge propagates itself through the VCDL like in classical VCDL previously presented. This oscillator has been also simulated using 130nm CMOS technology from STMicroelectronics. Fig.12 presents the phase quadrature error according to output frequency. As one can notice on the X-coordinate, the expected frequency range [0.9-4] GHz is performed. Moreover, the phase quadrature is less than 5° which makes at this point the F-DLL a zero-IF LO compliant architecture. To conclude, this technique offers two main advantages compared to the previous ones.

First, the quadrature phase error is independent on the duty cycle of the signal and the phase error is lower than 5°. Then, as the VCDL provides the two quadrature phase signal working at twice the expected frequency is no longer mandatory, hence it will decreased by a factor 2 the power consumed by the VCDL.

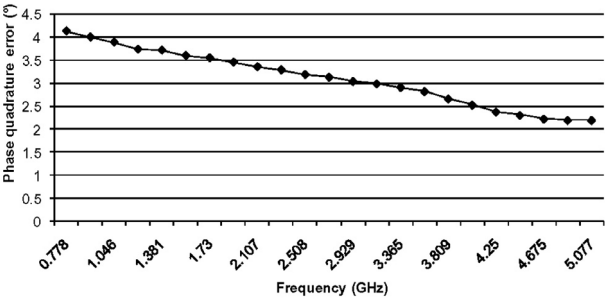

Figure 12. Simulated phase quadrature error of proposed VCDL.

5. MEASUREMENT RESULTS

Those two circuits have been fabricated using a 130nm CMOS SOI technology from STMicroelectronics. Fig.13 presents the microphotograph of the F-DLL where the proposed VCDL is implemented. It measures 2mm by 2mm including all the pads. However, effective chip area is 0.35mm². The high number of pads using by the chip is meanly due to the programmable counter and voltage supplies.

A. Factorial DLL measurement results

1) Output spectrum

Figure 14 presents the output signal spectrum of the F-DLL based on our proposed VCDL for different standards. A 100MHz, -6dBm, input reference signal has been used as it represents the higher common multiple of the targeted norms. In the measurement setup, a 10dB attenuator has been put in before the Agilent 8563E spectrum analyser input. So output signal power is between -5.5dBm up to -2.5dBm depending of the standards.

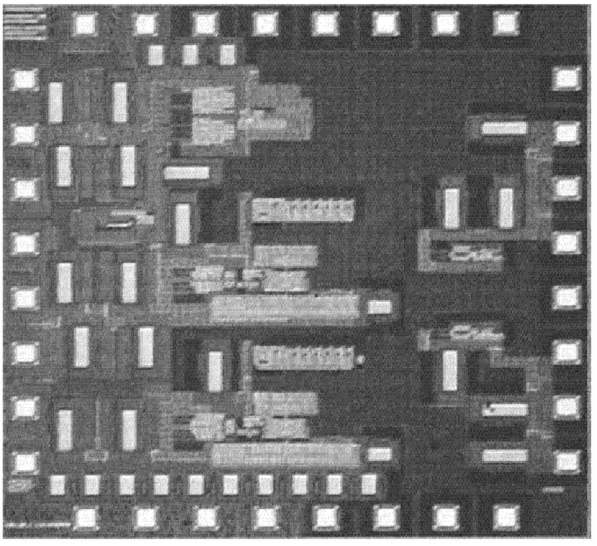

Figure 13. Chip microphotograph of the F-DLL designed with our proposed VCDL.

Figure 15 presents the measurement result of the output frequency versus the controlled voltage for the two VCDL. This result differs from simulated one of fig.7. Indeed the simulation has been performed using a 130 nm CMOS BULK technology while the realization has been done in SOI. In fact, this project has been funding within the MEDEA+ T206 SOI-LP/RF project whose aim was the development of 130nm SOI technology. So, both design kit and parasitic extraction tools were not available. Nevertheless, the expected functionality will be confirmed. As one can notice, the 0.9 to 4 GHz band has been reached. for our proposed VCDL. In contrast, the NMOS VCDL band is limited to 5.8GHz. So only a [0.9-2.9] GHz band is available with output phase quadrature.

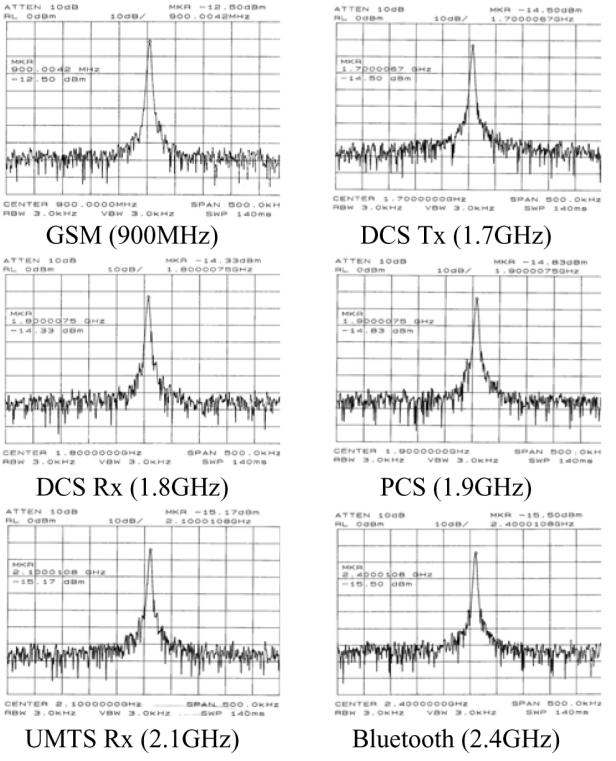

Figure 14. Output frequency F-DLL spectrum for several standrads.

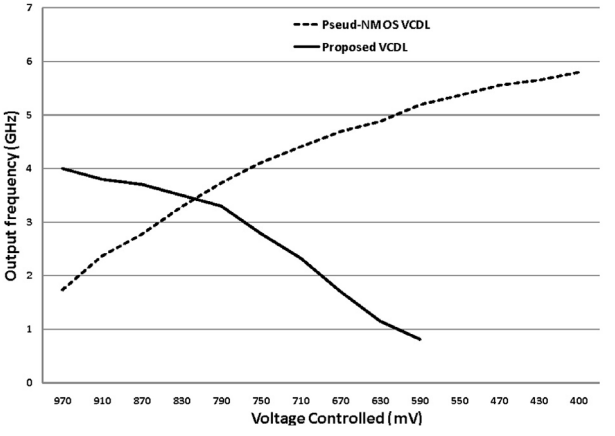

Figure 15. Output frequency versus controlled voltage for the two VCDL.

2) Phase noise measurements

Figure 15 presents the phase noise measurements of the F-DLL outputs for two standards (GSM and Bluetooth). For each graph, the lowest curve is the phase noise response of the 100MHz reference. The upper one is the F-DLL output signal phase noise. For the two graphs, the F-DLL output phase noise follows the reference phase noise, with a factor of 20log(N) where N is the multiplication factor during all the offset frequency from 1kHz up to

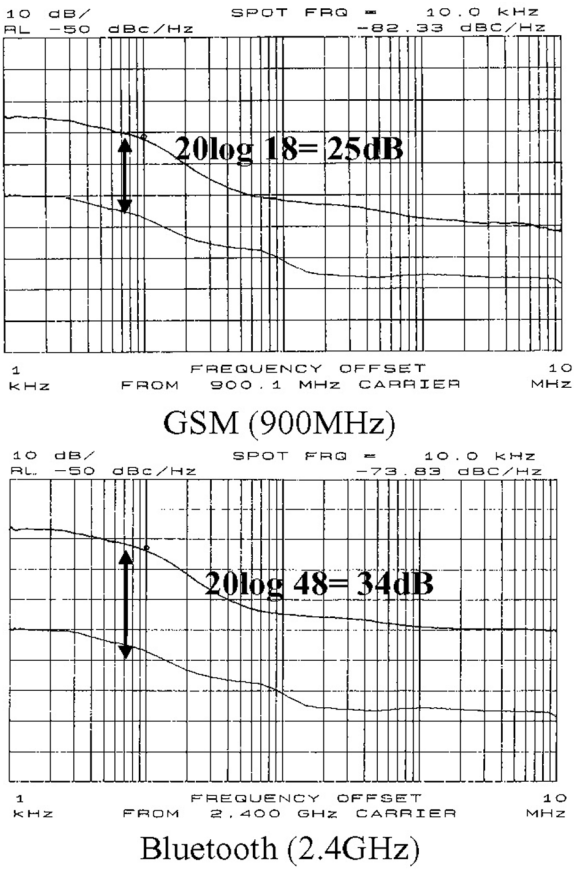

Figure 16. F-DLL phase noise measurements.

10MHz. These results confirm the F-DLL theory presented in section 3. This theory stands that for offset lower than the reference (here 100MHz) the F-DLL oscillator, which the main noise contributor of the system, does not accumulate jitter anymore. Consequently, at the output, we obtain only the input reference noise multiplied by N.

3) Settling time analysis

When designing a multi-standard LO, another point is of interest: the speediness of the loop and particularly its ability to switch quickly from one channel onto another in a same standard and also from one standard to another one for a multi-standard application point of view. F-DLL is like classical DLL a first order system which offers quick settling time. Figure 17 illustrates the oscillator controlled voltage evolution according to the time, realized with a Lecroy wavepro 960 oscilloscope, for a frequency hopping from 0.9GHz up to 2.5GHz. Controlled voltage of the oscillator is an image of the output frequency evolution. X-axis scale is 0.5µs by division whereas Y-axis scale is 50mV by division. It takes 1.5µs to switch from one standard onto the other which confirm the speediness of the loop. Furthermore, there is neither overshot nor oscillation in the response. Such an observation seems to confirm that the loop is stable in accordance with the theory which stands that DLL is a 1st order system.

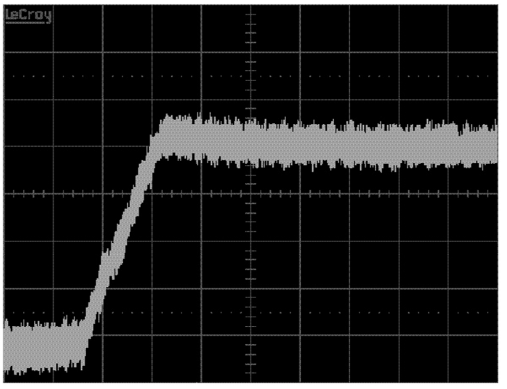

Figure 17. Controlled voltage response to a frequency hopping between 0.9MHz and 2.5GHz.

4) *Architecture limitation*

For LO, spectral purity is important. This is quantified thanks to spurious tones rejection. For this design, mainly due to the lack of transistor model and parasitic extraction tools, F-DLL exhibits poor spurious tones rejection. The worse one is obtained at an offset equal to the reference frequency and it is about -20dB. This is mainly due to static phase error produced at the phase comparator and charge pump stages. Indeed, mismatches exist between the two inputs of these blocks which are the reference signal and the oscillator block output. Retro-simulation has shown that a static phase error of 10% creates a minimum spurious tones rejection of -18dB. Nevertheless, a new design of this block will enhance the overall performances by lessening the spurious tones.

B. Quadrature phase performances enhancement

Figure 18 presents the measured output waveform for the NMOS VCDL (a) and our proposed one (b). The two outputs in phase quadrature are depicted only for the existing standards that the two VCDL can reach. The last waveform is the highest frequency achievable for each VCDL which confirms the VCDL ability to synthesize, on one hand, the [0.9-4] GHz band , and on the hand, the [1.8-5.8] GHz band.

Figure 19 presents the measured phase quadrature error according to the same standard as presented in the last figure. These results confirm the trend that the NMOS VCDL has poor phase quadrature performance, particularly for low frequency. In fact, the results are worse than expected. But, these measurement results confirm the fact that our proposed solution could make F-DLL a zero-IF LO multi-standard architecture. Indeed, measured phase quadrature errors are lower than 5°.

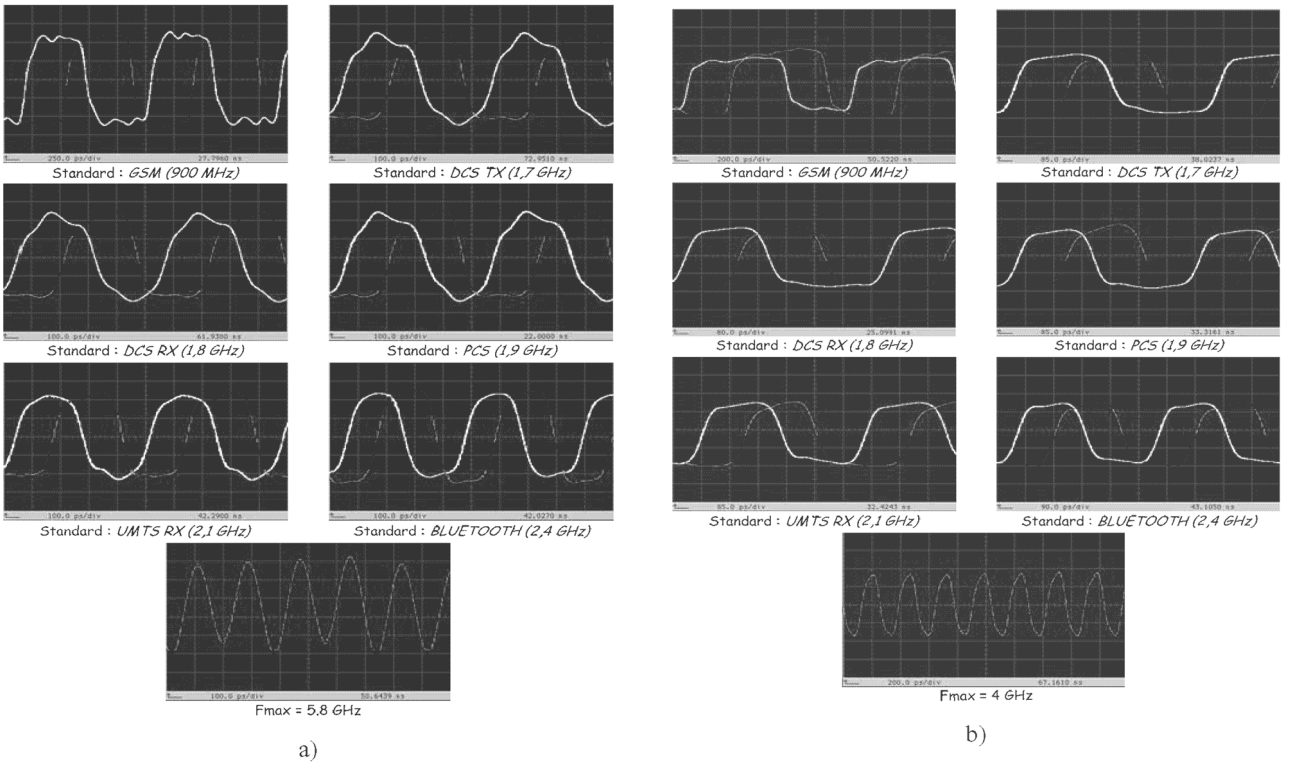

Figure 18. Ouput waveform (**a:** NMOS VCDL; **b:** Proposed VCDL).

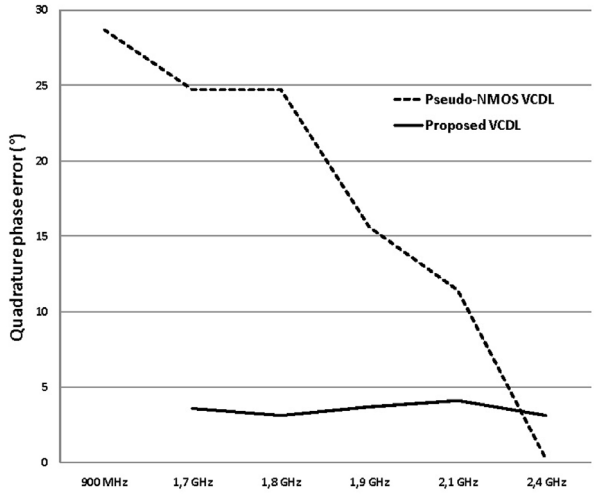

Figure 19. Phase quadrature error of the two VCDL.

6. CONCLUSIONS

This paper has presented the study and the measurement results of an original VCDL dedicated to Factorial Delay Locked Loop (F-DLL) for multi-standard local oscillator applications. F-DLL architecture has been presented. It offers the reconfigurability of the PLL topology thanks to its programmable counter and the phase noise performances of the DLL as each new cycle triggers a new oscillation. The main drawback of the pseudo-NMOS voltage controlled delay line which consists in too important quadrature phase output error is corrected by our proposed topology. Measurements confirm the low quadrature phase error of the topology always inferior to 5°. Further, they demonstrate the architecture ability to synthesize the [0.9-4] GHz targeted band while offering interesting performances in term of phase noise and settling time. So, this proposed circuit allows the F-DLL to be zero-IF compliant and so a good candidate for multi-standard LO.

ACKNOWLEDGEMENTS

Authors express their thanks to the French Government and the European Community for funding the research within the MEDEA+ T206 SOI-LP/RF project and STMicroelectronics for processing the prototype

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