Application of the Symmetric Doped Double-Gate Model in Circuit Simulation Containing Double-Gate Graded-Channel Transistors

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ABSTRACT

The development of models to simulate circuits containing new devices is an important task to allow the introduction of these devices in practical applications. In this paper we show the advantages of using the recently developed Symmetric Doped Double-Gate Model as already introduced in SmartSpice simulator, for modeling circuits containing Double-Gate Graded-Channel (GC) transistors. In this case there is no need to use two different models to represent the graded-channel device, as has been done up to now. Current-mirror circuits using GC devices have been simulated and the results were validated comparing them with those obtained using the MIXED-MODE module of two-dimensional numerical ATLAS simulator of the GC devices.

Index Terms: Double-Gate Graded-Channel Transistor, Symmetric Doped Double-Gate Model, SmartSpice simulator, 2D ATLAS simulation.

1. INTRODUCTION

In recent years, the use of graded-channel (GC) transistors in analog circuits has proven to be an interesting approach due to the advantages presented by these devices such as reduced drain output conductance, increased transconductance and high Early voltage. These are key characteristics for designers interested in improving the performance of analog integrated circuits [1]. In this device a region of length L_{LD} is kept with the natural wafer doping concentration, while the threshold voltage (V_T) implantation is performed at the source side only. The lightly doped (or undoped) region presents negative threshold voltage and acts as an extension of the drain region under the gate, reducing the effective channel length (L_{eff}=L–L_{LD}, L being the mask channel length). Figure 1 illustrates the GC DG MOSFET.

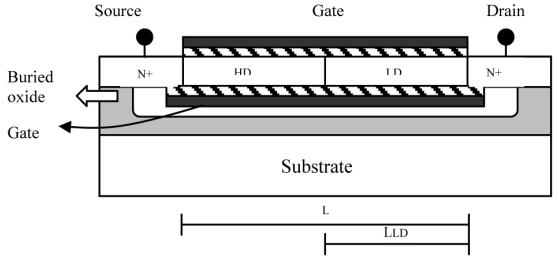

Figure 1. Double-Gate Graded-Channel structure.

Successful implementation of Graded-Channel double-gate devices has been achieved using Gate-All-Around (GAA) structures, resulting in extremely improved analog performance, mainly an appreciable reduction of the drain output conductance leading to improved Early voltage (≈1600V) and intrinsic voltage gain (> 75 dB) for 3 μm long devices [2].

For circuit simulation a main task is to count with a precise transistor model to reproduce the transistor behavior, which is either already introduced or can be implemented in the commercial circuit simulators to be used.

Recently, modeling of DG GC transistors has been proposed using two different models to represent each transistor: one for the doped region and the other for the undoped one [3] as presented in the equivalent circuit of Figure 2.

In this paper we show that for modeling purposes, DG GC transistors can be represented as the connection of two transistors in series in the SmartSPICE circuit simulator [4], Using this approach both channel regions can be simulated using only one model, the Symmetric Doped Double-Gate Model (SDDGM) [5-6].

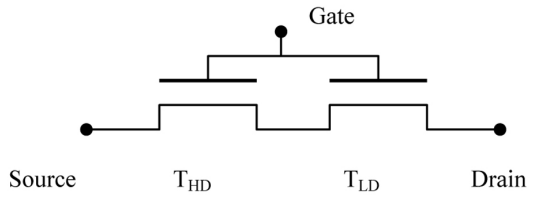

Figure 2. Equivalent representation of Graded-Channel structure: series association of two DG SOI transistors: high doped, T_{HD}, and natural doped or lightly doped, T_{LD}.

The new compact analytical SDDGM considers variable mobility and short-channel effects. This model has been successfully implemented in Verilog-A and introduced in SmartSPICE [7] in the way to consume less resources as memory and increase the simulation speed.

To illustrate this implementation, current-mirror circuits having the architectures known as Common Source and Wilson were selected [7]. Validation of the applicability of this model for GC transistors was done comparing results of circuit simulations performed using SmartSPICE with the SDDGM model with those obtained in MIXED-MODE and 2D ATLAS numerical simulation of the GC devices, including the lightly doped (LD) and high doped (HD) transistors parts.

2. GC TRANSISTOR MODELING

A brief description of the SDDGM model will be introduced. The SDDGM calculates the transcendental equation for the surface potential using the expression derived for the difference between the surface potential and the potential at the center of the silicon layer [5] and the Lambert Function. This analytical surface potential calculation gives the possibility of normalizing charge carrier calculation at source, q_s, and at the drain, q_d. The drain current for long channel transistors is calculated using the following equation [6]:

$$I_D = 2\frac{W}{L}\mu C_{ox}\phi t^2\left[\frac{q_s^{\,2}-q_d^{\,2}}{2}+2(q_s-q_d)-q_b\ln\left(\frac{q_s+q_b}{q_d+q_b}\right)\right] \quad (1)$$

where W is the channel width; C_{ox} is the gate capacitance per unit of area, $\phi t=kT/q$ (k being the Boltzmann constant, T the absolute temperature and q the electron charge); $q_b=qNat_s/C_{ox}\phi t$ is the normalized fixed charge concentration in the silicon layer of thickness t_s and surface mobility is defined by:

$$\mu_S = \frac{\mu o}{1+\left(\frac{\overline{E}}{E_1}\right)^{P_1}+\left(\frac{\overline{E}}{E_2}\right)^{P_2}} \quad (2)$$

where μo is the maximum mobility; $\overline{E}$ is the medium electric field at the surface, E1 is the critical field for ion scattering, is the critical field for $E_2 = E20\,(1+ E2V.V_{def})$ scattering at the surface roughness, and P1 and P2 are the corresponding exponents.

The effects of saturation velocity, v_{sat}, on mobility, on drain charge at saturation, q_{sat}, on saturation voltage, V_{sat}, and V_{Def} are considered by:

$$\mu = \frac{\mu_S}{\sqrt{1+\left(\frac{\mu_S V_{Def}}{v_{sat}L}\right)^2}} \quad (3)$$

$$q_{sat} = -\left(\frac{v_{sat}L}{\mu\phi t}+2\right)+\sqrt{\left(\frac{v_{sat}L}{\mu\phi t}+2\right)^2+q_s^2+4q_s}\ , \quad (4)$$

$$V_{sat} = \tau\cdot\phi t\cdot\left[q_s-q_{sat}+2\ln\left(\frac{q_s+q_b/2}{q_{sat}+q_b/2}\right)\right]. \quad (5)$$

$$V_{Def} = V_{sat}+\frac{1}{2}\cdot\left[V_d-V_{sat}+\frac{\phi t}{3}-\sqrt{\left(V_d-V_{sat}+\frac{\phi t}{3}\right)^2+4\frac{\phi t}{3}V_{sat}}\right] \quad (6)$$

Table I. Technological and modeling parameters.

GC length L [μm]	L_{LD}/L ratio	Transistor	L_{ind} [μm]	Na [cm^{-3}]	E1 [V/cm]	E20 [V/cm]	E2V [V^{-1}]	P1	P2	τ	λ
2	0.2	HD	1.6	10^{17}	4.71×10^4	1.09×10^6	0.042	0.32	1.5	0.9	1
		LD	0.4	10^{15}	5.71×10^4	1.01×10^6	0.125	0.32	1.49	0.77	30
	0.3	HD	1.4	10^{17}	4.81×10^4	1.08×10^6	0.04	0.33	1.5	0.9	1
		LD	0.6	10^{15}	5.4×10^4	1.04×10^6	0.115	0.31	1.5	0.83	24
	0.5	HD	1	10^{17}	5.11×10^4	1.09×10^6	0.036	0.34	1.5	0.89	15
		LD	1	10^{15}	5.21×10^4	1.06×10^6	0.05	0.31	1.51	0.87	15
GC length L [μm]	L_{LD}/L ratio	Transistor	L_{ind} [μm]	Na [cm^{-3}]	E1 [V/cm]	E20 [V/cm]	E2V [V^{-1}]	P1	P2	τ	λ
1	0.2	HD	0.8	10^{17}	5.35×10^4	1.09×10^6	0.1	0.34	1.5	0.88	25
		LD	0.2	10^{15}	6.59×10^4	9.70×10^5	0.28	0.35	1.48	0.86	35
	0.3	HD	0.7	10^{17}	5.60×10^4	1.08×10^6	0.1	0.35	1.5	0.93	25
		LD	0.3	10^{15}	6.03×10^4	1.01×10^6	0.22	0.33	1.49	0.86	20
	0.5	HD	0.5	10^{17}	6.22×10^4	1.09×10^6	0.13	0.37	1.5	0.91	20
		LD	0.5	10^{15}	5.58×10^4	1.03×10^6	0.13	0.32	1.49	0.9	20

Mobility parameters μ0, E1, E20, E2V, P1 and P2 are extracted from the transfer characteristics in the linear and in the saturation regions. Parameters τ and λ are extracted from the transfer characteristic in saturation and from the output characteristic.

Uniformly doped transistors T_{LD} and T_{HD} were numerically simulated in ATLAS individually covering the different combinations of L_{LD}/L ratios for the different channel lengths of the GC transistors. Using these individual devices the set of extracted model parameters are shown in Table I including the individual channel length L_{ind} and doping concentration N_a in each active silicon layer.

The technological parameters are: channel width, W = 1 μm; equivalent gate oxide thickness, t_{ox}= 2 nm; silicon layer thickness, t_{Si}= 50 nm and n-type polysilicon gate thickness, t_{poly}= 100 nm.

Figure 3 shows the output conductance (g_d) as a function of V_D of both individual uniformly doped transistors that conform the GC device with L=2μm and L_{LD}/L=0.3 at a gate voltage (V_G) of 1 V. As can be seen, a very good agreement is achieved between the simulated characteristic obtained from ATLAS and those obtained by circuit simulation, with a maximum error of 10% at individual points.

Figure 4 shows the simulated and modeled drain current (I_D) and transconductance (g_m) as a function of the gate voltage for the GC transistor with L=2 μm, with HD region of 1.4 μm and LD region of 0.6 μm (L_{LD}/L=0.3) at a drain bias V_D= 50 mV.

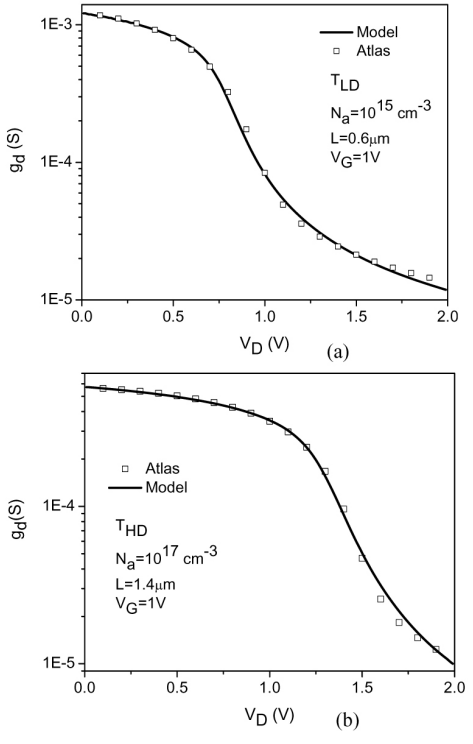

Figure 3. Simulated and modeled output conductance at V_G= 1V for both individual transistors.

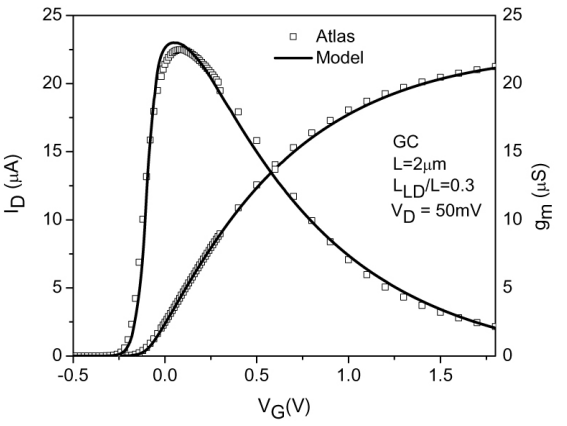

Figure 4. Transfer characteristics and transconductance, g_m, as a function of the gate voltage for the GC transistor with L = 2μm, W = 1μm, L_{LD}/L = 0.3 at V_D = 50mV.

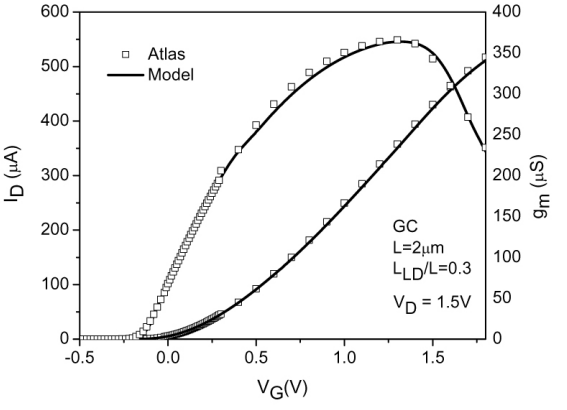

Figure 5. Transfer characteristics and transconductance, g_m, as a function of the gate voltage for the GC transistor with L = 2μm, W = 1μm, L_{LD}/L = 0.3 at V_D = 1.5V

In figure 5 we have the simulated and modeled drain current (I_D) and transconductance (g_m) as a function of V_G for the GC transistor with L=2 μm, with L_{LD}/L=0.3 at a drain bias V_D= 1.5V.

In both figures, 4 and 5, good agreement is obtained for both the I_D and its derivative in all operational regions demonstrating that the proposed series association of transistors implemented in SmartSPICE is able to describe the DG GC behavior obtained from Atlas two-dimensional simulations.

The output conductance as a function of V_D for the equivalent DG GC implementation is shown in figure 6a as well as the transconductance over drain current ratio (g_m/I_D) as function of the drain current is shown in figure 6b.

In both figures the results from Atlas numerical simulations are also presented for comparison purposes. As can be seen, both characteristics are very well described in all operational regions by the GC equivalent circuit simulation.

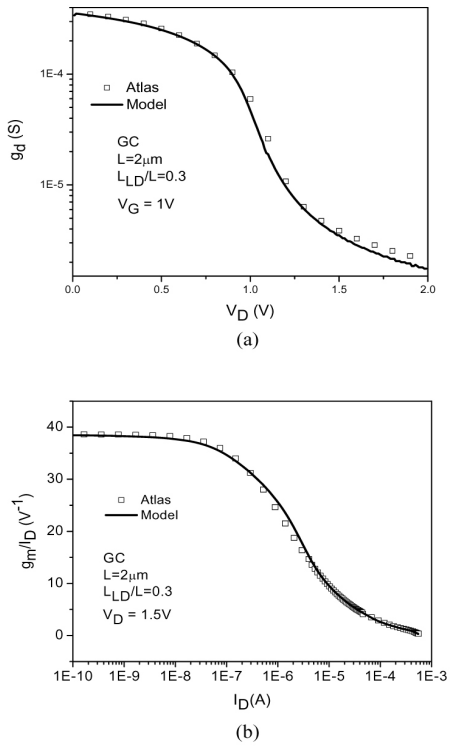

Figure 6. a) Output conductance of the GC transistor at V_G= 1V; **b)** g_m/I_D ratio of the GC transistor at V_D = 1.5V.

3. CURRENT MIRROR SIMULATION

In order to show the possibilities of the equivalent model to simulate circuits with graded-channel transistors in commercial circuit simulators, current mirrors with Common-Source and Wilson architecture were selected. Figure 7 presents the Common-Source current mirror and the equivalent implementation with DG GC proposed in this work.

The current mirror circuit was described in the SmartSpice as the interconnection of four transistors, as illustrated in figure 7b. Figure 8 shows the input current (I_{DIN}) and in figure 9 we have the output current (I_{DOUT}) as a function of the input drain voltage ($V_{D\,IN}$) with a fixed drain output voltage ($V_{D\,OUT}$) of 1.0 V in linear and semilogarithmic scale obtained by the equivalent model and ATLAS two-dimensional

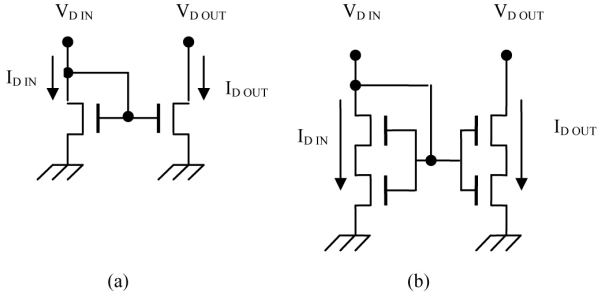

Figure 7. a) Common-Source current mirror and **b)** Current mirror with GC transistors formed by two transistors in series association.

simulator using the MIXED-MODE module, using GC devices with technological parameters of table I. Good agreement was obtained between circuit simulations and ATLAS MIXED-MODE ones, with a maximum error of 5 %.

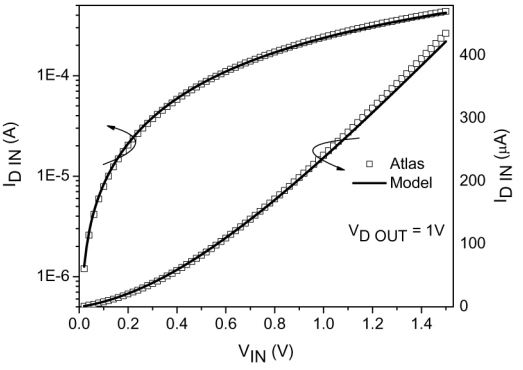

Figure 8. Input current of the current mirror circuit in Common Source architecture.

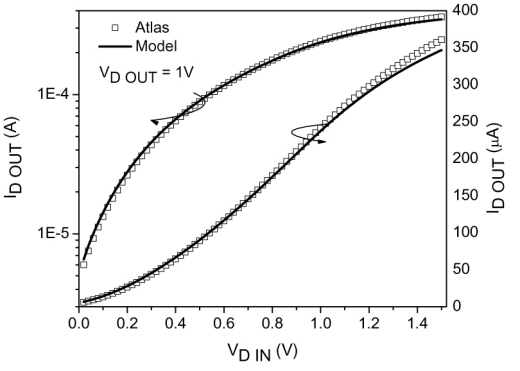

Figure 9. Output current of the current mirror circuit in Common Source architecture.

Figure 10 shows also a very good agreement for the ratio I_{DOUT}/I_{DIN} as function of the input current in semilogarithmic scale for the devices mentioned in table I, obtained by circuit simulation and by device simulation with MIXED-MODE and 2D ATLAS ensuring that the proposed equivalent circuit simulation scheme implemented in SmartSPICE successfully simulated circuits with DG GC devices.

As demonstrated in figure 10, the output current increase as the input current is reduced is very well described by the series association model. We can also note that the behavior of the circuit simulated is well described according to the use of GC devices with different channel length and L_{LD}/L ratios.

The current mirror in the Wilson architecture was also described in order to show that the implementation of GC devices in series association works rightly with larger circuits. In figure 11a we have a current mirror in Wilson Architecture as well as the equivalent circuit composed with GC transistors formed by the series association of two DG transistors in figure 11b.

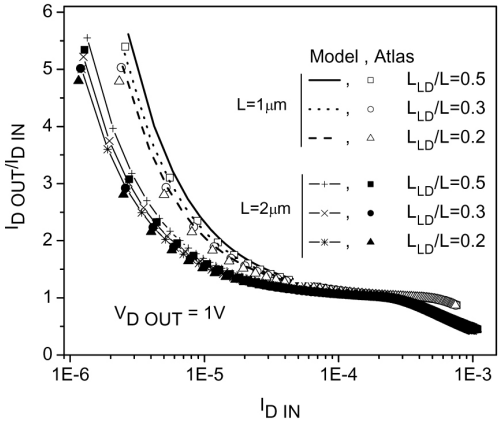

Figure 10. I_{DOUT}/I_{DIN} ratio as a function of $I_{D\,IN}$ for the current mirror with GC transistors with L = 1μm and L = 2μm, at $V_{D\,OUT}$ = 1V.

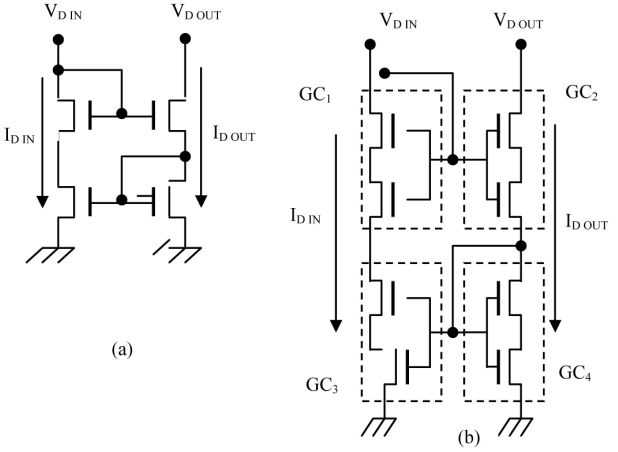

Figure 11. a) Current mirror in Wilson architecture and **b)** Current mirror with GC transistors formed by two transistors in series association.

In figure 12 the results of the $I_{D\,OUT}/I_{D\,IN}$ ratio for the two different channel lengths of the GC transistors and the three L_{LD}/L ratios can be seen.

As in the case of the common source architecture it is expected that the output current increase as the input current is reduced, but now an improved mirroring precision is achieved due to the disposition of the transistors that gives better characteristics.

In figure 13 we have the results of the simulation comparing both architectures: common source and Wilson architecture, showing that as it was expected with the Wilson architecture a better performance is obtained with an improvement in the mirroring precision that can be seen because $I_{D\,OUT}$ remains with a value similar to $I_{D\,IN}$ for a larger range of $I_{D\,IN}$.

In addition, calculations of the Output Resistance (R_{OUT}) confirm that the implementation of GC transistors with the series association has good results because with the current mirror in the Wilson Architecture it is expected to obtain a larger R_{OUT} compared with the common source architecture, showed in figure 14.

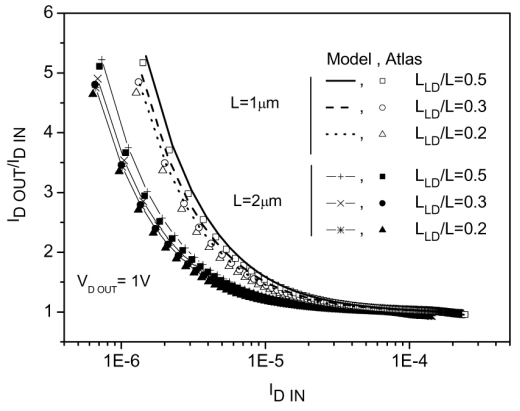

Figure 12. I_{DOUT}/I_{DIN} ratio as a function of $I_{D\,IN}$ for the current mirror in Wilson architecture with GC transistors with L = 1μm and L = 2μm, at $V_{D\,OUT}$ = 1V.

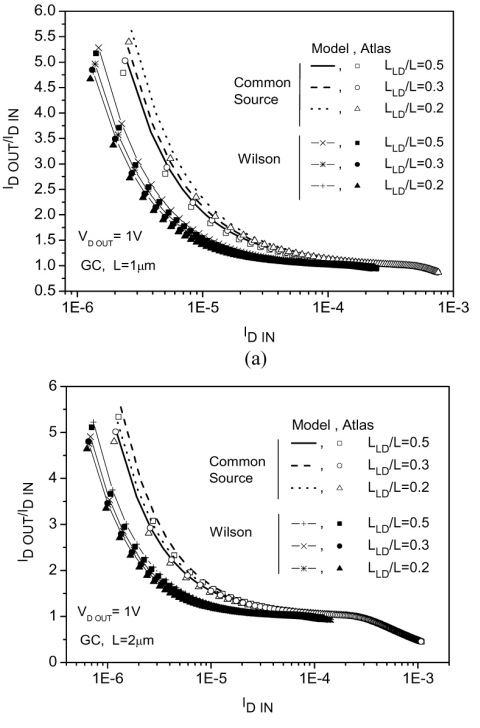

Figure 13. I_{DOUT}/I_{DIN} ratio for the two different architectures of current mirror **a)** Using GC devices of L=1μm **b)** using GC devices with L=2μm.

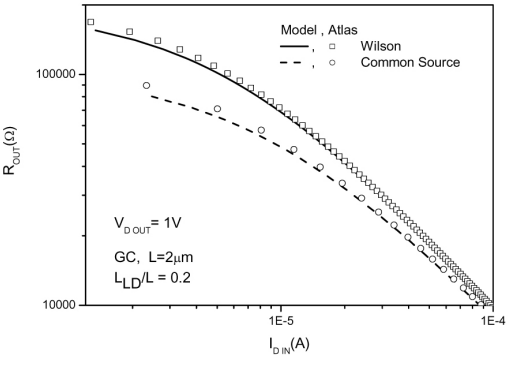

Figure 14. Output Resistance (R_{OUT}) for the two different architectures of current mirror using GC devices of L=2μm at V_D=1V.

4. CONCLUSIONS

This paper demonstrated that circuits containing Graded-Channel can be satisfactorily simulated using the Symmetric Doped Double-Gate Model previously introduced in SmartSPICE as an external model described in Verilog-A. Comparison of the I-V characteristics corresponding to a GC transistor with L=2μm and L_{LD}/L= 0.3, as well as their derivatives, obtained in SmartSPICE, with those obtained in MIXED-MODE and 2D ATLAS simulation provide very good agreement. In this case, the LD and the HD regions of the GC transistor are represented in SmartSPICE as two transistors in series, represented by the same model DSDGM with different parameters. The important parameter of the current mirror circuit I_{DOUT}/I_{DIN} ratio was obtained by circuit simulation and 2D device simulation showing a very good coincidence. In addition, it has been demonstrated that with the series association, circuits containing GC devices are very well described as it was shown with the comparing of current mirrors with different architectures, where our simulation follows the right behavior according to the kind of circuit simulated.

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