Impact of Selective Epitaxial Growth and Uniaxial/Biaxial Strain on DIBL Effect Using Triple Gate FinFETs

Sara Dereste dos Santos[1], João Antonio Martino[1], Eddy Simoen[2] and Cor Claeys[2,3]

[1]LSI/PSI/USP, University of São Paulo,
Av. Prof. Luciano Gualberto, 158 trav.3 - CEP 05508-900 São Paulo, Brazil
[2]Imec, Kapeldreef 75, B-3001 Leuven, Belgium
[3]E.E. Dept., KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium
sarad@lsi.usp.br

ABSTRACT

The influence of Selective Epitaxial Growth (SEG) and the Uniaxial and Biaxial Strain are studied in triple gate FinFETs, analyzing the Drain Induced Barrier Lowering Effect (DIBL). The splits using SEG present better performance for strained devices than the unstrained ones but the inverse is observed for devices without SEG. The DIBL values are higher for SEG devices in all cases. For devices without SEG, the effect of mechanical stress is more pronounced and the mobility is higher in the uniaxially strained devices. These devices have lower V_T values in the saturation condition causing the highest DIBL.

Index Terms: DIBL, Strain, SEG, Triple Gate, FinFET.

1. INTRODUCTION

FinFET is an interesting device concept for MOS transistors with gate lengths below 50 nm [1]. These devices belong to the multiple gates and non-planar device family and are widely studied as they strongly reduce short channel effects. The FinFET structures consist of a vertical silicon fillet (fin) with the gate wrapped around the three sides of the fin. A FinFET structure is presented in Figure 1. The gate oxide between the metal gate and the silicon fin determines whether the transistor has two or three gates, i.e., if the top gate oxide is too thick, the potential applied in this region is not sufficient to invert the channel in the top fin and therefore the transistor works as a double-gate structure. In triple gate FinFETs, with the influence of the three sides, the effective gate width of the transistor is equal to two times the height of the silicon-on-oxide layer plus the width of the silicon fin, $W_{eff} = 2H_{Fin} + W_{Fin}$. In these structures, improvements are obtained such as a reduction of subthreshold slope and better short channel effects (SCEs) [2,3].

Another way to improve the device performance is using strain engineering due to the increase of the carrier mobility. [4]. The mechanical stress can be

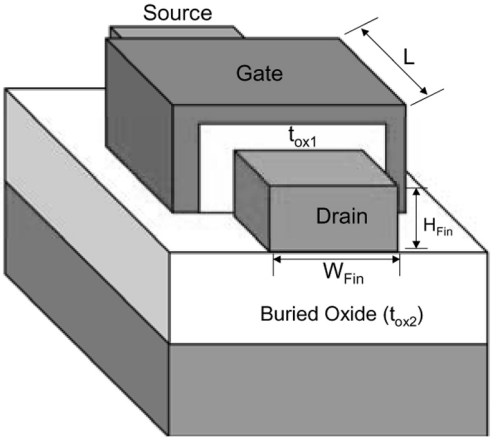

Figure 1. Triple gate FinFET structure.

generated by the insertion of foreign atoms in the silicon (such as Ge), which changes the original lattice parameter. Positive stress values indicate tensile stress and negative values are compressive [5].

Several techniques can be used to obtain strained silicon. One of the most popular techniques is to deposit a silicon nitride Contact Etch Stop Layer (CESL) with an intrinsic stress on top of a transistor transferring the film stress into the channel (uniaxial strain). Another manner to obtain stress is using the

biaxial global strain approach (sSOI), whereby the stress is introduced across the entire substrate by a SiGe buffer layer. When silicon is grown on top of this SiGe layer, the atoms in the silicon layer align with those in the SiGe layer, which has a slightly larger lattice constant [4,5]. The main characteristic of strained devices is the increase of the current drive due to higher carrier mobility. Also, the material band gap is affected by the stress that modifies the energy levels approach. The E_g variation changes directly the intrinsic carrier concentration and Fermi level, resulting in a threshold voltage that in general is smaller than unstrained devices [4].

The use of selective epitaxial growth (SEG) in source/drain regions contributes to performance enhancement by decreasing the total resistance [7]. In general, the thickness grown varies from 20 to 50 nm. Above these values the effect of current concentration is predominant and the total resistance increases again.

The DIBL effect has received special attention in order to evaluate the performance of new devices [2,8]. DIBL is a short channel effect (SCE) that shows the change of the threshold voltage with the drain voltage variation. When the channel length decreases the DIBL values tend to increase because of the significant portion of charges controlled by the drain [9]

In this paper, unstrained and strained nFinFETs are studied, comparing the DIBL behavior with and without SEG.

2. DEVICES FEATURES

The measured transistors are triple gate unstrained and strained nFinFETs with and without SEG processed at Imec. The transistors were fabricated on SOI wafers with 145 nm buried oxide thickness, according to the process described in [11]. The silicon layer thickness (H_{Fin}) is 65 nm and the EOT = 1.9 nm. The gate stack consists of 2.3 nm HfSiON on 1 nm interfacial SiO_2 capped by TiN and polysilicon. The biaxial tensile strain in the unprocessed sSOI substrates is 1.5 GPa. A Contact Etch Stop Layer (CESL) formed by SiN induces the uniaxial tensile strain. Multiple finger structures (5 fins) with variable fin width (W_{Fin}) and channel length (L) were measured. In all cases, the devices were measured at two different drain voltages, V_{DS1}= 0.05V and V_{DS2} = 1.2V. The constant current approximation method was used to obtain the threshold voltage value in both bias conditions. The DIBL was calculated by the equation (1).

$$DIBL(mV/V) = \frac{V_{T1(VDS1)} - V_{T2(VDS2)}}{V_{DS2} - V_{DS1}} \qquad (1)$$

3. EXPERIMENTAL STUDY

A. Devices without SEG

The $I_{DS}xV_{GS}$ characteristics were obtained from a HP-4156C parameter analyzer. Figure 2(a) presents the extracted threshold voltage and Figure 2(b) the equivalent value of DIBL for the three different process splits. It allows to directly compare de threshold voltage reduction with L roll-off and to point out differences between strained and unstrained devices. It is possible to note that an increase of DIBL occurs for small channel lengths in all devices due to the short channel effects. According to Figure 1(b), for the 80 nm-long devices, the DIBL value is 135 mV/V, 95 mV/V and 75 mV/V for the strained (uniaxial and biaxial), and unstrained (reference) devices, respectively.

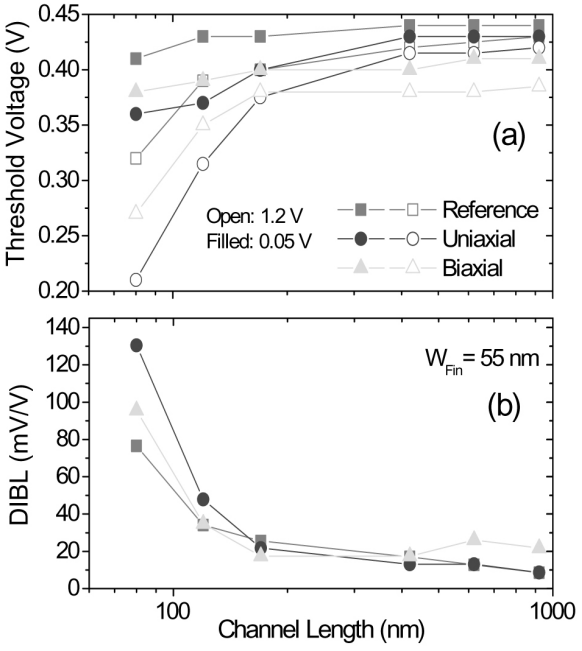

Figure 2. Threshold voltage **(a)** and DIBL **(b)** as a function of channel length.

The higher DIBL observed for strained devices can be associated to the drain depletion penetration. The strain causes the band gap (E_g) reduction that decreases the silicon work function (Fermi level decreases due to the increase of the intrinsic carrier concentration), which consequently affects the depletion region at the drain/channel junction, increasing the DIBL. For uniaxial devices, the increase of the drain depletion region is higher than the others and hence the DIBL is more pronounced due to the higher effective uniaxial stress obtained for short channel lengths.

Figure 3(a) shows the transconductance as a function of front gate voltage obtained for 80 nm-long devices for the V_{DS1} bias condition, confirming that strained devices present higher mobility and lower

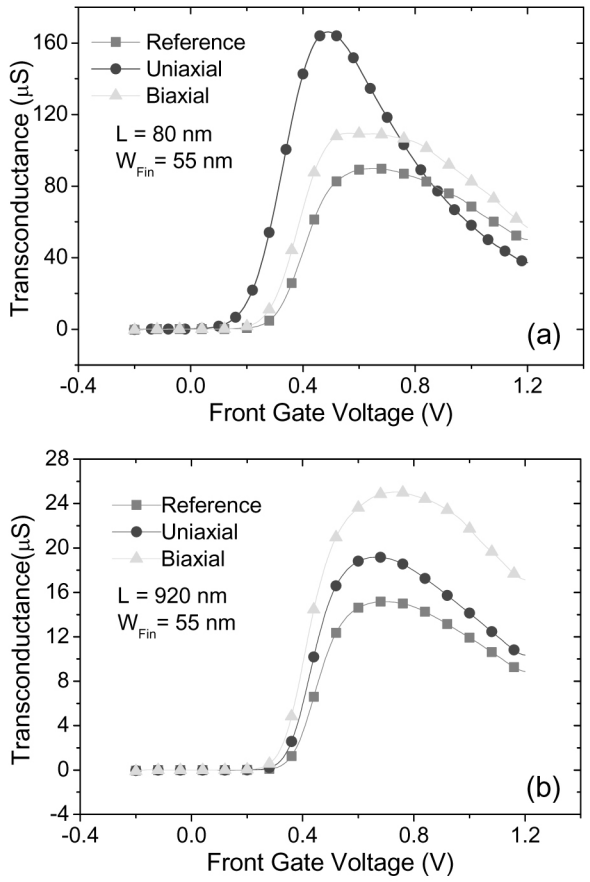

Figure 3. Transconductance versus front gate voltage for short **(a)** and large **(b)** channel lengths.

threshold voltage due to the bandgap decrease caused by strain. For biaxial devices, the influence of mechanical stress is not significant in small structures, approaching the unstrained device behavior. Figure 3(b) gives the same analyze using a large channel length. In this case, the uniaxial stress does not cause an effect in the entire channel because for large lengths the stress remains only near the source/ drain regions. Consequently, the current level is smaller and the transconductance appears below to the biaxial values. The effect of stress into two directions is more significant when the strained region is larger so that the performance of biaxial devices becomes better than the uniaxial ones, presenting a higher transconductance.

Figure 4 shows the DIBL for 100 nm channel length. The W_{Fin} varies from 25 nm to 2875 nm but for devices with W_{Fin} > 75 nm it was not possible to extract the DIBL by the current criteria due to the higher difference between the two curves analyzed. Increasing W_{Fin}, the threshold voltage also increases and DIBL reaches high values mainly for uniaxial devices since the channel size is small. The increase of DIBL for large fin width can be associated with the gates uncoupling. This effect occurs when the gates potential becomes stronger only next to the surface. The region where the potential is less strong is susceptible to suffer depletion coming from the drain potential.

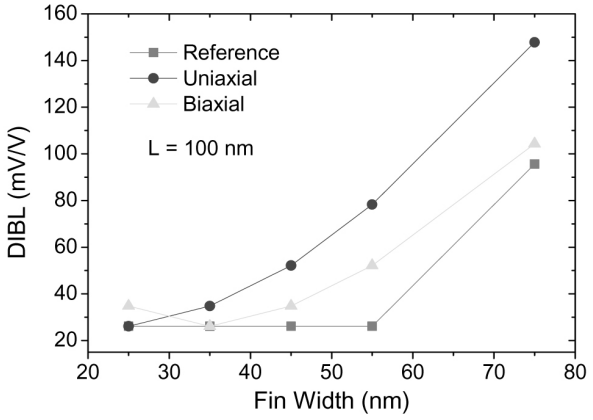

Figure 4. DIBL versus fin width for 100nm of channel length.

B. Devices with SEG

The same analyzes were done for devices with SEG. Figure 5 shows the threshold voltage (a) and the DIBL (b) as a function of channel length. An opposite behaviour is observed in this case where strained devices present better performance with small DIBL values. Observing the threshold voltage curve, it is possible to note an increase of V_T values for uniaxial devices. This increase indicates that the mechanical stress decreases when SEG is used. The transconductance variation is shown in Figure 6 for the short (a) and the large (b) channel length devices. In fact, for short channel devices, the transconductance level is the same for uniaxial and biaxial technologies demonstrating the effective loss of uniaxial stress. On the other hand, the biaxial device with large channel length presents a high transconductance, suggesting that the SEG process does not influence the mechanical deformation in the channel. The possible explanation for the SEG influence in the uniaxial stress case can be associated with the distance between the channel region and the tensile layer. The increase of source/drain areas because of the selective epitaxial growth decreases the distribution of the mechanical forces in the channel area.

Figure 7 presents the DIBL as a function of fin width for 100 nm of channel length. For W_{Fin} > 75 nm the DIBL values were also very high. In all situations, the strained devices show better performance with the smallest DIBL values. The difference between reference and biaxial devices is almost 30% for W_{Fin} = 75 nm.

C. Comparison between SEG and NO SEG Devices

Figure 8 shows a comparison among the transconductance (gm) versus the front gate voltage (V_{GS}) for unstrained and strained devices with and without SEG. It is possible to note an improvement of gm for biaxial devices and also for unstrained ones

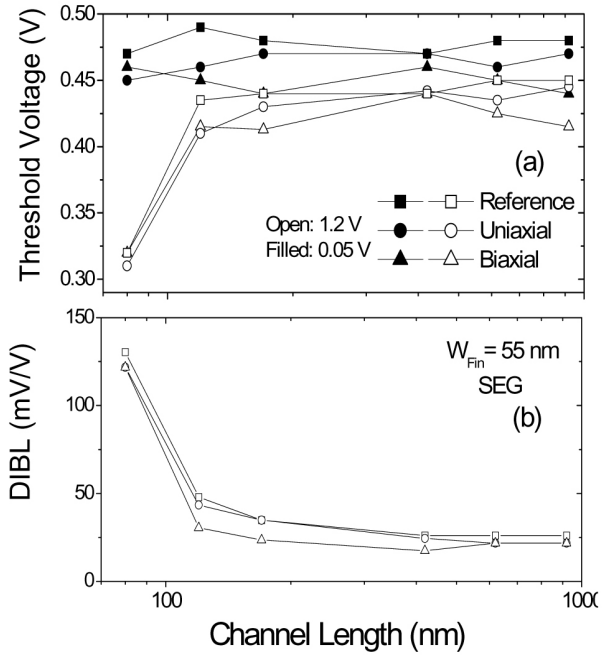

Figure 5. Threshold voltage (a) and DIBL (b) as function of channel length for SEG devices

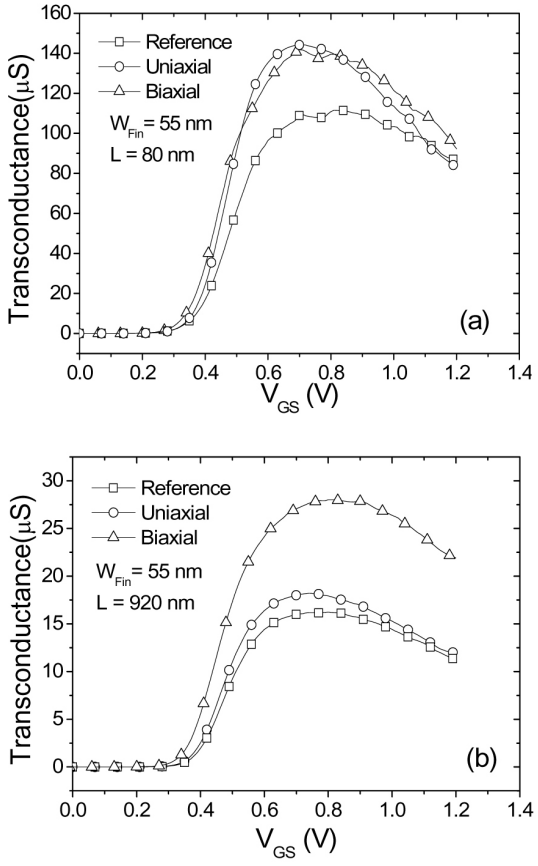

Figure 6. Transconductance versus front gate voltage for short **(a)** and large **(b)** channel lengths SEG devices

when selective epitaxial growth is used. This result is expected since the total resistance decreases [8]. However, the uniaxial device does not present a gm improvement in accordance with the previous explanation. Thus the use of SEG diminishes the stress effect induced by CESL, which can also be observed due to the increase of the threshold voltage (i.e., the energy bands are not much affected by strain). Uniaxial transistors without SEG present a higher gm degradation introduced by the strain process that decreases when SEG is used due to the decrease of the effective stress. The Figure 9 shows maximum transconductance (gm_{max}) as a function of channel lengths. For reference and biaxial devices there is an increase of gm_{max} when SEG is used. The opposite occurs for uniaxial devices for all channel lengths since the effective stress is lost.

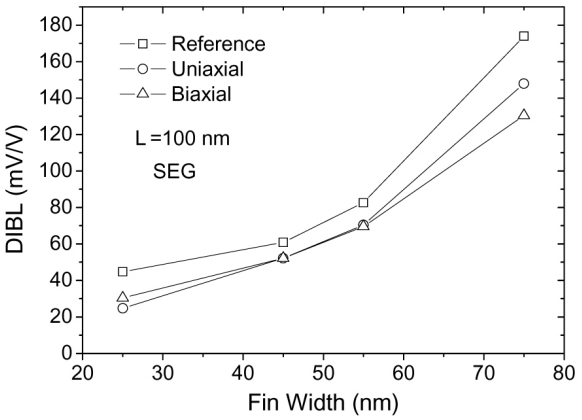

Figure 7. DIBL versus fin width for 100 nm channel length SEG devices

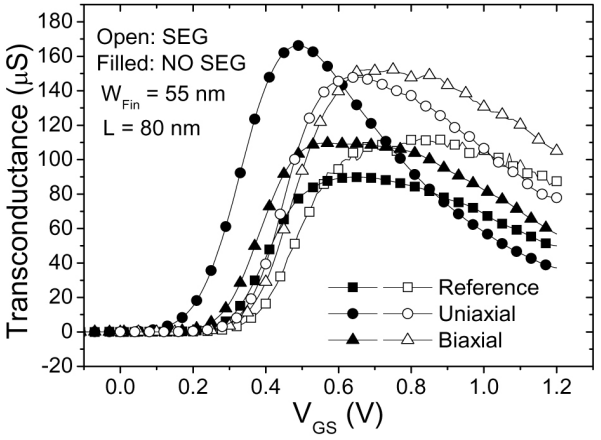

Figure 8. Transconductance as a function of front gate voltage for 80nm channel length and 55 nm of fin width

Table I shows the threshold voltage values for different channel lengths. The use of SEG results in higher V_T values that can be associated to the change in the flat-band voltage (V_{FB}). A possible change in the metal workfunction in addition to the decrease of the charges in the gate oxide would be responsible for the V_T increase.

The results of Figure 10 and Figure 11 confirm that DIBL increases for short channel lengths and also for high fin widths. A comparison between SEG and NO SEG devices for 80 nm channel length show that

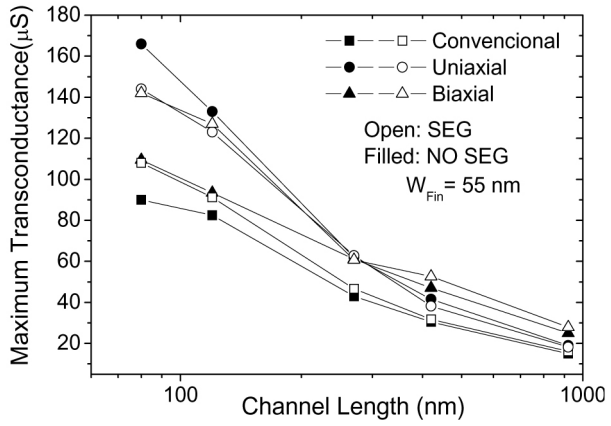

Figure 9. Maximum transconductance as a function of channel length.

Table I. V_T values for devices with and without SEG and V_{DS} = 50 mV

L (nm)	V_T Reference (V)		V_T Uniaxial (V)		V_T Biaxial (V)	
	SEG	NO SEG	SEG	NO SEG	SEG	NO SEG
920	0.48	0.44	0.47	0.43	0.44	0.41
620	0.48	0.44	0.46	0.43	0.45	0.41
420	0.47	0.44	0.47	0.43	0.46	0.40
170	0.48	0.43	0.47	0.40	0.44	0.40
120	0.49	0.43	0.46	0.37	0.45	0.39
80	0.47	0.41	0.45	0.36	0.46	0.38

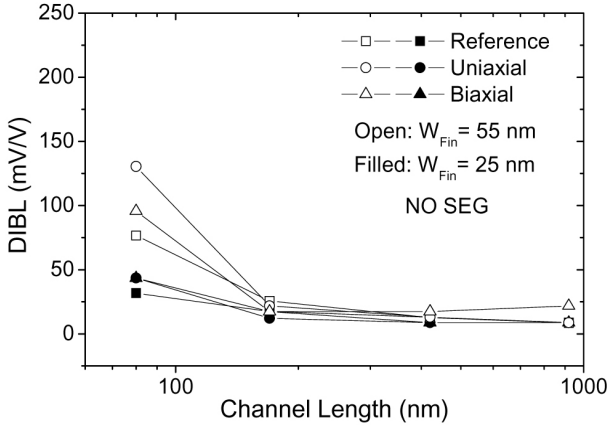

Figure 10. DIBL versus channel length for two different fin widths using devices without SEG.

there is an increase of DIBL in all situations when SEG is used. Strained devices with SEG present better DIBL values than the unstrained ones and for W_{Fin} = 25 nm this difference increases. However the inverse is observed for NO SEG devices.

Comparing the results presented in Figure 12, the curves of 75 nm fin width devices without SEG show approximately 50% of variation between the unstrained and uniaxial technologies. Strained devices in this case are more susceptible to DIBL. However, the DIBL values for unstrained devices with SEG are the highest. For W_{Fin} > 75 nm the threshold voltage variation becomes very large due to the gates uncoupling

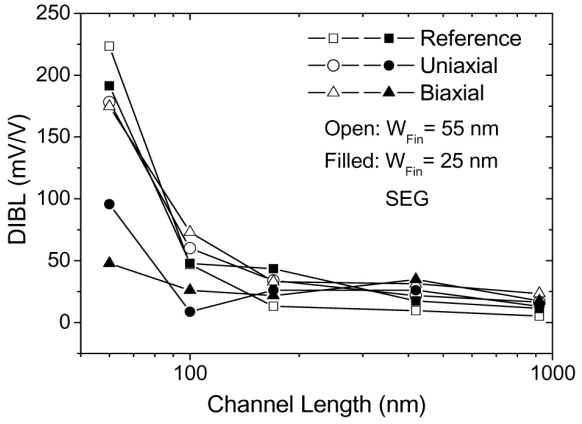

Figure 11. DIBL versus channel length for two different fin widths us-ing devices with SEG.

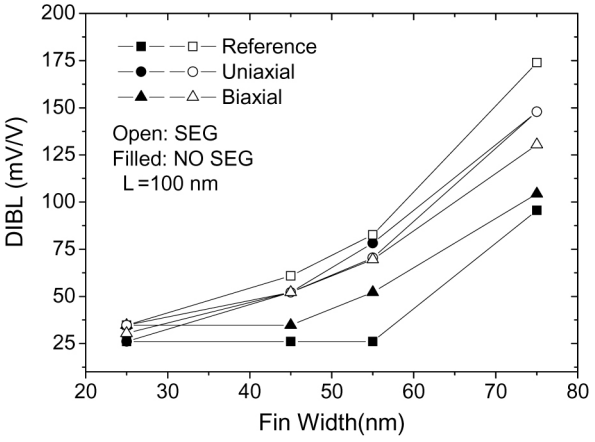

Figure 12. DIBL comparison between SEG and NO SEG as a function of fin width for 100 nm channel length.

and the higher short channel effects. In general, NO SEG devices with strain present worse DIBL than unstrained ones mainly due to the narrower bandgap in strained devices. Devices with SEG exhibit an increase of DIBL values due to the decrease of source/drain contact resistance that induces an increase of the potential in the channel region, i.e. most of the drain potential remains in the channel, causing an increase of the charge depletion. Consequently, a small gate potential is sufficient to invert the channel so that the threshold voltage for high drain voltage is smaller, resulting in a higher DIBL.

4. CONCLUSIONS

This paper presented a study on the DIBL effect in unstrained and strained devices with/without selective epitaxial growth.

The FinFETs with SEG presented high DIBL due to the decrease of series resistance and, consequently, an increase of potential drop into the channel (from drain side to source). In this case, strained devices presented better performance (i.e. smaller DIBL) com-

pared to unstrained ones. For uniaxial devices, the SEG process caused a stress decrease due to the larger distance between the tensile layer and the channel region because of the epitaxial layer grown. As a result, the effective stress into the channel was smaller than for the devices without SEG. For biaxial devices with SEG, the increase of DIBL occurred due to the change in the total resistance. It was verified that the high potential in the channel region caused higher charges depletion and induced higher DIBL. Therefore, the DIBL values depended on the change in the total resistance.

Analysing the devices without SEG, the opposite behaviour was observed. The strained devices were more susceptible to DIBL due to the narrower bandgap than for the unstrained ones. For these devices, the resistance distribution (source, channel and drain resistances) was almost the same even as the potential drops.

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