Performance of Source Follower Buffers Implemented with Standard and Strained Triple-Gate nFinFETs

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ABSTRACT

In this work the application of standard and strained triple-gate FinFETs in unity-gain source-follower configuration is compared. The analysis is performed by evaluating the buffer voltage gain with respect to the fin width and channel length as well as the total harmonic distortion. It is demonstrated that the application of strained material in narrow FinFETs, when the devices are operating in double-gate mode, can be beneficial for the performance of buffers in any channel length. On the other hand, for triple-gate FinFETs or quasi-planar ones the degradation of the output conductance overcomes the transconductance improvements from strained material and the performance of standard buffers is better than of strained ones. Narrow strained buffers also offer better harmonic distortion.

Index Terms: use maximum 5 index terms.

1. INTRODUCTION

Multiple-gate devices are important candidates for the continuous MOSFET downscaling to the nanometer technological nodes due to the excellent gate control of the channel charges allowing for excellent short-channel immunity. Generally, tall devices with relatively narrow fins are used to improve the gate control by the coupling between the two sidewall gates[1] , leading these devices to operate as double-gate ones. Thus, the majority of the drain current flows in the (110) plane and not in the traditional (100) plane as in planar devices. The problem associated with this change in the conduction direction is that the mobility of electrons is degraded in the (110) crystal orientation with respect to (100), thereby reducing the on-to-off (I_{ON}/I_{OFF}) current ratio [2].

Recently, the adoption of mechanically strained silicon techniques as mobility booster is being largely applied, providing higher current drive without increasing the off-state current. For nMOSFETs tensile strain is desired whereas for pMOS compressive strain is necessary to improve the device characteristics. Strained silicon layers can be obtained in a localized way by the use of strained Contact Etch Stop Layers (CESL), which leads to process-induced strain in the channel direction only (or uniaxial)[3]. On the other hand, strained material can be globally applied by the use of substrate-induced (or biaxial) strained material (or sSOI). In the latter case, epitaxially grown Si_xGe_{1-x} relaxed buffer layers are formed with the desired lattice parameter where on top a monocrystalline strained silicon layer is obtained[4]. In the literature successful improvements by the use of strain in planar Silicon-On-Insulator (SOI) devices with ultra-thin body can be found, not only for the carrier mobility[5] but also for the low frequency noise[6], the analog performance[7] and the linearity[8]. Thus, the use of strained material in FinFETs is of interest because it can contribute to the electron mobility increase in narrow devices. Successful results have been shown for digital device aspects by introducing uniaxial or biaxial strain in FinFET devices and confirm the expectation of device performance improvement[9,10].

The potential of FinFETs in analog applications has also been demonstrated at device level exhibiting reduced drain output conductance (g_D) and higher open-loop voltage gain[11]. Successful implementation of analog circuits[12] and analog-to-digital convert-

ers[13] has been demonstrated. However, in ref. [14] it has been presented that the analog performance of strained FinFETs can be inferior to standard ones because of the larger channel length modulation effect degrading the g_D, depending on the fin width. Standard and strained FinFETs with short channel length and narrow fins have similar analog properties, whereas the increase of the channel length degrades the g_D of the strained devices, consequently decreasing the device intrinsic voltage gain with respect to standard ones. Narrow strained FinFETs with long channel show a degradation of the g_D if compared to standard ones.

Analog buffers are important circuits for general purpose analog systems aiming at impedance matching. Classically they are implemented in source-follower configuration (or common-drain amplifier)[15], where the device is biased by a current source (I_{bias}) in common-drain configuration, with a bias voltage (V_D), as presented in Figure 1. The input (V_{IN}) and output (V_{OUT}) signals are also indicated in Figure 1. Ideally, these circuits should have unitary voltage gain and do not add any distortion to the input signal, having high input impedance and low output impedance. However, because of the non-zero MOSFET output conductance as well as the non-linear output current *versus* voltage characteristics, these circuits degrade the input signal by reducing the voltage gain to less than one and add some distortion to the input signal.

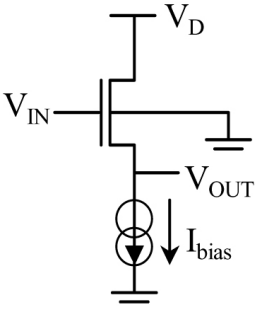

Figure 1. Schematic representation of a unitary voltage gain source-follower buffer.

The purpose of this paper is to study the main figures of merit for FinFETs in source-follower operation using standard and strained devices, comparing the performance of them.

2. EXPERIMENTAL RESULTS AND DISCUSSION

The devices used in this work were fabricated at the IMEC facilities, following the process flow described in ref. [16]. In case of strained FinFETs, sSOI wafers with 1.5 GPa intrinsic biaxial tensile strain and buried oxide thickness t_{box}=130 nm were used whereas standard Unibond wafers have t_{box}=145 nm. The fin height (H_{Fin}) is 60 nm and 55 nm for the standard and sSOI FinFETs, respectively. The gate stack is composed of a 1 nm thick interfacial thermal oxide with on top 2 nm HfO_2. Then, a 5 nm thick TiN layer is deposited and a 100 nm thick amorphous silicon capping completes the gate stack. No channel doping or halo implantation is applied during the processing, keeping the p-type doping level in the order of 10^{15} cm^{-3}. Nickel silicidation is used to reduce the series resistance.

A. Voltage Gain

Standard and strained triple gate FinFETs were measured in the source-follower configuration, as shown in Figure 1, and the output characteristics were obtained with a Keithley 4200 SCS Semiconductor Parameter Analyzer. The drain voltage (V_D) has been fixed at 1.0 V and the V_{OUT} *vs.* V_{IN} characteristics were obtained by sweeping the gate voltage (hereafter called the input voltage, V_{IN}), and measuring the source voltage, V_{OUT}, for different bias current (I_{bias}). For comparison purposes the devices were biased with a normalized bias current ($I_{bias}/(W/L)$) of 100 nA and 4 μA, covering the operation in moderate and strong inversion regimes, respectively.

Initially, the influence of the fin width (W_{Fin}) on the buffer operation has been verified. In this case, devices having single fins with channel length of L=10 μm were used. The V_{OUT} curves as a function of V_{IN} for standard and strained buffers in both biasing conditions are presented in Figure 2. The device channel width has been estimated as $W=2*H_{Fin}+W_{Fin}$.

Using the curves of Figure 2 the input voltage range (V_{IR}), that is the difference between V_D and the minimum V_{IN} for which the output voltage is higher than zero can be extracted as indicated in Figure 3.

As the fin width is increased, independently if standard or strained devices are considered, there is an increment of the available V_{IR} that can be associated to the small differences of the threshold voltages as well as the larger carrier mobility in devices with wider fins due to the top conduction. Also increasing the bias current and moving the device towards strong inversion reduces the V_{IR} because of the smaller V_{OUT} required as $I_{DS}/(W/L)$ is increased. When comparing devices with and without strain it is clear that the application of strain increases the V_{IR} for devices with similar W_{Fin} which is caused by the smaller input voltage required to sustain the same normalized drain current because of the larger carrier mobility. This effect happens in both moderate and strong inversion regimes.

From the measured V_{OUT} *vs.* V_{IN} curves the buffer voltage gain (A_V) has been calculated as $A_V = dV_{OUT}/dV_{IN}$. Figure 4 presents results of A_V as a function of W_{Fin} for L=10 μm standard and strained FinFETs. The open symbols refer to operation in moderate inversion and the closed ones to strong inversion.

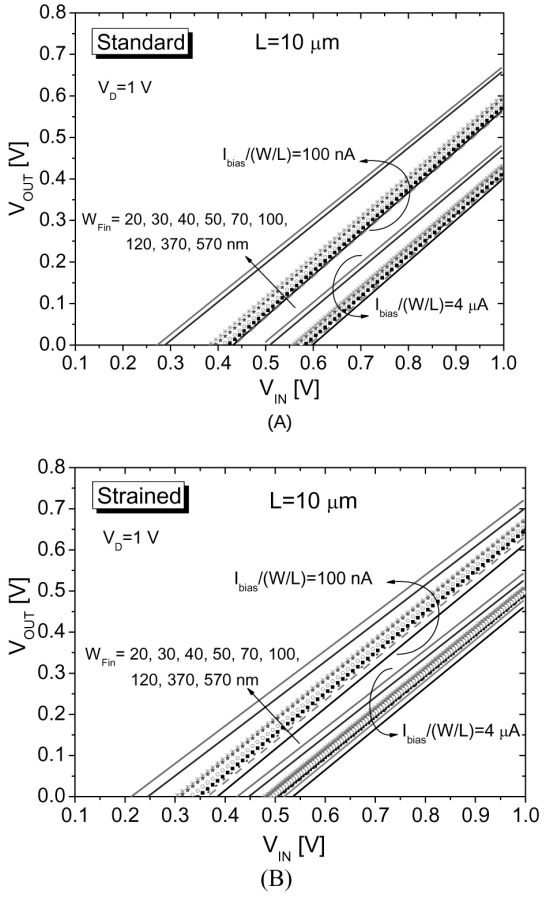

Figure 2. Measured V_{OUT} versus V_{IN} curves (V_D=1 V) for **(A)** standard and **(B)** strained FinFETs with L=10μm and several W_{Fin}*

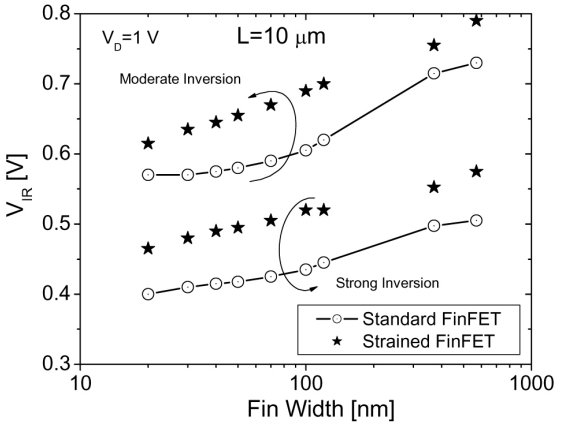

Figure 3. Extracted V_{IR} as a function of W_{Fin} for single fins with L=10 μm.

The voltage gain (A_V) in buffer configuration is described by eqn. (1) [15]:

$$A_v = \frac{g_m}{ng_m + g_D} \qquad (1)$$

where g_m is the transconductance and n is the body factor.

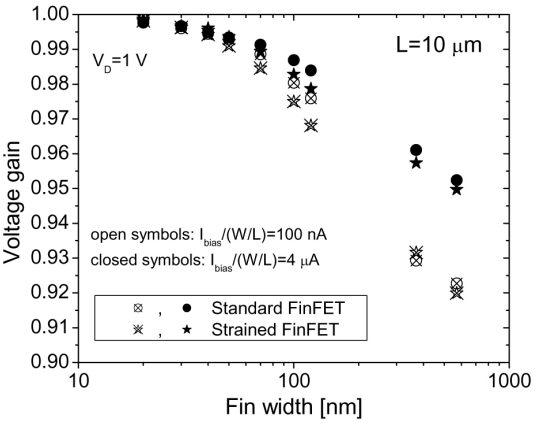

Figure 4. Measured voltage gain as a function of W_{Fin} for devices biased in moderate and strong inversion regimes.

From equation (1) one can see that the theoretical limit for A_V is 1/n and is obtained when g_D is negligible. The results of Figure 4 show that, irrespective if standard or strained material is used, the A_V is closer to the unity (or nearly ideal) for narrow W_{Fin}, when the devices operate in double-gate mode. The excellent gate control provided by the reduced W_{Fin} yields a body factor close to one and the g_D of these devices is extremely reduced. Independent of the bias in moderate or strong inversion, there is practically no difference between the performance of standard and strained buffers for W_{Fin} up to 40 nm. Increasing W_{Fin} there is a reduction of the gain mainly related to the increase of g_D. Although the degradation on g_D of strained devices could degrade A_V, in case of narrow W_{Fin} the increase of g_m thanks to the strain overcomes the degradation of g_D leading to a similar gain. On the other hand, for FinFETs wider than 40 nm, i. e. when the devices are operating in triple-gate mode or as a quasi-planar one, the mentioned increase on g_D of strained devices degrades A_V with respect to standard ones for any W_{Fin} and bias condition. The reduction on the bias current degrades A_V of both standard and strained FinFETs because of the g_m reduction.

For comparison purposes the A_V of planar fully-depleted SOI devices with L=10 μm from a 65 nm technology with 1.5 nm thick nitrided gate oxide and 15 nm thick silicon film[17], made in standard and biaxially strained material, has been extracted in strong inversion. The obtained results are A_V=0.980 and A_V=0.978 for standard and strained transistors respectively, confirming that the presence of strain leads to similar A_V also for planar transistors. The degradation of A_V in planar devices with respect to narrow FinFETs is caused by the increase of n as well as the higher g_D. However, these values are comparable to the results obtained for FinFETs with W_{Fin} wider than 120 nm indicating the improvements provided by narrow FinFETs in this analog building block.

The influence of the channel length has been verified for standard and strained devices biased in moderate and in strong inversion, as presented in Figure 5. In this case, multiple finger devices composed by 30 fins with W_{Fin}=20 nm have been used.

Independent of the bias in moderate or strong inversion regimes, the results of Figure 5 indicate that for any channel length the A_V of strained devices is larger than for standard ones. For shorter L this difference increases. Following the results of Figure 5 it is clear that shorter strained FinFETs can be used for a given A_V. Moving the operational point from moderate to strong inversion also degrades the A_V as for the single fins because of the gm reduction. Although there is a relaxation in the strain component perpendicular to the current flow in narrow FinFETs[18], making the strain practically uniaxial, the remaining strain improves the gm such that the A_V of strained FinFETs becomes larger than for standard ones.

B. Harmonic Distortion

As previously mentioned, it is known that buffers introduce some non-linearity (or distortion) to the input signal. In the previous section the use of strained FinFETs demonstrated to be beneficial with respect to the voltage gain. The following analysis aims to compare the harmonic distortion introduced in the input signal by buffers with and without strain. To conduct this evaluation, the Integral Function Method [19,20] has been applied. The input signal was considered as composed by a constant bias voltage V_{IN} associated with a sinusoidal signal with amplitude Va.

The influence of fin width on the harmonic distortion of standard and strained FinFETs is presented in Figure 6 where the Total Harmonic Distortion (THD), obtained in the middle of V_{IR} for Va=25 mV in strong inversion, is plotted.

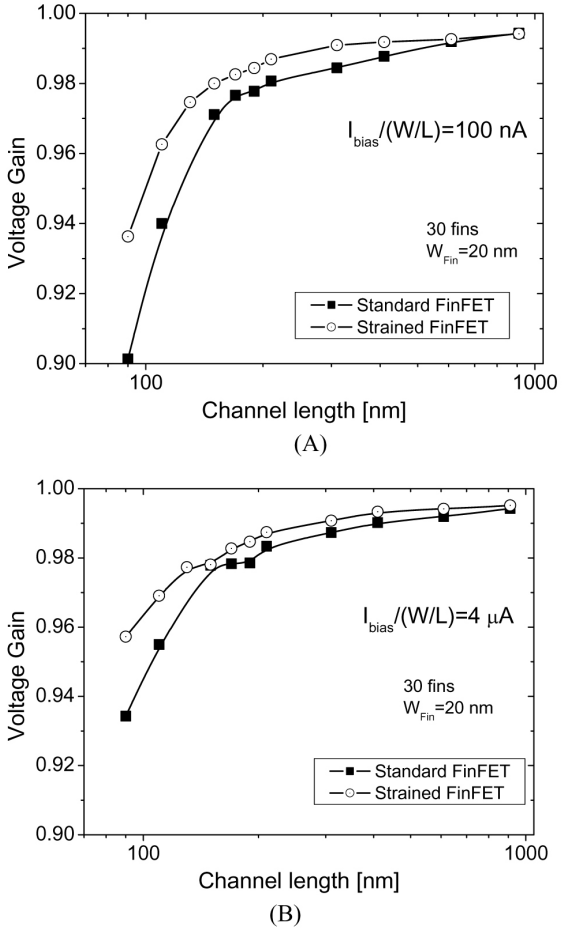

Figure 5. Extracted A_V as a function of L for standard and strained multi finger devices with W_{Fin}=20 nm biased in moderate and strong inversion regimes.

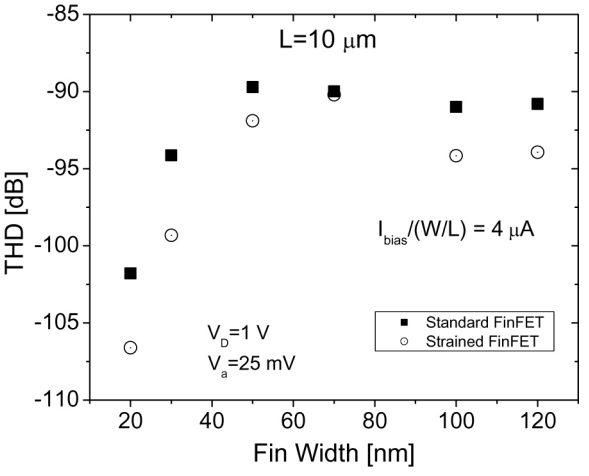

Figure 6. Extracted Total Harmonic Distortion as a function of W_{Fin} for standard and strained FinFETs .

Initially, the results of Figure 6 show that buffers implemented with FinFETs, for both standard and strained ones, present a linearity level below -90 dB, which ensures good linearity. The reduction of W_{Fin} benefits the linearity. Also the results of figure 6 indicate that the application of strain improves the linearity by about 4 dB with respect to standard FinFETs in case narrow devices are used.

When applied as buffers, the most important distortion component is the second order harmonic (HD2). Following ref. [21], the second order harmonic distortion of a source-follower is given by:

$$HD2 \approx THD \approx \frac{1}{4T} \cdot \frac{g_D}{g_m} \frac{2V_{ip}}{V_{GS} - V_t} \qquad (2)$$

where T is the feedback factor, V_{GS} is the gate voltage, V_t is the threshold voltage and V_{ip} is the peak input voltage.

The improvement of the linearity as W_{Fin} is reduced can be understood with the help of equation (2) as the g_D term decreases for narrow FinFETs. Considering that for all the devices a similar amplitude has been applied as well as they are biased in similar condition, despite the higher g_D in strained FinFETs

than in standard ones and the slightly small V_{GS}-V_t, both contributing to worsen the linearity, the larger gm is responsible for the improvement demonstrated in figure 6.

The THD extraction for the planar devices mentioned in the previous session results in -76 dB and -78 dB for the standard and strained FD SOI MOSFETs, repectively. This confirms that the linearity of FinFETs as buffers is better than for planar devices, with a difference larger than 10 dB in favor of FinFETs. Looking at equation (2) one can see that the reduction of the output conductance in FinFETs leads to better THD.

3. CONCLUSION

The performance of narrow source-follower buffers, when the devices are operating mostly like a double-gate transistor, is improved or at least presents similar behavior than for standard FinFETs by the application of strain when the devices are biased in moderate and strong inversion due to the larger transconductance that overcomes the degraded output conductance of strained FinFETs. On top of a nearly ideal voltage gain, the input range of strained devices is improved. When the fin width is increased, the improvement of the transconductance of strained FinFETs is not enough to compensate their output conductance degradation and the voltage gain of strained FinFETs becomes smaller than for standard ones. For narrow FinFETs, independently, if in moderate or strong inversion, the improvement provided by the strain holds for any channel length indicating that this analog building block can benefit from the application of strain. The harmonic distortion of narrow strained FinFETs is improved with respect to standard FinFETs, which can also be associated to the larger transconductance. A comparison with planar fully depleted SOI MOSFETs from a 65 nm technology confirmed that the gain is larger in narrow FinFETs as well as the linearity is more than 10 dB better.

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