A 5.4 GHz Fully-Integrated Low-Noise Mixer

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ABSTRACT

An active mixer using a Gilbert-cell topology that incorporates a low-noise RF transconductance stage is presented in this paper. The chip operates at a frequency of 5.4 GHz and was fabricated in 180 nm CMOS technology. A current-bleeding circuit is used to provide different dc bias currents to the LO switching stage and the RF transconductors. The transconductor, designed using the power constrained simultaneous noise and input match technique, together with the bleeding circuit enables the mixer to have a measured single-sideband noise figure of 7.8 dB and a power conversion gain of 13.1 dB. The measured input-referred 1-dB compression point, IP_{1dB} is -17.8 dBm while its OP_{1dB} is -5 dBm. A two-tone test was carried out and the mixer exhibits an IIP3 of -6.2 dBm and an OIP3 of +6.9 dBm. All of the inductors are on-chip and the size of the mixer core is only 380 μm x 350 μm (0.133 mm^2).

Index Terms: RFIC, mixer, CMOS, MMIC, low-noise, microwaves.

1. INTRODUCTION

The system noise figure (NF) of a receiver is a measure of how much electronic noise is generated inside the receiver at a particular ambient temperature. Reducing the system NF is of fundamental importance because it allows the receiver to detect weaker signals. In practical terms this means that if a hub tower for cellular communications has a low-noise receiver, that receiver will be able to detect incoming signals from cell phones that are further away. In turn, this will increase the tower's coverage area and therefore fewer towers per square kilometer will be needed, ultimately leading to lower operating costs for service providers and lower fees for their end-users.

To reduce the system NF of a receiver, the individual NF of the receiver components need to be reduced. A basic conclusion from Friis's equation [1] for calculating the total NF of a cascaded network is that the gain and NF of the components at the input of the network dominate the total NF relative to components that are further down the chain. In wireless receivers, the first element after the antenna is often a bandpass filter for band selection. These filters are normally passive and since their NF is related to the transmission loss through them, expensive low-loss ceramic materials such as alumina (Al_2O_3) are often used to implement the filters [2]. At frequencies below a few GHz, surface acoustic wave (SAW) filters are predominant. While the NF of the filters is reasonably small, the fact that they are passive means that their power gain is below 0 dB and hence their impact on the total NF of the receiver is significant. If a low-noise amplifier (LNA) is placed before the filter, this will certainly improve the system NF but the radio designer must be certain that any strong out-of-band signals picked up by the antenna will not overdrive the LNA and create distortion. Thus, to avoid this problem, it is common to put the filter first followed by the LNA stage.

Traditionally, the mixers used in communications receivers have had higher noise figures relative to those of the LNA circuits. Since the mixers appear after one or more amplification stages, their contribution to the system NF can be mitigated. Nevertheless, it is of significant interest to develop mixer circuits with low NF because this can relax the gain requirements in the preceding LNA stages that is needed to keep the system NF below a certain level. One benefit of reducing the gain of the LNA stage even by just a few dB is that the third-order intercept point (IP3) of the entire receiver can be noticeably improved.

In this article we describe a 5.4 GHz low-noise active mixer that was designed and fabricated using a standard 180 nm CMOS process. The mixer has a Gilbert-type LO switching core and it uses a symmetric low-noise transconductance stage to convert the RF input signal from a voltage signal to a current signal before entering the switching core. In the next section, a short background on developments in low-noise mixers will be presented. In Section 3 a detailed description of our proposed circuit will be given and Section 4 will present the measured results.

2. BACKGROUND

There are two general classes of RF mixer circuits: passive and active. As their name implies, passive mixers do not consume dc power and they are typically made using Schottky diodes or FET devices, but superconducting devices such as Josephson Junctions are also used to make mixers for radio astronomy receivers [3] and other scientific applications.

Depending on the devices that are used to make a passive mixer they can operate at exceptionally high frequencies reaching into the THz region. They also have very good linearity performance but along with these positive attributes there is also the fact that they have conversion loss instead of gain. With regards to NF, it is well known that the number of devices in the mixer is a major determinant of the circuit's NF. For example, unbalanced passive mixers using only one device will have a lower NF than double-balanced mixers that have four devices, provided the devices are the same. In high-performance communications systems, unbalanced mixers are usually not an option to reduce NF because it is often the case that only double-balanced mixers can meet the necessary linearity, port-to-port isolation, spurious rejection specifications of the radio links.

In the case of active mixers one of their most important characteristics is that they can be designed to have conversion gain, which means fewer amplifiers are needed in the receiver system. Active mixers implemented in monolithic form lend themselves to higher levels of integration: it is fairly straightforward to design double-balanced mixers and connect them with the LO circuits and amplifier stages on the same chip. In terms of operating bandwidth they do not yet reach into the THz region like passive mixers, but they can operate above 100 GHz which is quite adequate at this time for commercial wireless applications.

Active mixers based on the Gilbert-cell topology [4] are in widespread use because they are double-balanced and they can produce high amounts of conversion gain. However, their NF has traditionally been noticeably higher than passive mixers and even other active mixers. Nevertheless, research advances have shown that the NF of Gilbert cell mixers can be significantly reduced by replacing the RF transconductor stage of the mixer with a low-noise amplifier (LNA) type of circuit [1]. One challenge is that as the gate-length dimension scales down, the biasing current required increases, which in turn reduces the conversion gain. To alleviate this problem, the current-bleeding technique [6] can be applied to reduce the noise figure and supply the current required by the transconductors [7][8][9][10][11]. As the transistor gate-length is reduced, a larger bleeding circuit is required. The large tail capacitor associated with the bleeding circuit will require a shunt inductor to be placed between the drains of the transconductors to keep the gain high even when flicker noise is not a concern. This paper shows that by properly designing the transconductor, the shunt inductor can be removed while all inductors can be realized on-chip without compromising its performance.

3. INTEGRATED CIRCUIT DESIGN

The goal of this work is to improve the performance of the low-noise mixer in Figure 1 in several ways. While prior designs with a similar topology required large inductors, which often had to be placed on-chip, here all of the inductive elements have been carefully optimized to create a compact RFIC without resorting to off-chip components. Furthermore, the conversion gain of the mixer has been kept at a fairly high value to be able to relax the gain on the LNA stages that would normally precede the mixer.

A. Low-Noise Transconductors

A simple way to design the low-noise transconductors in the RF stage of the mixer shown in Figure 1 is to use the simultaneous noise and impedance match

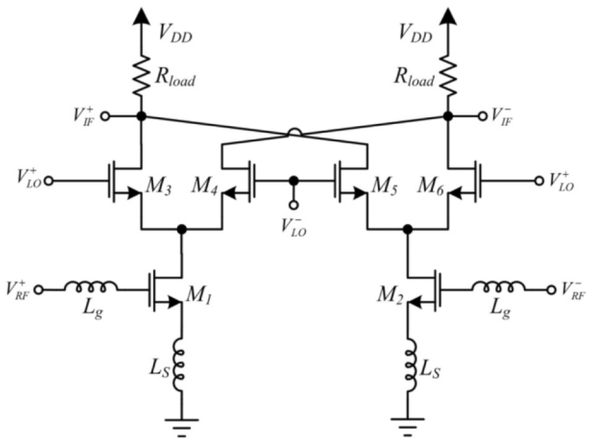

Figure 1. Conventional low-noise mixer circuit.

(SNIM) technique to achieve the lowest possible noise figure and input match at the same time [12]. However, the drawback of that method is that the large gate-source capacitance (C_{gs}) required in the transistor results in a large current consumption. Since the required C_{gs} at a particular frequency is roughly independent of technology node, the drain current increases substantially when shorter gate-length transistors are used. Furthermore, as the length of the transistor goes down, so does the operating voltage. Besides increased dc power consumption, having large bias currents in the mixer has another unwanted consequence: low voltage headroom because of the large voltage drop across the load resistors, R_{load}. To maintain a reasonable voltage headroom, R_{load} must be reduced but then the conversion gain is adversely affected since the conversion gain of the basic Gilbert-cell mixer is given by [13] [14]

$$A_V = \frac{2}{\pi} g_m R_{load} \tag{1}$$

where g_m is the transconductance of the RF stage and perfect switching is assumed for transistors M_3-M_6.

The approach chosen here to obtain a high conversion gain for the mixer while maintaining a reasonably large voltage headroom is to reduce the dc bias current is to apply the power constrained SNIM (PCSNIM) technique to the RF transconductors. A description of the method, originally developed for LNA's, is given in [12].

The resulting mixer circuit is shown in Figure 2. Transistors M_1 and M_2 are the low-noise transconductors and C_{ex} is an external capacitor placed between the gate and the source of the transistor so that the device size can be reduced. To simultaneously accomplish noise and input match, C_{ex} and L_s are chosen to obey the following relationships

$$C_{gs} + C_{ex} \approx \frac{2G_{opt}}{\omega} = \frac{2}{Z_o \omega} \tag{2}$$

$$L_s = \frac{Z_o (C_{gs} + C_{ex})}{g_m}. \tag{3}$$

The inductor sizes used in this chip were: 0.33 nH for L_s and 4.2 nH for L_g. While the PCSNIM technique allows us to reduce the dc bias current and at the same time the load resistors can be large, the approach does require higher inductance values at the source and the gate of the transistors. Large inductors, besides requiring more area than small inductors, also have a higher series parasitic resistance, R_s.

Like any other resistor, R_s will generate thermal noise and therefore the NF of the mixer-LNA circuit can be adversely affected. Therefore the gate and source inductors in these circuits must be minimized whenever possible. Another reason for preferring

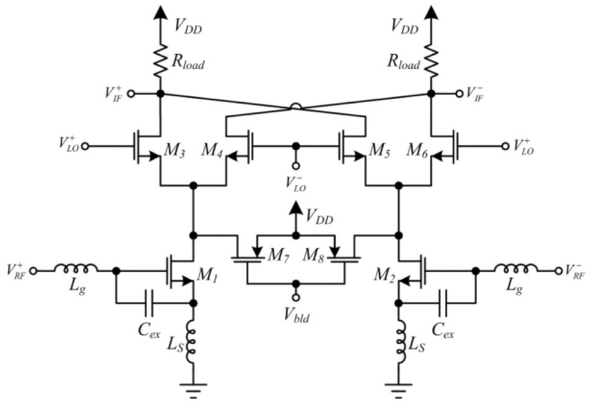

Figure 2. Improved low-noise mixer circuit

small inductors is that their quality, Q, is usually higher, which is follows from the expression

$$Q = \omega L / R_s \tag{4}$$

where L is the inductance and R_s is the series parasitic resistance. Of course, in cases where the increase in L is much larger than the relative increase in R_s then the Q can will be better for the large inductor compared to a smaller inductor, but the problem of the thermal noise contribution of R_s would still remain.

B. Current Bleeding Circuit

The LO switching transistor pairs (M_3/M_4 and M_5/M_6) are the load network of the low-noise RF transconductance stage that incorporates devices M_1 and M_2. In spite of using the PCSNIM technique, the RF stage still draws a moderately large amount of current. Therefore the LO switching pairs have to present a low-impedance load to M_1 and M_2 to prevent these devices from dipping into the triode region when large signals are incident at the RF port. To reduce the load impedance presented by the LO switching pairs usually requires a large drive voltage on the switches and that has the adverse effect of making them behave less ideally.

Since it is preferable that the current through the LO switches be small while the RF transconductors demand higher currents, we used a current bleeding circuit [14] in our design to meet these two competing demands. The bleeding circuit consists of transistors M_7 and M_8 in Figure 2 and it allows us to provide different bias currents through the RF transconductors and the LO switches.

Figure 3 shows a close-up of the current bleeding circuit. Because dc current flow in the mixer is from the switching core towards the RF transconductor stage, we note that

$$I_{RF} = I_{SW} + I_b \tag{5}$$

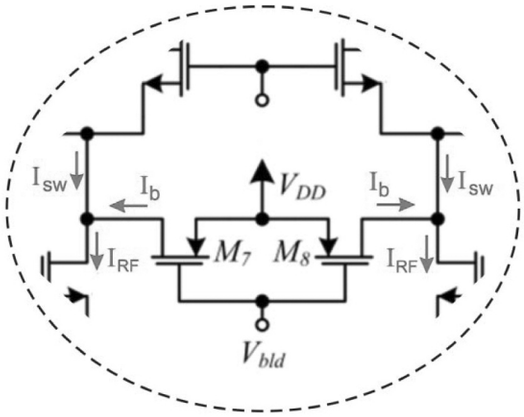

Figure 3. Close-up view of the current bleeding circuit from Fig. 2.

where I_{RF}, I_{SW}, and I_b are the dc current flows as drawn in Figure 3. The source terminals of M_7 and M_8 are tied to V_{DD} while their gates are tied together to a control voltage, V_{bld}, which regulates the current I_b. Depending on the value of V_{bld}, then I_b can go from a small current to a fairly large current thereby giving the designer a good amount of freedom to choose how much larger I_{RF} can be relative to I_{SW}.

The signal currents travel in the opposite direction of the dc currents shown in Figure 3 and, as a result, it is imperative that most of the RF signal enter the switching core instead of leaking out through the bleeding circuit. What is required, then, is for the current bleeding circuit to have a high input impedance looking in to the drain terminals of M_7 and M_8, and this is why PMOS devices were used here instead of NMOS devices.

In spite of the high input resistance of the PMOS devices, the bleeding circuit does have an impact on the mixer behaviour because a certain amount of signal current will still leak away through M_7 and M_8. An expression was derived in [5] for the output current of a basic mixer which takes into account the presence of the bleeding circuit,

$$i_{out} = \frac{R_{bld_{out}}[g_{m_{sw1}}(t) - g_{m_{sw2}}(t)]}{1 + R_{bld_{out}}[g_{m_{sw1}}(t) + g_{m_{sw2}}(t)]} \cdot i_{RF} \qquad (6)$$

where is the of the n[th] switch and is the output impedance of the bleeding circuit.

C. Complete Circuit

In this design, the PCSNIM technique is used in conjunction with the current-bleeding circuit. As mentioned before, this LNA design technique can reduce the current by having larger inductors. The LNA transistor is reduced to a point where high Q inductors can no longer be realized on chip at the frequency of interest. The current-bleeding circuit is then used to provide the extra current needed. The switching pairs are sized to reduce the switching rise time while keeping the tail capacitance low enough. The length of each transistor in the chip is 0.18 μm and while the gate widths were of different sizes, the devices were biased to obtain a current density of 0.13 mA/μm for optimal noise performance. For more information on why the 0.13 mA/μm was selected, the reader can consult [17].

For testing purposes, an on-chip buffer is integrated with the mixer to convert the differential output into a single-ended signal that drives a 50Ω instrument. The buffer is designed to have a 0 dB voltage gain so that the true conversion gain of the mixer can be measured. It is a differential amplifier with a current mirror load. Figure 4 shows the complete circuit of the low-noise mixer.

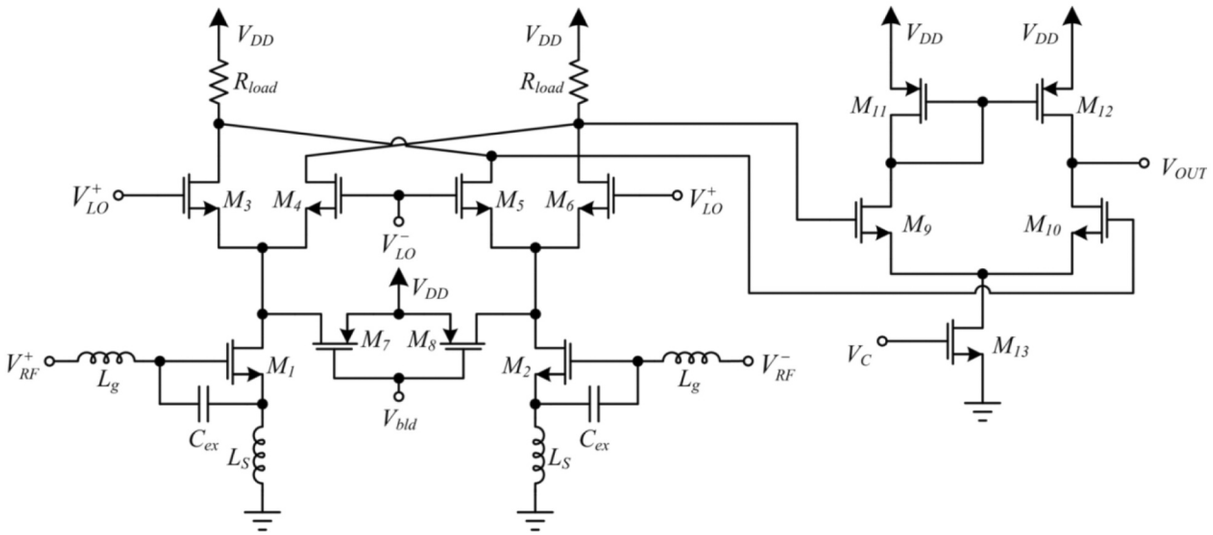

Figure 4. Complete low-noise mixer including output buffer.

D. Additional Noise Considerations

The relentless march towards smaller device feature sizes in CMOS makes the NF of radio-frequency integrated circuits (RFIC's) more sensitive to process variations. This can be seen from the fundamental NF equation for the case of a transistor amplifier, which is

$$F = F_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2 \quad (7)$$

The sensitivity of the noise figure is determined by the noise resistance, R_n, which is given by

$$R_n = \frac{\gamma g_{d0}}{g_m{}^2}, \quad (8)$$

where γ and g_{d0} are process-dependent parameters and g_m is the transconductance. Since g_m is inversely proportional to the gate-length of the transistors in the circuit, then it is clear from Eqns. (7) and (8) that the NF is strongly dependent on the transistor gate dimensions and, by extension, on any process variations.

The switching pairs also contribute noise. In [15], the output noise density due to one switch is given by

$$\overline{\left|i_{o,n}{}^2\right|} = 4kT\gamma\,\frac{I}{\pi A} \quad (9)$$

where γ is the channel noise factor, I is the bias current, and A is the LO amplitude. From (9), it is clear that the output noise density of the switches is proportional to the bias current and inversely proportional to the LO amplitude. The current-bleeding circuit can therefore reduce the thermal noise from the switches. With the current through the switches reduced, the size of the switches can be reduced, which reduces the tail capacitance. It can also have a smaller overdrive voltage so that a more ideal switching can be obtained such that it is more like a square wave. This would improve conversion gain because the conversion gain for non-perfect switching can be approximated by

$$A_V = g_m R_{load}\,\frac{2}{\pi}\,\frac{\sin\left(t_r/T\right)}{t_r/T} \quad (10)$$

where t_r is the rise time of the non-perfect square wave. The bleeding circuit thus serves multiple of purposes: supplies current to transconductors, allows the load resistance to increase, reduces thermal noise of switching pairs, and makes the switching more ideal to improve conversion gain.

4. EXPERIMENTAL RESULTS

The chip was fabricated using a standard 180 nm CMOS process. All of the inductors are on-chip and they were designed using the ASITIC software and verified with the full-wave field solver Momentum from Agilent Technologies. Furthermore, the RF input and output transmission lines were also simulated in Momentum in order to model the self inductance of the lines and other parasitics. The area for the low-noise mixer core is about 380 µm x 350 µm (0.133 mm²) and the total chip size including pads is 700 µm x 670 µm (0.469 mm²).

The low-noise mixer was designed at 5.4 GHz with a 300 MHz IF and a 5.1 GHz LO. All measurements were done on wafer with the use of two differential CPW probes and one GSG CPW probe for the single-ended IF output. The LO input power was set to 0 dBm. The RF power was swept and the output power of the mixer was measured using a spectrum analyzer.

Figure 5 shows the measured output power versus input power and the measured input-referred 1-dB compression point (IP_{1dB}) is -17.8 dBm, while the output-referred 1-dB compression point (OP_{1dB}) is -5 dBm.

To measure the third-order intercept point (IP3), a two-tone test was conducted with the signals separated by 1 MHz. Figure 6 shows the output

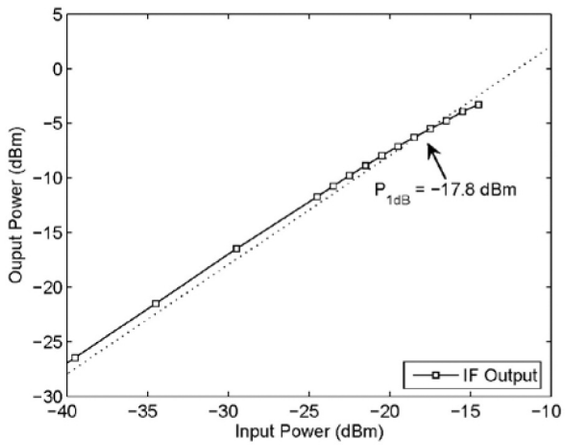

Figure 5. Measured IF output power versus RF input power.

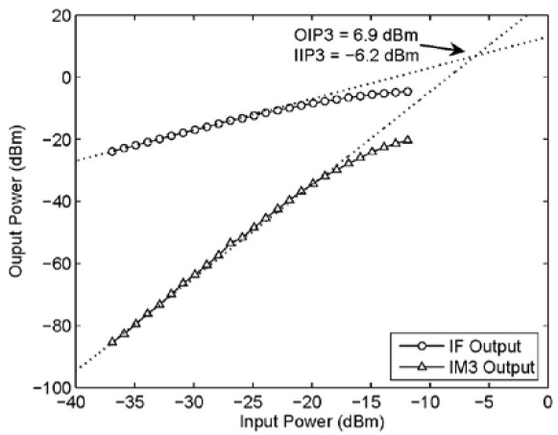

Figure 6. Measured and simulated conversion gain..

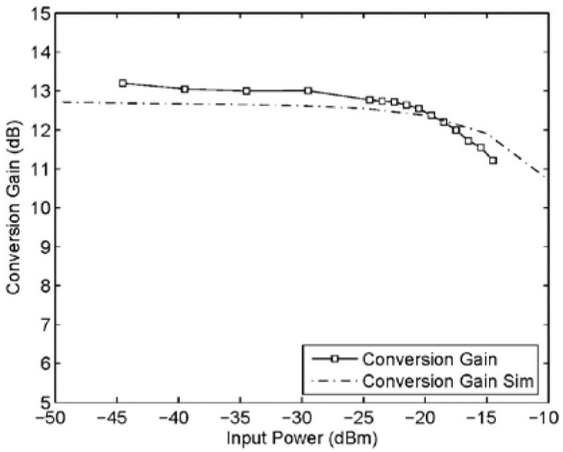

Figure 7. Measured and simulated conversion gain.

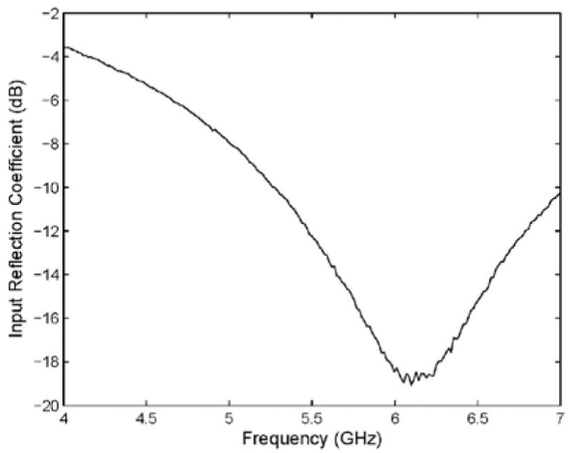

Figure 9. Measured reflection coefficient at the RF input port

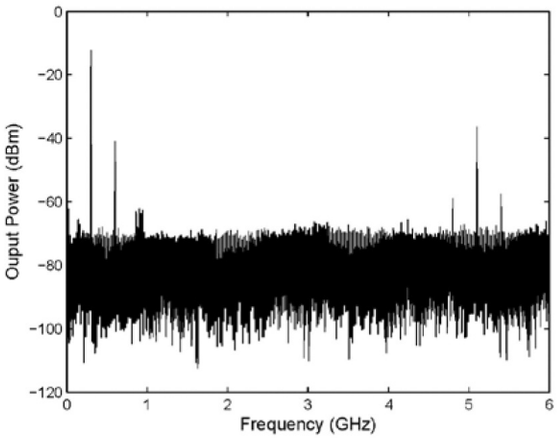

Figure 8. Figure 8. Measured output spectrum from 0 to 6 GHz with an input power of -25.5 dBm at 5.4 GHz and an LO power of 0 dBm at 5.1 GHz.

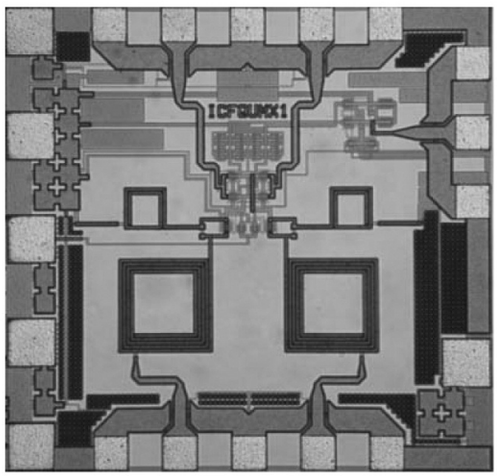

Figure 10. Microphotograph of the complete low-noise mixer chip.

spectrum in a two-tone test and includes both the measured IF and intermodulation output powers. The input-referred IP3 is -6.2 dBm and the output-referred IP3 is +6.9 dBm.

Figure 7 shows the measured conversion gain of the mixer to be 13.1 dB, which is very close to the simulated gain of 12.76 dB. The single-sideband (SSB) noise figure was measured and after de-embedding the loss and noise from the input balun, the SSB noise figure is found to be 7.8 dB. It should be noted that the noise from the buffer was included in the measurement. The SSB noise figure of the mixer block alone should thus be smaller than 7.8 dB.

Figure 8 shows the output spectrum from 0 to 6 GHz with a -25.5dBm of RF input power. The low LO-to-IF and RF-to-IF feedthroughs can be clearly seen in this plot.

A 2-port VNA was used to measure the input reflection coefficient. In order to find the differential S_{11}, a full 2-port measurement was first conducted for the input differential ports. Once the full 2-port data was recorded, (9) was used to find the equivalent differential S_{11} [16]

$$S_{dd11} = \frac{1}{2}(S_{11} - S_{21} - S_{12} + S_{22}). \qquad (11)$$

Shown in Figure 9 is the measured input reflection coefficient. Due to unwanted coupling between the gate inductors, the frequency for best match drifted upwards. Nevertheless, at 5.4 GHz, the measured S11 is -11.1 dB. Good port-to-port isolation was achieved by making the layout as symmetric as possible. The LO-to-RF feedthrough was measured, and it is -61.8 dB. The entire chip was biased from a single dc voltage power supply, VDD, of 2 V. No current mirrors were used on-chip.

The complete mixer including the output buffer consumes 31 mA, while the mixer core only consumes 18 mA of current. Figure 10 shows a microphotograph of the complete chip. A performance comparison with similar design topologies is shown in Table 1.

Table 1. Performance Comparison

Reference	CMOS Technology	Input Frequency (GHz)	Conversion Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	DC Power (mW)	Area (mm^2)	All Inductors On - Chip
[18]	0.35 μm	2.1	23 (Voltage)	3.2 (DSB)	-1.5	21.6	-	No
[19]	90 nm	0.1 - 3.85	12.1 (Power)	8.4 - 11.5 (SSB)	N/A	9.8	0.88 W/pads	Yes
This Work	0.18 μm	5.4	13.1 (Power)	7.8 (SSB)	-6.2	36 (core)	0.133	Yes

5. CONCLUSIONS

In this paper, a design guideline was proposed and a fully integrated low-noise mixer in 180 nm CMOS technology was presented. Both PCSNIM and current-bleeding techniques were used in the design to reduce the NF while having a reasonable gain. The mixer works at 5.4 GHz with a 300 MHz IF and has a power conversion gain of 13.1 dB, a low 7.8 dB SSB noise figure, and an IIP3 of -6.2 dBm. The mixer core itself only consumes 18 mA from a 2.0 V supply and the complete test circuit consumes 31 mA.

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