# Low power CMOS full adder design with body biasing approach

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**ABSTRACT**

In this paper, five different low power full adders using XOR/XNOR gates and multiplexer blocks with body biasing have been presented. In the first methodology, the adder depicts minimum power dissipation of 204.09μW and delay of 5.9849 ns. In the second, an improvement in power consumption has been reported at 128.92μW with delay of 5.9875 ns by using voltage biasing of two PMOS (P1 &P2) along with substrate biasing. In the third methodology, adder gives minimum power dissipation of 0.223nW with a delay of 5.2352 ns. Further, in fourth, it shows minimum power consumption of 0.199nW with a delay of 5.1002 ns and finally in fifth methodology, minimum power reduces to 0.192nW. Moreover, power delay product (PDP) results also have been compared for these methodologies. Comparisons have been made with earlier reported circuits and proposed circuits show better performance in terms of power consumption and delay.

**Index Terms:** Body bias, exclusive-OR (XOR), exclusive-NOR (XNOR), full adder design and low power.

## 1. INTRODUCTION

In recent years, power consumption in CMOS circuit has become major design consideration for very large-scale integration (VLSI) system. Growing demand of portable devices like cellular phones, notebooks, personal communication devices have aggressively enhanced attention for the low power consumption. In VLSI systems, power consumption includes dynamic power and static power consumption. Major portion of power consumption in any VLSI system consists of dynamic power consumption [1]. Moreover, the scaling trends of MOSFETs lead to the development towards nano-scale processes as driven by Moore law. With these developments the leakage currents are also increasing and the static power component of power dissipation is playing a vital role in the total power consumptions [2]. Static power is dissipated mainly due to the source and drain leakage currents and controlling the bulk terminal of CMOS device offers improved performance in term of power dissipation and delay. For obtaining low power consumption the transistor has to operate in sub-threshold region [3, 4].

An adder is a critical component in systems like processor, memory design, arithmetic logic unit (ALU) etc. and XOR/XNOR gates are the basic building blocks of these systems [5-12]. Therefore, careful design of these circuits improves the power consumption and other performance metrics of VLSI systems. In recent years different circuit techniques have been reported to improve the performance of XOR/XNOR gates. The XOR/XNOR gates with static CMOS pull–up PMOS & pull-down NMOS networks are the most conventional but require more transistors. A three input XOR circuit with least number of transistors and without requirements of complementary inputs was reported in [13]. Pass transistor logic (PTL) based 4 and 6-transistors XOR/XNOR circuits were presented in [14, 15] with degraded logic problems. Further, XOR and XNOR circuits called powerless XOR and groundless XNOR were reported in [16, 17]. Moreover, circuits using the transmission gates and inverter with better driving capability at the cost of power dissipation were reported in [18]. Circuits of XOR/XNOR with dual feedback network were reported in [19, 20]. Circuit level design optimizations are required for reducing the power consumption in CMOS circuits. Here, in this paper XOR/XNOR circuits [20] are modified with body biasing. Five different methodologies have been proposed with an inspiration to improve the power consumption of single bit full adder with reduced transistor counts.

The paper is organized as follows: in Section II body biasing technique has been applied to XOR/XNOR gates and the modified designs have been presented. Moreover, in this section, full adder circuits based on structured approach with these gates and multiplexer have been presented. Further, in section III results for the modified gates and full adders have been reported and a comparative analysis has been carried out. Finally, in Section IV conclusions have been drawn.

## 2. SYSTEM DESCRIPTION

Application of body bias to XOR/XNOR gates and full adder circuit reduces the power consumption by increasing the threshold voltage (V ) of individual transistor and thus reducing the leakage currents [3, 4]. The single bit full adder circuits have been designed with structured approach as shown in Figure 1 using XNOR/XOR gates and two multiplexer's.

Circuits have been designed with a gate length of 0.35µm for NMOS & PMOS transistors and the width of transistors has been taken as 1.0µm & 2.5µm for NMOS and PMOS respectively. These have been simulated in SPICE using TSMC 0.35µm model files with supply voltage of 3.3V. Different proposed methodologies are as follows:

### *A. Methodology: I*

In this methodology, a full adder has been designed using XOR/XNOR gates with forward feedback loops and the multiplexer blocks. All body terminals of PMOS are connected to 3.3V and body bias of [0 to -3.3] V has been applied to NMOS. Figure 2(a) shows schematic of XOR/XNOR gate and Figure 2(b) illustrates the circuit diagram of full adder using body biasing.

### *B. Methodology: II*

In this methodology [Figure 3(a)], an additional voltage bias has been applied to PMOS transistors (P1 & P2) of the XOR/XNOR gates, instead of ground as in Figure 2(a). The voltage bias (V3) of transistors P1 & P2 has been varied from [0 to 3.3] V. The substrate bias of 3.3 and -3.3V has been applied

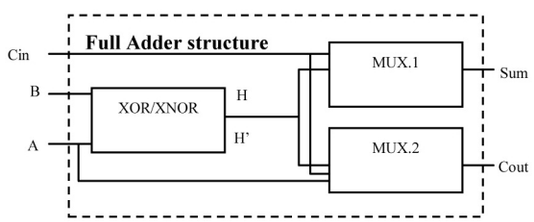


**Figure 1.** Structure of single bit full adder

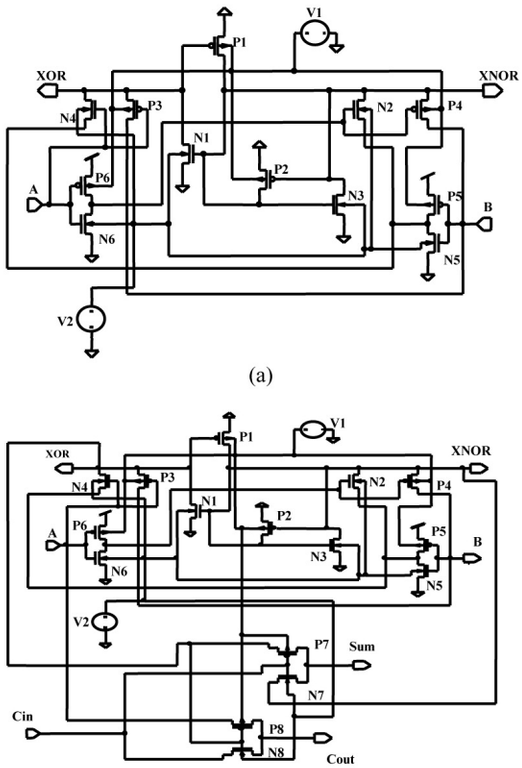


**Figure 2.** Circuits with body bias (a) XOR/XNOR gate (b) Full adder

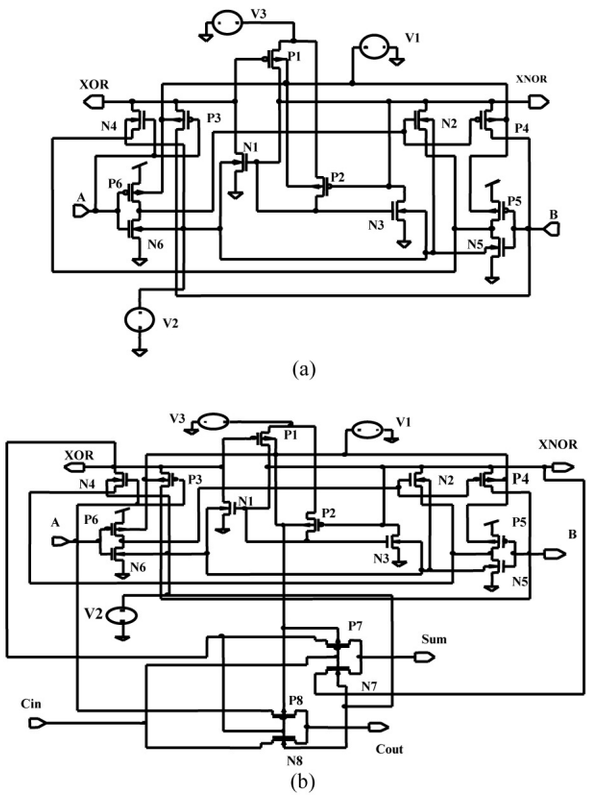


**Figure 3.** Circuits with an additional biasing of P1 & P2 (a) XOR/XNOR (b) Full adder

to PMOS & NMOS transistors respectively. Further, this XOR/XNOR gate has been incorporated to design a full adder using two multiplexer as shown in Figure 3(b).

### *C. Methodology: III*

XNOR portion is the major source of power consumption in previous methodology. Here, in Figure 4(a), XNOR portion has been eliminated and its operation has been achieved by adding an inverter. The body bias voltage, varying from [0 to -3.3] V and fixed bias of 3.3V have been applied to NMOS & PMOS transistors respectively. Figure 4(b) shows a full adder by using the circuit mentioned in Figure 4(a).

### *D. Methodology: IV*

Here, a full adder as shown in Figure 5(a) has been designed using XOR gate and two multiplexers along with additional inverter (required for Cin complemented signal). Here, the XNOR portion has been eliminated at the cost of one additional inverter because it shows large power consumption. Body biasing of 3.3V has been applied to all the PMOS transistors whereas body bias of NMOS has been varied from [0 to 3.3V].

### *E. Methodology: V*

In this methodology, an additional voltage bias to PMOS transistors (P1& P2) along with the substrate bias has been applied to full adder circuit designed in previous methodology. For minimum power consumption, NMOS & PMOS substrate biases have been fixed at -1.0 & 3.3V respectively. The voltage biasing of PMOS transistors (P1&P2) has been varied from [0 to 0.8] V as shown in Figure 5(b).

## 3. RESULTS AND DISCUSSIONS

Simulation results of the XOR/XNOR gate and full adder without body bias shows power consumption of 939.15µW & 946.99µW respectively. Table I and Table II shows simulations results of the methodologies I to V with different biasing conditions. Result shows that the power dissipation has been reduced significantly with the application of biasing in all the proposed methodologies with very small conciliation in delay. The power consumption has been reduced due increased threshold voltage and the subsequent reduction in sub threshold leakages currents of transistors. In methodology-I, minimum power consumption 204.07µW for XOR/XNOR and 204.09 µW for the full adder has been achieved at the bias voltage of 3.3V for PMOS and -3.3 V for NMOS transistors. The output delay for adder is varying from [5.1120 - 5.9849] ns with variation in the bias voltage from [0 to -3.3] V. At the bias voltage of -3.3V power consumption is lowest i.e. 204.09µW for adder with maximum output

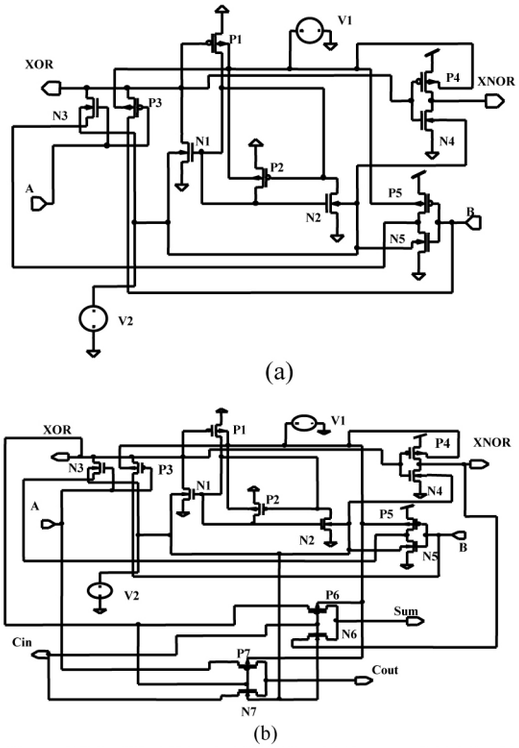


**Figure 4.** Modified Circuit (a) XOR with inverter (b) Full adder

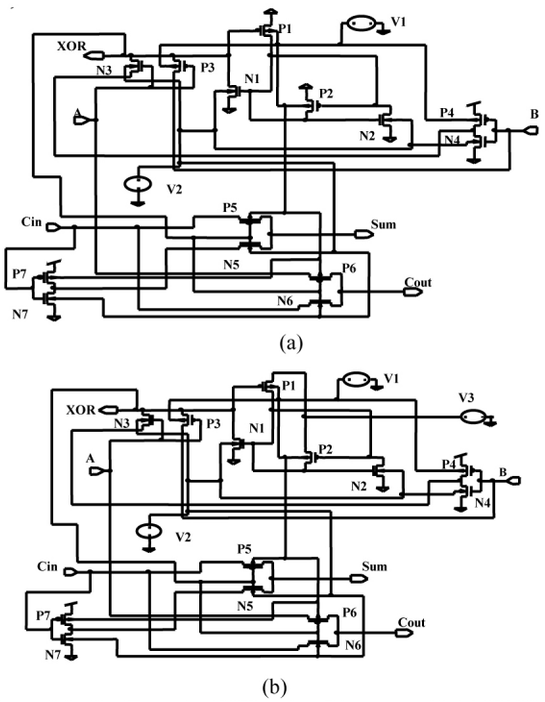


**Figure 5.** Full adder using XOR and multiplexers with (a) NMOS & PMOS body bias (b) additional voltage biasing of P1 &P2

delay of 5.9849 ns. The power delay product (PDP) shows deviation from [2501.55 - 1221.45] fJ with variation bias voltage from [0 to -3.3] V. It has been observed from Table-III that methodology I shows significant improvement in PDP with the body bias. Results for methodology-II [Figure 3] shows that the power consumption decrease with increase in the bias voltage up to 1.5V and further it increase. Additional biasing of P1 and P2 reduces the flow of leakages currents to ground and power consumption is reduced. With further increase in bias voltage above 1.5V, benefits of biasing vanished and the power consumption increases due to high bias voltage as it directly affects power consumption.

**Table I.** Power Consumption Comparisons of Proposed Methodologies with Body Bias

| Methodology-I | | | Methodology-II | | | Methodology-III | | | Methodology-IV | | Methodology-V | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NMOS body bias (V) | XOR/XNOR power (µW) | Full adder power (µW) | P1 and P2 Bias (V) | XOR/XNOR power (µW) | Full adder power (µW) | NMOS body bias (V) | XOR/XNOR power (µW) | Full adder power (µW) | NMOS body bias (V) | Full adder power (nW) | P1 and P2 bias (V) | Full adder power (nW) |
| 0 | 481.11 | 489.35 | 0 | 204.09 | 204.10 | 0 | 1.24 | 1.39 | 0 | 0.845 | 0.0 | 0.199 |
| -0.5 | 431.25 | 431.37 | 0.5 | 178.83 | 178.85 | -0.5 | 0.201 | 0.516 | -0.5 | 0.230 | 0.1 | 0.197 |
| -1.0 | 380.37 | 380.44 | 1.0 | 155.53 | 155.57 | -1.0 | 0.136 | 0.234 | -1.0 | 0.199 | 0.2 | 0.196 |
| -1.5 | 334.92 | 334.95 | 1.5 | 128.89 | 128.92 | -1.5 | 0.151 | 0.223 | -1.5 | 0.222 | 0.3 | 0.195 |
| -2.0 | 293.85 | 293.87 | 2.0 | 155.98 | 156.01 | -2.0 | 0.177 | 0.259 | -2.0 | 0.259 | 0.5 | 0.193 |
| -2.5 | 256.55 | 256.57 | 2.5 | 334.03 | 334.03 | -2.5 | 0.209 | 0.304 | -2.5 | 0.304 | 0.6 | 0.192 |
| -3.0 | 222.72 | 222.74 | 3.0 | 633.40 | 633.65 | -3.0 | 0.246 | 0.356 | -3.0 | 0.356 | 0.7 | 0.206 |
| -3.3 | 204.07 | 204.09 | 3.3 | 862.02 | 862.03 | -3.3 | 0.271 | 0.391 | -3.3 | 0.391 | 0.8 | 0.781 |

**Table II.** Delay Comparisons of Proposed Methodologies with Body Bias

| Methodology-I | | Methodology-II | | Methodology-III | | Methodology-IV | | Methodology-V | |
|---|---|---|---|---|---|---|---|---|---|
| NMOS body bias (V) | Maximum output delay of full adder (ns) | 1 and P2 Bias Volt-age(V) | Maximum output delay of full ad-der (ns) | NMOS body bias voltage(V) | Maximum output delay of full adder (ns) | MOS body bias volt-age(V) | Maximum output de-lay of full adder (ns) | P1 and P2 bias volt-age(V) | Maxi-mum output delay of full adder (ns)r |
| 0 | 5.1120 | 0 | 5.9847 | 0 | 5.0928 | 0 | 5.0635 | 0.0 | 5.1002 |
| -0.5 | 5.1457 | 0.5 | 5.9854 | -0.5 | 5.1285 | -0.5 | 5.0773 | 0.1 | 5.1002 |
| -1.0 | 5.1833 | 1.0 | 5.9859 | -1.0 | 5.17212 | -1.0 | 5.1002 | 0.2 | 5.1002 |
| -1.5 | 5.2293 | 1.5 | 5.9875 | -1.5 | 5.2352 | -1.5 | 5.1355 | 0.3 | 5.1002 |
| -2.0 | 5.298 | 2.0 | 6.0191 | -2.0 | 5.3361 | -2.0 | 5.1889 | 0.5 | 5.1002 |
| -2.5 | 5.4195 | 2.5 | 10.1072 | -2.5 | 5.51078 | -2.5 | 5.2807 | 0.6 | 5.1002 |
| -3.0 | 5.6727 | 3.0 | 10.0236 | -3.0 | 5.9223 | -3.0 | 5.4896 | 0.7 | 5.1002 |
| -3.3 | 5.9849 | 3.3 | 10.0251 | -3.3 | 6.4337 | -3.3 | 5.7412 | 0.8 | 5.1001 |

**Table III.** Power Delay Product Comparisons of Proposed Methodologies with Body Bias

| Methodology-I | | Methodology-II | | Methodology-III | | Methodology-IV | | Methodology-V | |
|---|---|---|---|---|---|---|---|---|---|
| NMOS body bias (V) | Power delay product (fJ) | P1 and P2 Bias Voltage (V) | Power delay product (fJ) | NMOS body bias voltage (V) | Power delay product (fJ) | NMOS body bias voltage (V) | Power delay product (fJ) | P1 and P2 bias voltage (V) | Power delay product (fJ) |
| 0 | 2501.55 | 0 | 1221.47 | 0 | 0.00707 | 0 | 0.00427 | 0.0 | 0.00101 |
| -0.5 | 2219.70 | 0.5 | 1070.48 | -0.5 | 0.00264 | -0.5 | 0.00116 | 0.1 | 0.00100 |
| -1.0 | 1971.93 | 1.0 | 931.22 | -1.0 | 0.00121 | -1.0 | 0.00101 | 0.2 | 0.00099 |
| -1.5 | 1751.55 | 1.5 | 771.90 | -1.5 | 0.00116 | -1.5 | 0.00114 | 0.3 | 0.00099 |
| -2.0 | 1556.92 | 2.0 | 939.03 | -2.0 | 0.00138 | -2.0 | 0.00134 | 0.5 | 0.00984 |
| -2.5 | 1390.48 | 2.5 | 3376.10 | -2.5 | 0.00167 | -2.5 | 0.00160 | 0.6 | 0.00979 |
| -3.0 | 1263.53 | 3.0 | 6351.45 | -3.0 | 0.00210 | -3.0 | 0.00195 | 0.7 | 0.00105 |
| -3.3 | 1221.45 | 3.3 | 8641.93 | -3.3 | 0.00251 | -3.3 | 0.00224 | 0.8 | 0.00398 |

Minimum power consumption of 128.89μW for the XOR/XNOR and 128.92μW for the full adder has been reported at a bias voltage of 1.5V for PMOS (P1 &P2). Here, by using the additional bias of P1& P2, improvements in power consumption from [204.09 to 128.89] μW for XOR/XNOR gate and [204.10 to 128.92] μW for full adder have been achieved. Table II shows that the delay for adder varies from [5.9847 - 10.0251] ns with variation in bias voltage of P1, P2 transistors from [0 to 3.3] V. With the bias voltage of 1.5 V for P1, P2, power consumption is minimum i.e 128.92μW for adder having the delay of 5.9875 ns. Table III shows PDP is significantly improved and shows deviation from [1221.47 - 8641.93] fJ with bias variation of P1 & P2 from [0 - 3.3] V.

Simulation results of the XOR/XNOR gate and full adder as mentioned in methodology III [Figure 4] shows that the power consumptions reduces stridently with NMOS body bias due to reduction in leakage current through increased threshold voltage of transistors. It has been observed that there is a little effect on the power consumption beyond -1.0V NMOS biasing. Here, the minimum power consumption of 0.136nW for XOR/XNOR module with body bias of -1.0V for NMOS and 3.3V for PMOS has been obtained. Full adder with the modified XOR/XNOR shows minimum power consumption of 0.223nW with body bias of -1.5V for NMOS and 3.3V for PMOS transistors. The output delay shows variation from [5.0928 - 6.4337] ns with varying NMOS bias from [0 to -3.3] V. The delay is marginally increased but the overall PDP has been improved and shows variation [0.00707 - 0.00251] fJ.

For methodology IV [Figure 5(a)] the power consumptions diminish rapidly with NMOS body bias and shows small effects beyond -1.0V. Minimum power consumption of 0.199nW has been achieved with body bias of 3.3V for PMOS and -1.0V for NMOS transistors. Table II shows that the output delay varies from [5.0635 - 5.7412] ns with varying bias of [0 to - 3.3] V to NMOS transistors. There is little increase in delay with the overall improvement in PDP which shows variation from [0.00427-0.00224] fJ.

In methodology V [Figure 5(b)] the power consumption varies from [0.199 - 0.781] nW by varying the voltage bias of PMOS (P1 & P2) from [0 to 0.8] V. Here, minimum power consumption of 0.192nW for full adder has been obtained at bias voltage of 0.6V for P1 & P2. It has been observed from Table II that the output delay is almost constant with value of 5.1002 ns in this methodology. PDP has been improved and varies from [0.00101 - 0.00398] fJ as shown in Table III.

A comparative study of proposed and earlier reported adders has been given in Table IV. It has been shown that circuits proposed in methodology III, IV and V show lesser power consumption than earlier reported full adders. Methodology I and II also depict better performance than earlier reported adders using 10, 16 and 20 transistors. Methodology I-IV also shows an improvement in output delay as compared to 10 transistors SERF [11], pass transistor logic-14T [8] and transmission function-16T adder [7]. Methodology V shows better performance among all as XNOR portion has been eliminated and adder has been designed with XOR gate only with reduced leakage current. Here, in addition to substrate biasing, bias voltage has also been applied to P1 & P2 transistor which further reduces the leakage currents. On the other hand methodology I show worst performance due to existence of XNOR portion that adds to leakage currents.

In reported work, power efficient adders have been designed with different combination of XOR/XNOR gates and multiplexer concept. Power consumption has been reduced with reverse body bias and simple voltage biasing of transistors. Reverse body biasing technique provides the way to reduce power consumption without any extra hardware on circuit. This paper extend the concept of body bias for optimized adder design and shows that proper selection of bias voltage affects the power consumption & overall performance of system.

**Table IV.** Power Consumption Comparisons (TSMC 0.35μm, Supply Voltage: 3.3V)

| Full Adder configuration | Power Consumption | Output delay |
|---|---|---|
| Conventional 28 transistors [10] | 1.26nW | 2.112 ns |
| Transmission gate 20 transistors [6] | 1.25mW | 4.966 ns |
| Transmission function 16 transistors [7] | 1.24nW | 25.01 ns |
| Pass transistor 16 transistors adder [9] | 591.11μW | 4.982 ns |
| Pass transistor 14 transistors adder [8] | 0.626nW | 10.107 ns |
| 10 transistors SERF adder [11] | 531.29μW | 9.960 ns |
| Methodology-I with 14 transistors [ present work] | 204.09μW | 5.984 ns |
| Methodology-II with 14 transistors [ present work] | 128.92μW | 5.987 ns |
| Methodology-III with 14 transistors [ present work] | 0.223nW | 5.235 ns |
| Methodology-IV with 14 transistors [present work] | 0.199nW | 5.100 ns |
| Methodology-V with 14 transistors [present work] | 0.192nW | 5.100 ns |

## 4. CONCLUSIONS

The full adder circuits using XOR/XNOR gate (dual feedback) and multiplexer blocks using body bias have been proposed. Compared with earlier reported circuit, proposed full adder circuits show less power consumption and delay with reduced transistor count in different methodologies. PDP in first methodology shows improvement from [2501.55 - 1221.45] fJ by body biasing. Further additional biasing of two PMOS (P1 & P2) shows improvement in power consumption from [204.07 to 128.89] μW for XOR/XNOR and [204.09 to128.92] μW for full adder. In Methodology-II PDP shows variation from [1221.47 - 8641.93] fJ with minimum value of 771.90 fJ at 1.5V. The full adder designed with elimination of XNOR portion provides minimum power dissipation of 0.223nW with PDP of 0.00116 fJ. Full adder designed with only XOR gate and multiplexer block using body biasing shows minimum power consumption of 0.199nW with PDP of 0.00101 fJ. Further power consumption has been minimized up to 0.192nW with PDP of 0.00979 fJ in methodology-V by biasing two PMOS (P1 & P2) transistors along with body bias.

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