Design Methodology and Practical Aspects of a 9-Bit Continuous-Time Sigma-Delta A/D Converter

Sumit Bagga, Jose C. da Costa, Adson F. da Rocha and Leonardo R. A. X. de Menezes
sums1@hotmail.com
{camargo, adson, leonardo}@ene.unb.br

Universidade de Brasília - UnB
Departamento de Engenharia Eletrica, Faculdade de Tecnologia – FT
Cx. Postal 4386 Brasilia - DF - Brazil - 70919-970

Abstract

This research of a first-order sigma-delta (ΣΔ) converter is being conducted because it is a part of an integrated system-on-chip (SOC) called UnB-2001. This chip, once fabricated will have both a processor and RF section on it. The discussion begins with a variety metrics used to evaluate modulator performance with emphasis on those that are important for physical variable sensing and RF applications. Furthermore, the fundamental power limits and area restrictions for sigma-delta converters will be illustrated using continuous-time as opposed to switched capacitor mode. Thus, an experimental prototype with a resolution of 9-bits can be implemented in CMOS technology, having clock fs of 20MHz, an oversampling ratio of 100, and supply voltage of +/- 3.3V

1 Introduction

Sigma-delta modulation techniques have been very successfully used in analog-to-digital conversion (ADC) applications over the last two decades. However, the purpose of ΣΔ modulators is to trade higher sampling speed (i.e., higher f_s) for obtaining higher resolution. [NAD 94]

The design of the converter presented in this study takes these issues into consideration by avoiding the use of SC networks and of operational amplifiers: it relies on the gain of the system loop to achieve the required linearity: it also employs a linear (rather than switched) l-bit DAC to eliminate the dynamic noise generated by the switching. [COM 91]

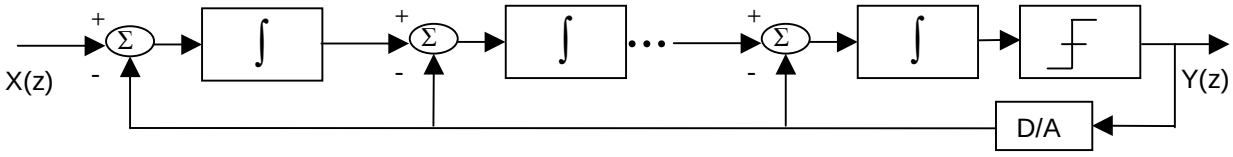

Figure 1 - Sigma-delta modulator block diagram.

2 Basic Concepts

The series of integrators are situated in the forward path of the sigma-delta modulator, and feedback loop contains the quantizer and can be observed in Fig. 1. The input for each integrator is the difference between the D/A converter output and the previous integrator output. The feedback loop is responsible in bringing the average value at the first integrator input to zero. Thus, the input signal X(z) is equal to the output of the D/A converter. Since

the output of the D/A converter is simply an analog representation of the digital output Y(z) of the quantizer, we can now state that Y(z) is equal to input signal, X(z).

For oversampling, modulator samples the input analog signal at a higher rate than required by the Nyquist sampling frequency. Because of this, multiple samples are averaged to produce a digital output Y(z). Hence, our sigma-delta modulator can then be used as an oversampled A/D converter. [TEM 93]

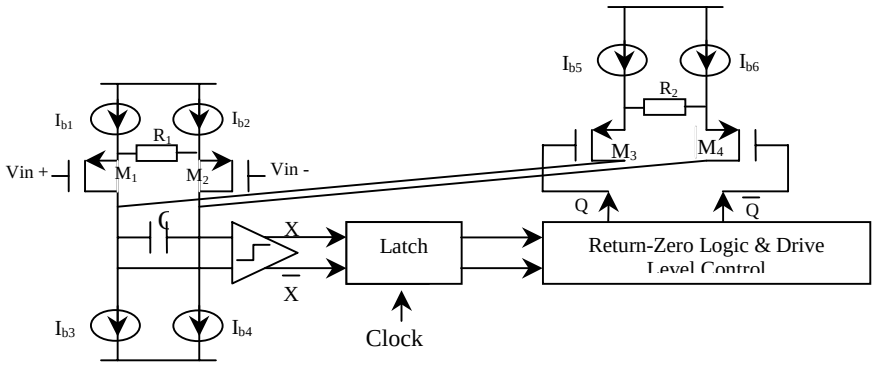

Figure 2 – Sigma-delta modulator architecture.

3 System Design

3.1 The Digital Block for the ΣΔ Converter

The architecture of the ΣΔ modulator is illustrated in Fig. 2. It is a differential structure. [TEM 92]

3.1.1 The Operational Transconductance Amplifier (OTA)

The OTA can be considered as an integrator that drives the floating capacitor *C*. The current sources $I_{bl} - I_{b4}$, transistors M_l and M_2, and resistor R_1 make up the OTA. The analog input signal is initially converted into a current, and then the capacitor integrates this current. The capacitor limits he speed of the integrator and is responsible for generating the dominant pole.

3.1.2 The D/A Converter

This block consists of a second differential pair (transistors M_3 and M_4) that is matched to the input differential pair. The system feedback loop closes at the nodes of the capacitor (terminals). The DAC injects current pulses at these nodes of the integrating capacitor. To maintain M_3 and M_4 in saturation, signals Q and Q (inverted) are generated by the driver level control block (DLCB). They are square waves of limited amplitude. Because of this, the differential pair continues to operate within the linear region and this guarantees a high switching speed.

3.1.3 The Quantizer

A comparator and a latch make-up the quantizer. The latch drives the Drive Level Control Block (DLCB).

3.2 Reasons for Implementation and Features

Why was the sigma-delta converter chosen? [KIN 98]

One of the key aspects in choosing a sigma-delta analog-to-digital converter is the reduction in analog block requirements. In addition, the design of the anti-alias filter is easily

calculated. Simultaneously, no sample and hold circuit is mandatory and it can be easily re-drawn for a new technology. One more factor is that it uses a low voltage power supply.

3.2.1 Improving the Linearity of the ΣΔ Loop

The feedback loop offers certain advantages towards improving the linearity of the sigma-delta converter, such as shaping the *quantization noise* and reducing the total harmonic distortion. Distortion can be well controlled, even though the differential stage is the only input block outside the loop. The quantizer is in the forward path of the feedback loop to maximise linearity.

3.2.2 Absence of Feedback Amplifiers

With the absence of feedback amplifiers, difficulties such as, frequency compensation and reducing the settling time are avoided.

3.2.3 D/A Conversion (linear)

Besides having ideal linearity, the single-bit D/A converter has a tendency to generate spikes in its output, when switching from one level to another. Furthermore, additional noise that degrades the SNR of the overall system, could be a result of these dynamic irregularities. One way to remove this problem would be to allow transconductor stage to operate in the linear region.

3.2.4 Differential Block

Since we are employing a limited power supply, a differential structure was chosen for the entire system. Better power supply rejection, greater noise immunity, and less distortion were also other parameters taken into consideration when choosing this differential circuitry.

4 Analysis of Micropower CMOS Temperature Sensor

Instruments typically measure physical variables such as temperature, weight, gas concentration and chemical balance. Such variables tend to change gradually and over a long period of time creating specific requirements for the system A/D converter. One typical application of the sigma-delta converter is, the CMOS smart temperature sensor. Obviously a number of design parameters would require change, such as the sampling rate. Once again, because of lower complexity in design and die area restrictions, the first order sigma-delta converter was taken into account. The analog input signal for this application is < 2Hz. Cost effective, high-performance temperature sensors are becoming popular for the following applications: [BAK 96]

- to control the dissipation on VLSI chips
- in strongly automated production plants
- in consumer products like cars and home appliances

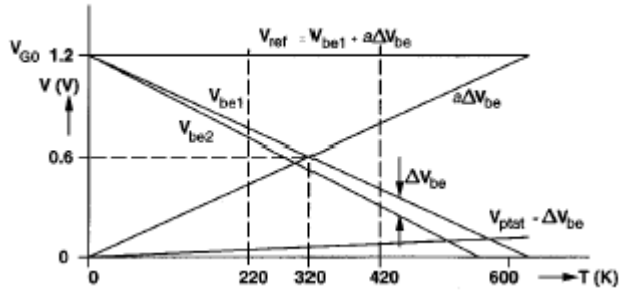

Figure 3 - Derivation of V_{ptat} and V_{ref} .

4.1 System Design: Derivation of Temperature and Reference Signals

The vertical bipolar substrate transistor seems to be the best candidate for integrated temperature sensors. To derive the temperature and reference signals from bipolar transistors has been shown in Fig. 3. We can clearly see that the base-emitter voltage (V_{be}) of the transistor is inversely proportional to the temperature. The temperature coefficient is dependent on the emitter current density and is approximately -2 mV/^{o}C. The difference between two base-emitter voltages $\bullet V_{be}$ can be written as (Eq. 1)

$$V_{ptat}(T) = (kT / q).(\ln(p)) \qquad \text{Eq. 1}$$

where p is the emitter current density ratio, k is Boltzmann's constant, and q is the electron charge. When p=8, the temperature coefficient of this PTAT voltage is 0.2mV/^{o}C. The bandgap reference voltage is given by the following equation:

$$V_{ref} = V_{be1} + a \bullet V_{be} \qquad \text{Eq. 2}$$

4.2 Calibration

To control the entire process, a microprocessor is needed. Thus, it will be less expensive to implement the calibration facility and maybe a BIST (Built in System Test) in this microprocessor than to perform a digital calibration on the chip.

5 Limitations of the Sigma-Delta Approach and *what may lie ahead*

Local loop - speed limitation; Stability; Clock jitter;
Power consumption, area;

1. Promising approach for high- speed medium- resolution converters for next technologies and low voltage;
2. Interesting alternative to switched- capacitor modulator;
3. Wireless/ cordless phones, pagers.

6 Conclusion

A study for a first-order ΣΔ converter was discussed. It has the advantages offered by a continuous-time structure without feedback amplifiers: high speed, simplicity, and small area. Furthermore, given the absence of operational amplifiers, a high linearity is more difficult to achieve. Implementing a temperature sensor with the sigma delta converter was also studied. An integrated sigma delta A/D converter prototype based on this principle will be designed, fabricated, and tested. Its performance will then confirm the validity of the theoretical assumptions.

7 References

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