# Wireless Comunication System in a Single Chip - Transceiver

**Alessandro Benevenuto, José C. da Costa, Adson Rocha, Leonardo Menezes**
**abenevenuto@uol.com.br**
**{camargo,adson,leonardo}@ene.unb.br**

Universidade de Brasília – UnB
Departamento de Engenharia Elétrica – LPCI (Lab. de Proj. de Circuitos Integrados)
Caixa Postal 4386 – Brasília – DF – 70919-970

***Abstract***

*This study presents some of the fundamental characteristics of the transceiver used in a wireless communication system in a single chip. The article discuss the major characteristics of the blocks used in construction of the RF section of the chip (transceiver) and presents a minimal topology.*

## 1 The RF System

The principle characteristics and specifications of the transceiver are illustrated in Table 1. They were established on the basis of the projects requirements. The objectives of this section are that it will operate in the ISM (Industrial, Scientific and Medical) band, optimum usage of the spectrum, MSK modulation, power control of the output stage (6 bits – 36dB), low energy consumption and finally size restrictions. Figure 1. Demonstrates a block diagram of the RF System.

**Table1: RF System Characteristics.**

| | |
|---|---|
| **Operating Frequency** | **902-928 MHz** |
| **Modulation techniques used** | **MSK and FSK** |
| **Technology** | **FDMA** |
| **Output Power** | **100 mW** |
| **Output Swing** | **36 dB (6 bits)** |
| **Receiver** | **Direct Conversion** |
| **Local Oscillator** | **PLL - XTAL** |
| **Bandwidth** | **128 Kbps** |
| **Supply Voltage** | **3,3 V** |
| **Output Impedance** | **50 Ω** |

The topology was realized taking into consideration the restrictions in size of the integrated circuit. Because of this limitation, it is preferred to generate the signals for transmission directly in the band without the use of upconversion. The main blocks for the transmitter are as follows:

***Local oscillator:*** it is a ring oscillator, formed by using CMOS inverters with a crystal resonator in the feedback loop, generating a square wave with an operating frequency of 33 MHz.

***Frequency Synthesizer:*** it generates 3 fundamental frequencies that are used by the RF system; the receiver utilizes fo when downconverting, $f_1$ and $f_2$ being used in the MSK or FSK modulation and not needing upconversion methods. The frequency synthesizer is constructed with the use of a PLL circuit. The PLL has the ability to select any of the 3 frequencies ($f_1$, $f_2$ e $f_0$) by allocating a binary word to the individual I/O ports, where the frequencies reside. Joining this block with that of the RF Amplifier would occupy maximum area space.

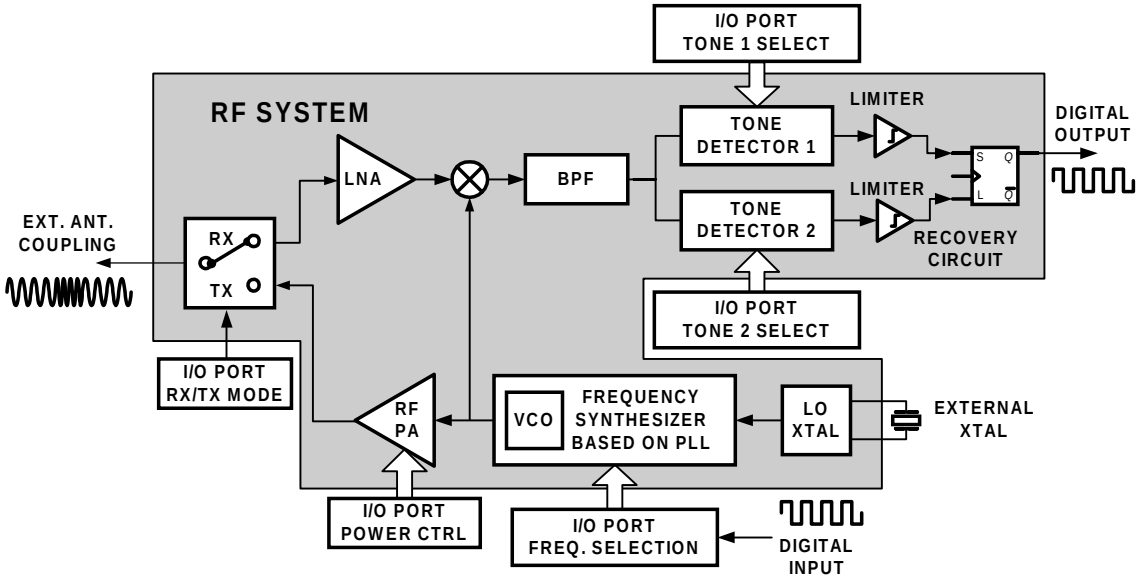


**Figure 1 - Diagram for the RF System.**

***RF Amplifier:*** It operates in the E class thus having moderate linearity, and it demonstrates good power efficiency. These characteristics make it appropriate to use and since the project are incorporating MSK and FSK modulation techniques, the linearity makes little to no difference. The power control is realized by the use of a 6 bit binary word, which loads in it the information of the reserved I/O. This results in a output swing of 36 dB of the amplifier.

Like the TX, RX can be run efficiently by minimizing the required occupied area and by reducing the power consumption. The direct conversion technique was chosen by taking into consideration the statements scripted above. The blocks of the receiver's sub-system are as follows:

***LNA:*** This is the most complex stage of the receiver. It registers a uniform gain in the entire bandwidth (902 – 928 MHz) and also we can expect a sensitivity of about 1μV with a power consumption of 10 mA and a supply voltage of 3,3 V.

***Downconverter:*** An extremely simple segment to comprehend. Basically consisting of a transmission gate, where we may apply a sampling signal to the control terminal and then it is followed by a passive low-pass filter stage.

***Tone Detectors:*** The signal obtained at the output of the passive low-pass filter is applied to 2 tone detectors that are constructed by PLLs. The tone maybe programmed through the use of

binary words, corresponding to the frequencies $f_1$ and $f_2$, which are MSK modulated. The binary words reach the tone detectors by passing through the processor specified, 2 I/O ports.

***Signal Recuperation Circuit:*** The signals leaving the output of the tone detectors are then used as inputs to the limiters circuits to condition the signal and then they are sent to a structure similar to a flip flop, which is used to detect and then recuperate the original signal.

***Interfacing the RF System and μ-processor:*** As shown above the interface and control of RF blocks use I/O ports of μ-processor. At all there are (08) I/O ports – 03 for storage of the binary words corresponding to fundamental frequencies used by RX/TX, 01 to adjust the power of transmission and 02 for selecting the tones of tone detectors. There are two more I/O ports – one dedicated to serial communication with a UART and other to select transmission mode or receiving mode.

All the inductors that will come to use can be calculated using Modified Wheeler's method. It has guard rings and polysilicon ground patterned shield with the proper grounding. The placement of the inductors was projected to minimize mutual and well coupling.

## 2 Conclusion

In this paper was proposed topology for a transceiver to be used as a part of the wireless system in a single chip. This topology was take in mind mainly the limited space required to implement all chip and electromagnetic compatibility with the other sections.

## 3 References

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