Testing Sigma-Delta Modulators Using Oscillation-based Test Method

F. P. Cortes, A. Girardi, J. Choi, M. Lubaszewski, S. Bampi
{girardi, fpcortes, choi, luba, bampi}@inf.ufrgs.br

Universidade Federal do Rio Grande do Sul - UFRGS / Instituto de Informática
Cx. Postal 15064 - Av. Bento Gonçalves, 9500 - Campus do Vale - Bloco IV
Bairro Agronomia - Porto Alegre - RS - Brasil - 91501-970

Abstract

This paper presents the development of an oscillation-based test circuit to a sigma-delta A/D modulator. During the test mode, the sigma-delta modulator is configured as an oscillator and the natural oscillation frequency is measured. The validity of the proposed test method is verified throughout electrical simulations of faults and sensitivity analysis.

1. Introduction

Testing analog and mixed-signal circuits can be accomplished in several ways, such as functional testing, DC testing, power-supply quiescent current monitoring and digital signal processing (DSP) techniques. These techniques are employed during the design phase, increasing the controllability and observability. The effectiveness of these techniques depends on the selection of suitable test vectors, when the complexity of the circuit under test (CUT) increases the problem of generating optimal test vectors assuring high fault coverage becomes critical. Built-in self-test structures based on these methods require the use of specialized input stimulus generation and output evaluation hardware which introduce a significant increase of silicon area. To overcome some above-mentioned problems, several papers discuss the oscillation-based test concept [ARA97][HAS98][HUE99], that can be used either in off-line testing or as the core of the so-called OBIST (Oscillation-based Built-In-Self-Test). Herein, these techniques are applied for sigma-delta A/D modulator testing and will be described on the following sections.

2. The oscillation-based test method

This test method, developed in [ARA97] is based on the partitioning of the analog circuit under test into functional building blocks or a combination of these blocks. During the test mode, each building block is converted to a circuit that oscillates. The oscillation frequency f_{osc} of each building block can be expressed as a function of its components or performances. The building blocks that generate inherently a frequency, and their output frequency is directly evaluated. It allows removing the traditional analog test vector generator and output evaluators, and consequently reduces the test complexity, area overhead, and test cost. As no test vector is required in this test strategy, testing of high-frequency analog circuits becomes less difficult. The test time is short because only a frequency per building block must be verified.

The observability of a fault in a component is the sensitivity of the oscillation frequency f_{osc} with respect to the variations of such component. To increase the observability of a defect in a component, the sensitivity of the oscillation frequency with respect to that component should be increased. In other words, during the configuration process of the CUT to an oscillator, the oscillator architecture must be chosen to ensure the maximum possible contribution of the CUT components in determining the oscillation frequency. Existing faults in the CUT related to components that are involved in the oscillator structure manifest themselves as a deviation of the oscillation frequency. Therefore, the maximum and minimum deviation of the oscillation frequency form the CUT tolerance band, that should be used to detect fault.

Self-oscillation circuits, such as in the sigma-delta modulators, are still more ease to test using this technique, because no additional circuitry is needed for the feedback loop.

3. Sigma-Delta Modulator Overview

A/D converters based on sigma-delta (ΣΔ) modulation combine sampling frequencies at rates well above the Nyquist rate with negative feddback and digital filtering in order to exchange resolution in time for that in amplitude. Sigma-delta modulators provide a means of exploiting the enhanced density and speed of scaled digital VLSI circuits so as to avoid the difficulty of implementing accurate analog circuit functions. ΣΔ modulator consists of an analog filter and a coarse quantizer enclosed in a feedback loop. Together with the filter, the feedback loop acts to attenuate the quantization noise at low frequencies while emphasizing the high-frequency noise. Since the signal is sampled at a frequency which is much higher than the Nyquist rate, high-frequency quantization noise can be removed without affecting the signal band. Then, the output is filtered digitally to remove the out-of-band noise power and the resulting high resolution digital signal can be down-sampled and coded.

Figure 1 shows an 1-bit ΣΔ modulator first-order loop where the filter consists of a single integrator, the quantizer is a comparator folowed by a latch and an 1-bit D/A converter. Higher order ΣΔ modulators, containing more than one integrator, offer the potential of increase resolution up to 16-20 bits.

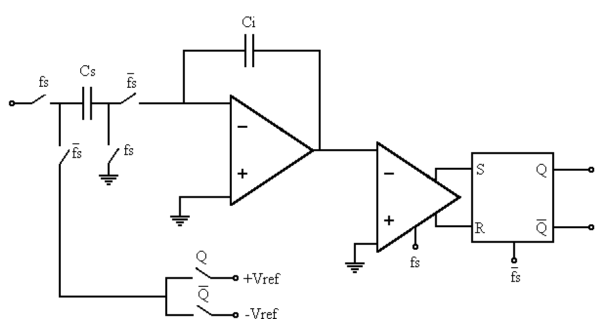

Figure 1 – A first order switched capacitor sigma-delta modulator.

4. Test circuitry

The circuit choosen for the simulation was a first order switched capacitor sigma-delta modulator, develop by [CHO00a][CHO00b].

The proposed test circuit uses the sigma-delta self-oscillation characteristic to improve the test. No additional circuit is needed since the loop feedback intrinsically exists in the circuit under test. In the test procedure, the input switch selects the ground input (disconnecting the external input) and the oscillation is established (see figure 2). The oscillation frequency is converted to a number by a counter of the test circuit. The number obtained is compared with a predetermined test signature to verify whether or not there is a fault in the sigma-delta modulator. After that, the circuit is reconfigured to its functional mode.

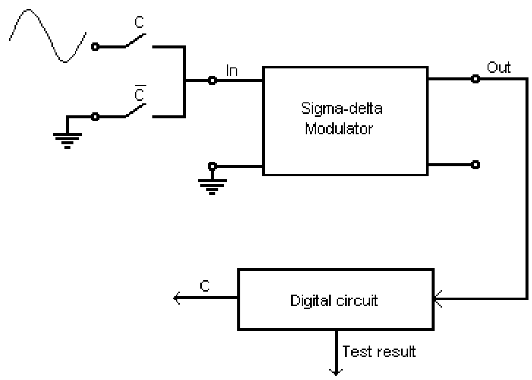

Figure 2 – Complete block diagram of the proposed test scheme.

5. Simulation results

In order to verify the fault coverage of the present test method, a fault list is required. A fault can be either parametric (soft) or catastrophic (hard). Parametric faults, caused by statistical fluctuations in the manufacturing process, comprise the small deviation of the circuit under test parameters from their tolerance band. Catastrophic faults are introduced by random defects, and result in failures in various components.

Table 1 – Electrical simulations results: Injected faults and output changes.

Device	Fault	Output characteristic
Ci	open	Changes on f_{osc}
Ci	short	No oscillation
Ci	↑50%	Changes on f_{osc}
Cs	↑100%	Changes on f_{osc}
Cs	short	Changes on f_{osc}
M4	drain and gate short	No oscillation
M1	drain and source short	No oscillation
V_{ref1}	↑40%	Changes on f_{osc}

A set of parametric and catastrophic faults have been injected in the sigma-delta modulator simulation and the output frequency observed (Table I). All faults resulted any type of deviation on the output frequency.

The oscillation frequency depends strongly on the important characteristics of the sigma-delta modulator. Existing faults in the sigma-delta modulator will deviate the characteristics from the nominal value, which can be monitored by observing the oscillation frequency through the test circuit. As the results demonstrate, all injected faults have been manifested by affecting the oscillation frequency, and can be detected.

6. Conclusion

The test of a sigma-delta modulator based on configuring the circuit to an oscillator have been discussed. The advantages of the technique, such as high fault coverage, reduced test time, a very simple test procedure, and the elimination of a test vector process, can be enumerated. Moreover, the output signal can be evaluated using pure digital circuitry. The technique using the property of sigma-delta modulation, self-oscillation, produces a signature that can be quantified directly by a digital tester. A test circuitry was proposed, based on counting the modulator output pulses and measuring the oscillation frequency. Electrical simulations have shown the sensitivity of some devices related to the circuit natural frequency.

7. References

[ARA97] K. Arabi, B. Kaminska, "Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol 16, No 7, Jun. 1997.

[BOS88] B. E. Boser, B. A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters", IEEE Journal of Solid-State Circuits, Vol 23, No 6, Dez. 1988.

[CHO94] J. H. Choi, "Uma Análise Comparativa Entre os Conversores A/D Sigma-Delta Direcionada ao Projeto de uma Arquitetura VLSI CMOS", Dissertação: PPGC, UFRGS, Porto Alegre, Set. 1994.

[CHO00a] J. H. Choi, M. Ismail, S. Bampi, "Sigma-Delta Analog-to-Digital Converters Test-Chips Designed in Both Full-Custom and SOT Array Methodologies", XV Microelectronics Seminar - Proceedings, Torres-RS, Brazil, 2000.

[CHO00b] J. H. Choi, "Mixed-Signal Analog-Digital Circuits Design on the Pre-Diffused Digital Array Using Trapezoidal Association of Transistors", Ph.D Thesis Proposal: PPGC, UFRGS, Porto Alegre, Dez. 2000.

[HUE99] G. Huertas, D. Vásquez, A. Rueda, J. L. Huertas, "Effective Oscillation-Based Test for Application of a DTMF Filter Bank", In: ITC International Test Conference, 1999.

[IHS98] H. IHS, K. Arabi, B. Kaminska, "Testing Digital to Analog Converters Based on Oscillation-Test Strategy Using Sigma-Delta Modulation", In: IEEE International Conference on Computer Design (ICCD), 1998.