Design of a Field Programmable Gate Array for BIST and Datapath-Intensive Applications

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Abstract

This work presents the design of a new FPGA architecture. This FPGA is targeted to datapath-intensive applications and features testability in the sense each cell has basic structures to implement test algorithms.

1 Introduction

Nowadays is ever more important the use of DFT (design for testability) during the design of an integrated circuit. Built-In Self Test (BIST) is a technique used to address testing ([ABR90] [AGR93]). However, it can be necessary many embedded test blocks to implement such technique, since different kinds of logical blocks require different test algorithms.

Carro [CAR00] proposes the use of a single test area made up of cells with reconfigurable connections and functions. Such strategy aims to reduce the amount of chip area dedicated to test circuitry, since the same hardware blocks can be sequentially reconfigured to perform each one of the required test procedures.

FPGAs are well known reconfigurable devices, however, the most usual general purpose FPGAs are targeted to glue logic. These devices are good to implement random logic but they aren't good to implement compute-intensive or datapath-intensive algorithms ([CHE94] [WAN93]).

In this way, this work intends to propose a new FPGA architecture targeted to compute-intensive or datapath-intensive applications. Another characteristic of this FPGA is the embedded testability in the sense that its architecture have adequate structures to implement BIST (Built In Self-Test) algorithms, as well as FPGA's self-test. Dynamic and partial reconfiguration are to be implemented onto the FPGA too.

This paper is organized as follows: Section 2 presents the methodology chosen and the first approach adopted. Section 3 shows a new approach for the cell and interconnection architecture. Section 4 presents the technique to address partial and dynamic reconfiguration. Some conclusions are finally presented in the last section.

2 Methodology and Previous Work

The design methodology adopted is the one proposed in [BRO96] and consisting in the following steps:

- Define the FPGA's parameters, such as cell granularity and routing architecture;
- Describe the architecture. In this work the VHDL language was used.

- Mapping of benchmark circuits onto the architecture;
- Synthesis (Standard Cells in this work);
- Performance evaluation (delay, area, power).

Our first work was to design an architecture to implement BIST algorithms [SOU00]. Our idea was to design a field programmable device composed of an array of processor elements (PE). Each PE was composed of a control part and a datapath part (Fig.1). Accordingly, each PE owns adequate structures, such as LFSR (Linear Feed-Back Shift Register), to implement BIST algorithms.

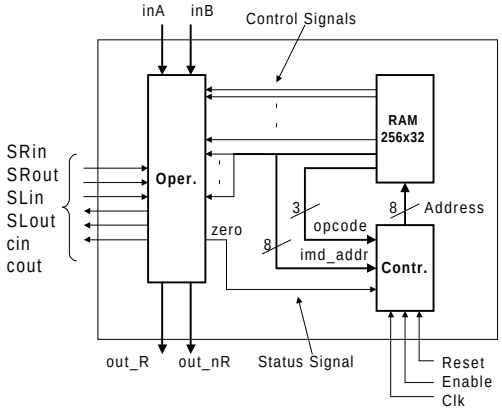

Figure 1- Cell architecture.

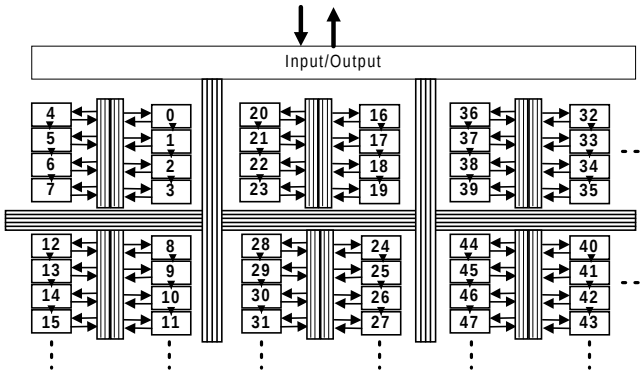

Figure 2 – Hierarchical interconnection.

Moreover, the high processing capability of the PEs allowed to choose a limited interconnection scheme. We chose a hierarchical interconnection structure (Fig.2) to reduce the interconnection delay and to attenuate the area impact on the final device [LAI97].

That device was named TTEPLD (Test Targeted Electrical Programmable Logic Device) [SOU00] since it was in fact an array of processors. It was described using the VHDL language and the validation was done using functional simulation. In that stage of the work we weren't concerned with delay or performance, we were concerned with the functionality of the device.

After that, it was started the mapping of BIST algorithms onto the TTEPLD. In this stage it was noticed that the cell's control part was not necessary at all. The only control needed was some few signals, such as read, write, clock and load. Once the control part occupied a considerable area, a study was started to eliminate this part. Figure 3 shows the mapping of a checksum algorithm onto the TTEPLD.

3 New Approach for the Cell and Interconnection Architecture

Next, we investigated in the literature and found out the datapath targeted FPGAs ([CHE94], [WAN93]). The proposal of [CHE94] is an FPGA with three parts: a memory, a control and a datapath. Each part of the FPGA is optimized to implement a circuitry class (memory, control or data-path). The focus of [CHE94] is on the datapath part.

Soon, it was decided that our device would be an FPGA for BIST and datapath-intensive applications. We then followed the approach of [CHE94] in the sense of our FPGA will have three parts (memory, control and data-path). This work is concerned with the datapath part only, since de control part is well implemented by general purpose FPGAs [CHE94].

3.1 New Cell Architecture

The first cell's version was 8-bit width and was composed of a control part and an operational part ([SOU00] [GON01]). It was noticed that that cell is very large for the targeted BIST applications. The control part is not necessary at all. Moreover, it is interesting to have a finer granularity. The new proposed cell is 4-bit width and is composed of a datapath only. However there will be a little control block outside the cell.

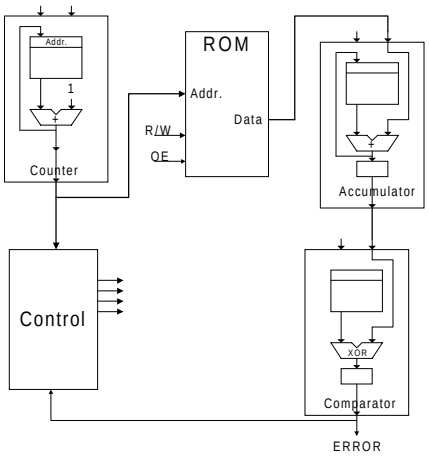

Figure 3 – Example of ROM test.

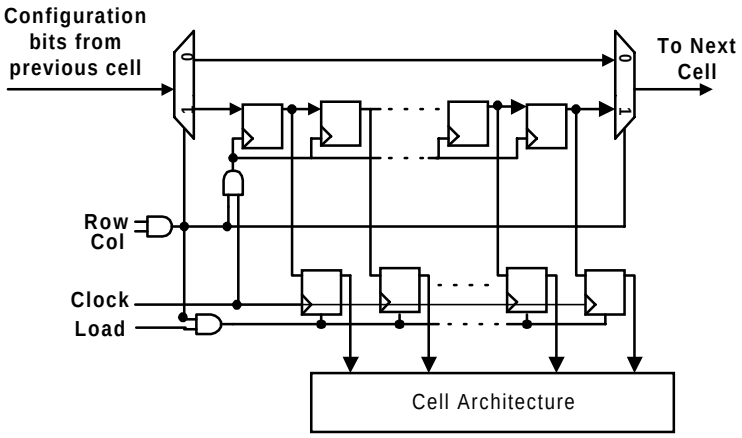

Figure 4 – Dynamic and partial configuration.

A study is going on to choose the new cell architecture. We are considering two ideas: an ALU-based cell like the first approach, but without the complex control part, and a LUT-based cell like the existing on usual FPGAs.

3.2 Interconnection Architecture

There are a variety of interconnection structure schemes, such as symmetrical array, row-based, sea-of-gates and hierarchical [WAN93]. In this work, we are tending to use either the hierarchical or an array-based scheme, since these are the most used in commercial FPGAs and it seems to fit the needs of our device.

The first version of the FPGA used a hierarchical interconnection scheme. An investigation is going on to check if this scheme is better or an array-based scheme should be used.

4 Partial and Dynamic Reconfiguration

In this work, partial reconfiguration is the capability to program some FPGA cells while the remaining cells keeps their original programming. Dynamic means the FPGA can be programmed during operation time [SHI96].

There are various strategies to implement partial and dynamic reconfiguration. Our idea is to implement a serial programming. Each cell has a row and column selector which allows to select the cell for programming. When the cell is selected, the bitstream program is fed into the cell otherwise it is bypassed (Fig. 4).

5 Conclusions

This paper proposes the design of a new FPGA architecture to address two applications classes: BIST and datapath intensive circuits. It was showed the high cell's processing capacity adopted in the first approach is not necessary. So, we are changing the approach to one with a small cell made up of a datapath part only. There are some pending questions, such as cell architecture (ALU-based or LUT-based) and interconnection architecture (hierarchical or array of cells). A study is going on to choose the best fitted to our applications.

6 References

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