A 5V 5-Bits CMOS Paralel ADC Based on Lookup Table Encoding

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Abstract

This paper describes a voltage referenced 5-bit CMOS parallel ADC based on lookup table encoding. Layout and simulation were performed, initial estimative results are presented and main features are discussed. The ADC architecture is the classical topology: voltage reference, comparators and digital encoder. The voltage reference is a resistive divider based with a MOS current source. The comparator circuit has 13 MOS transistors, where 6 perform the clock synchronization.

1 Introduction

Parallel ADC was initially applied in image digitalization. Today, it is widely used in communications, instrumentation and other high frequency applications. Parallel or flash ADC ultimate conversion rate is the clock frequency itself, delivering a word per cycle. Flash architecture is best suited for didactic purpose, since it is very simple in conception and its operating principle offers a strict understanding of analog to digital conversion process. Original flash ADC n-bit architecture is simply composed by a 2^n-1 resistors voltage divider, same number of comparators and a encoder, as shown in figure 1.

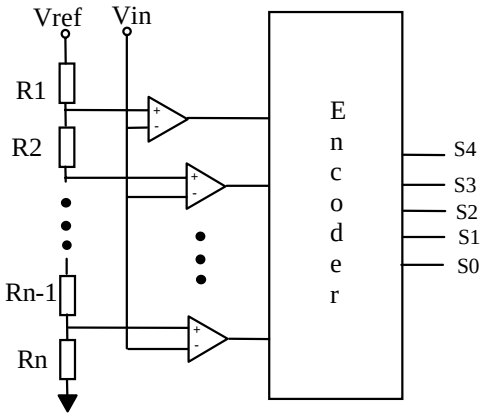

Figure 1 - Parallel ADC block diagram.

In this architecture, resistors characteristics determine overall converter precision, while comparators and encoder limitation dictates conversion rate. As the first block is mainly responsible for static power dissipation, two other blocks consumption is dependent on clock rate. Since, the number resistors and comparators grows exponentially with ADC

word size, this conception has its application limited to few bits converters. Increasing output size both narrows voltage drop in each reference resistor and expands the demand for silicon area. 8-bit or larger Flash ADCs requires interpolation techniques for reducing the number of resistors and comparators, and providing a more reasonable size for I.C. implementation.

2 System Architecture

The basic architectural flash ADC concept is directly implemented in layout. Figure 2 shows ADC layout representations. When a voltage is present at ADC input, all comparators check simultaneously its references levels and generate an output level, based on the following rule:

$$V_{out} = \text{High if } (V_{in}-V_{ref})>0$$

and

$$V_{out} = \text{low if } (V_{in}-V_{ref})<0$$

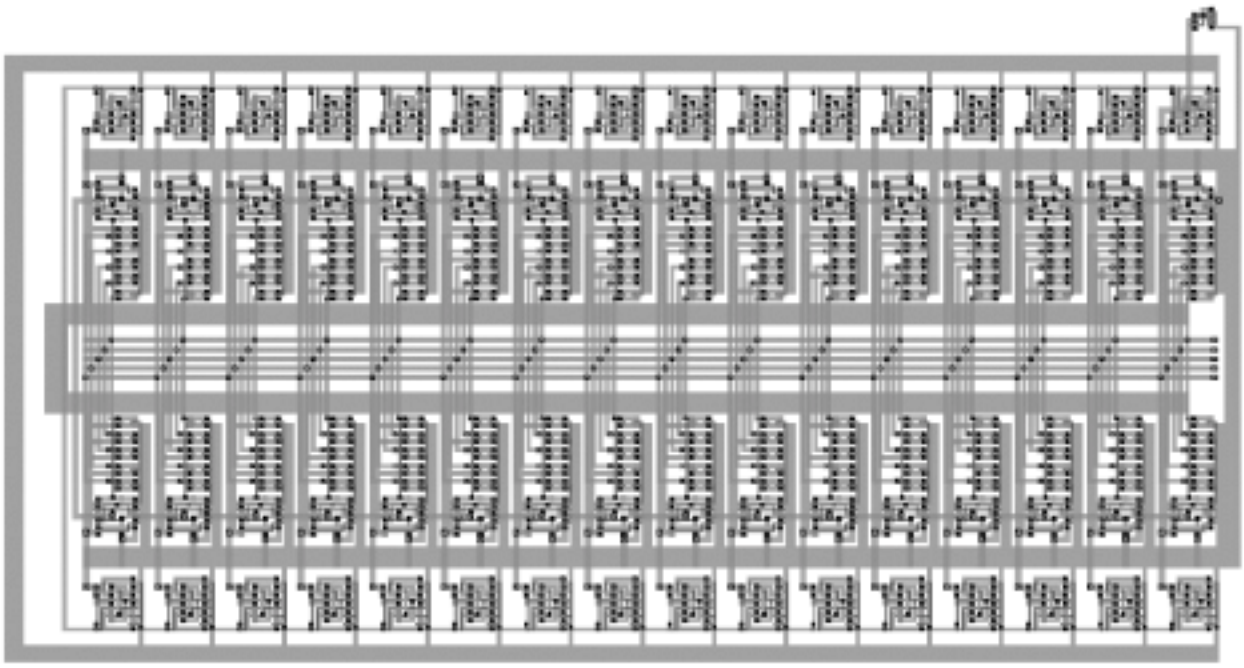

Figure 2 - 5-bit CMOS paralel ADC layout.

Consequently, all comparators output whose references voltages are smaller than V_i goes high, composing a thermometer scale representation for the input level. For each thermometer scale state, a unique binary output code will be generated at encoder block, by switching on a single line in the ROM circuit.

Circuit diagram (fig.2a.) illustrates the three ADC building blocks. Voltage reference is implemented with 31 n-implant resistors, biased by a simple n-mos current source (N1), whose gate is biased by the CMOS voltage divider (P1 and N2). Comparators are clocked, cross-coupled CMOS active loads. Each comparator is build with 6 p-mos (P2-P7) and 5 n-mos (N3-N7) transistors as shown in figure 3.

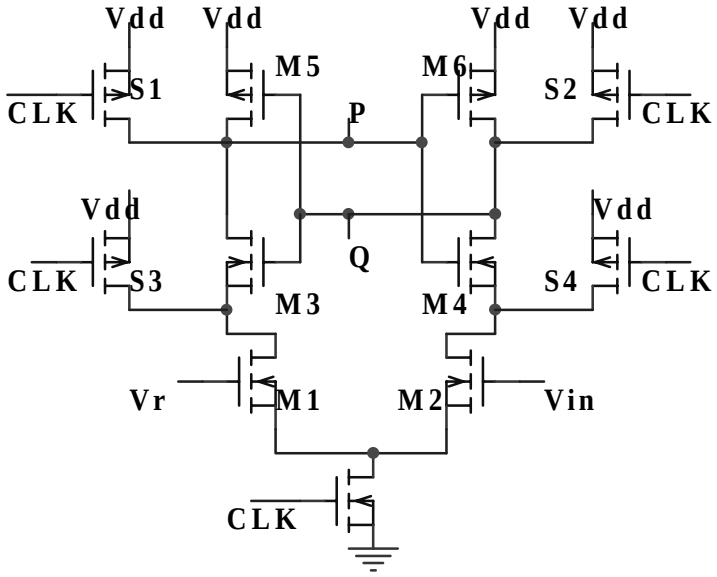

Figure 3 – Clocked CMOS comparator.

This kind of comparator offers three important properties that make it attractive for high-speed design[1]: zero static power dissipation, only a single phase clock is required and input offset dependent on the differential pair rather by the offset of cross coupled devices. Its operation can be explained as follows: as clock remains low, P2-P5 remains in saturation, short circuiting P6, P7, N3 and N4, while N5 is off. Nodes P, Q, X and Y are precharged at V_{DD}, placing the comparator in the reset state. No valid code is available during this period. When clock goes high, P2-P5 turn off, N5 turn on and the input difference (V_{in} - V_{ref}) is amplified by the differential pair N6-N7. As V_{DS} in N6 rises, and drops in N7, P6, P7, N3 and N4 undergoes the opposite effect. The decrement in P node voltage helps P7-N3 action at the same time the resulting Q node increment helps N7-P6, resulting a regenerative extra-gain. An important withdraw of this kind of comparator is its drawback noise produced at th beginning of reset and regeneration modes. This effect can be substantially reduced[1] if a pair of cross coupled devices are added in differential pair. This solution was not yet implemented, because its results are technology dependent and the circuit implementation is still not defined.

Output encoder is based on 32 lines of 5-bit ROM cells composed by transmission gates as illustrated in figure 4. Output binary codes are obtained simply tying the gate input to V_{DD} or V_{SS}. This solution allows an easy code selection, if other than binary output is desired. The selection of an particular code is obtained when the output of C_n comparator is high and C_{n+1} is low, resulting a single and gate output in high level.

3 Experimental Results

The estimate static ADC power consumption is 8mW and, when the clock goes high, it’s about 21mW at a 10MHz of conversion rate.

4 Conclusions

A 5-bit CMOS parallel ADC with lookup table encoding has been presented at layout level. Initial experimental results indicate that although a linear conversion relation is obtained, it has a very limited conversion rate. This problem is associated to comparators performance and the narrow voltage at its inputs in worst-case operation conditions. It signalizes also, the limitation for simple expansion of this architecture to higher bit number.

As a next step, a two-stage comparator will be tested for higher conversion rates operation.

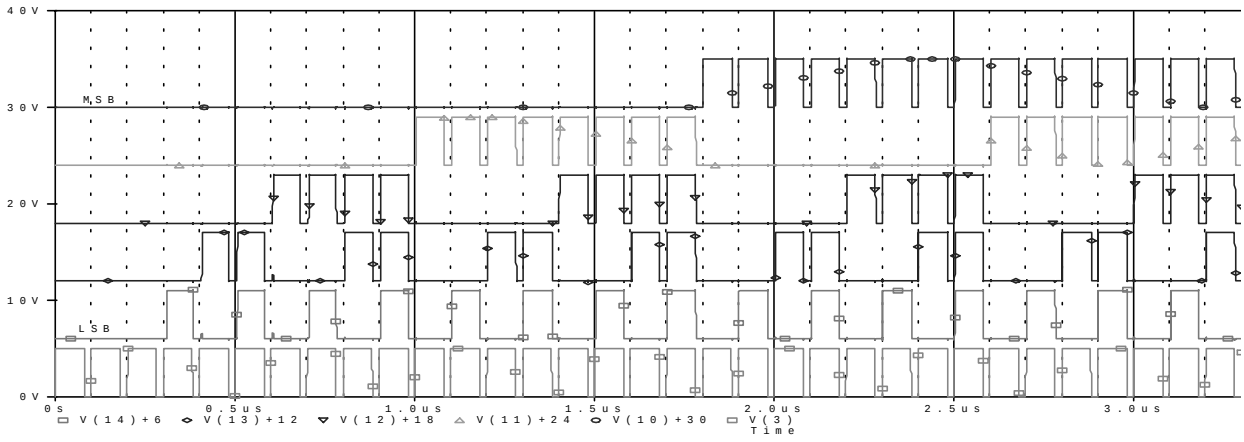

Figure 4 – 5-bit binary lookup table encoder.

4 References

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