Experimental Behavior of the GC SOI MOSFET Operating at Low Temperature

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Abstract – **This work presents the behavior of Graded-Channel SOI nMOSFET at low temperatures. It compares this new device to the Conventional SOI MOSFET decreasing the temperature from 300K down to 100K. The subtheshold slope, transconductance and threshold voltage are analyzed as a function of temperatures and different Graded-Channel devices configuration.**

1.INTRODUCTION

The Graded-Channel SOI MOSFET transistors were created as an alternative to reduce the inherent parasitic bipolar effect in SOI conventional devices. These transistors have an asymmetric dopant concentration in the channel region, which is divided into two parts: the first one presenting low doping concentration beside the drain, length (L_{LD}) and the second one with the usual concentration used in SOI transistors to control the threshold voltage beside the source, length (L_{HD}).

The low doped region is inverted even if the gate voltage (V_{GF}) is equal to zero due to the negative threshold voltage and can be analyzed as a drain extension through the inversion layer. The effective channel lengths (L_{eff}) may be considered as a difference between the mask of channel length (L) and the length of low doped region [1], being equal to L_{HD}.

Due to the reduction of the doping level near the drain, the impact ionization is reduced.

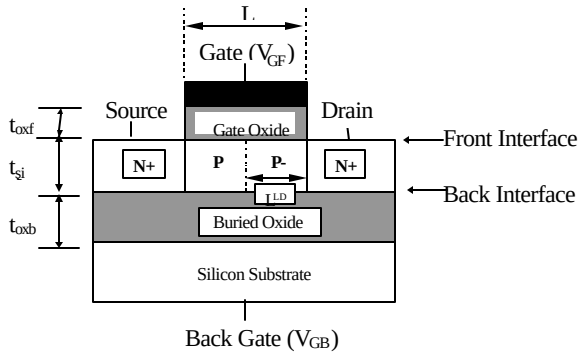

Figure 1: GC-SOI nMOSFET structure

The comparison between this new device with the conventional SOI MOSFET (uniformly doped from source to drain) at room temperature showed an increase in the transconductance, a reduction in the parasitic bipolar effect and improvement in the breakdown voltage[2].

The objective of this paper is to analyze the operation of this new device in low temperatures (since 100K up to 300K) and compare to conventional SOI MOSFETs.

2. EXPERIMENTAL RESULTS AND ANALYSIS

The studied transistors have 30nm thick gate oxide (t_{oxf}), 80nm silicon film (t_{Si}), 390nm buried oxide thickness (t_{oxb}), 2µm channel length (L) for conventional SOI MOSFET and for GC-SOI MOSFET with some different rates L_{LD}/L (0.085, 0.15, 0.30, 0.40 e 0.55) and 18µm channel width (W), $1.10^{17}cm^{-3}$ doping concentration in the high doped channel region (Na_{fHD}) and $1.10^{15}cm^{-3}$ in the lightly doped region (Na_{fLD}).

The measurements were realized in the Variable Temperature Micro Probe System, model K20 by MMR Technology equipment and the curves I_{DS} x V_{GS} and I_{DS} x V_{DS} extracted by Semiconductors Parameters Analyzer HP4145B.

The curves I_{DS} x V_{GF} were extracted with a drain bias of 0.1V, varying V_{GF} from –0,5V to 3V (steps of 10mV) using long integration time.

The Figure 2 shows the variation of subthreshold slope (S) with the variation of temperature for several L_{LD}/L variation obtained of the experimental curves.

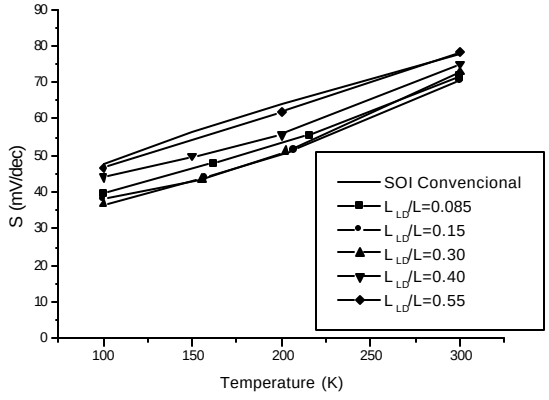

Figure 2: Subthreshold versus Temperature (SxT) for several L_{LD}/L rates.

From the figure 2 is possible to verify that similar subthreshold slope behavior is observed in both GC-SOI

MOSFET and conventional SOI MOSFETs devices, independently on L_{LD}/L.

As the temperature decreases, the subthreshold does as well. This reduction occurred due to the direct influence of temperature in the subthreshold slope. It's important to note that the S reduction is related to the temperature and the capacitance rate $(1+\alpha)$ as shows the equations (1 ,2).

$$S = \frac{k \cdot T}{q} \cdot \ln(10) \cdot (1 + \alpha) \quad (1)$$

being $$\alpha = \frac{1}{C_{oxf}} \left(\frac{C_{Si}(C_{oxb} + C_{itb})}{C_{Si} + C_{oxb} + C_{itb}} + C_{itf} \right) \quad (2).$$

where C_{oxf} is the gate oxide capacitance, C_{oxb} is the buried oxide capacitance, C_{Si} Silicon layer Capacitance, C_{itb} traps capacitance at back interface and C_{itf} traps capacitance at front interface.

With the subthreshold slope values, it was calculated the capacitance rate $(1+\alpha)$. The $(1+\alpha)$ results found to the variation of temperature between 100K and 300K is an average got from the devices operating with the same temperatures (table1).

Table1:Capacitance rate values to different Temperatures

Temperature	1+α
100K	1.8566
150K	1.4674
200K	1.3259
300K	1.2003

With the capacitance rate values obtained, it can be observed that the interface traps capacitance presents a bigger influence when the devices operate at low temperatures.

This larger influence occurs because the Fermi level approaches to the Bandgap edges as the temperature decreases, increasing the trapped charge.

Figure 3 shows the transcondutance versus temperature for several L_{LD}/L variation.

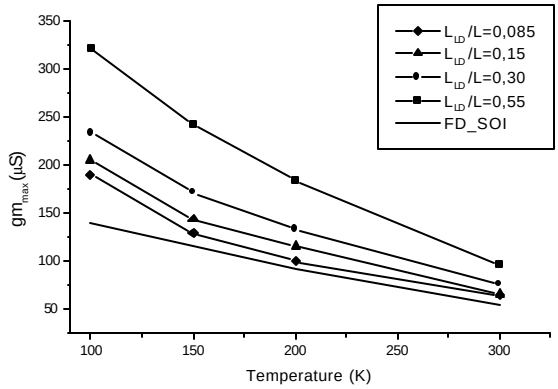

Figure 3: Maximum transcondutance versus temperature (gm x T) for several L_{LD}/L

The graphic was extracted from the first derivative of experimental I_{DS} x V_{GS} curves, according to equation (3)[3]:

$$gm = \frac{dI_{D_{Sat}}}{dV_{GS}} = \frac{W\mu_n C_{oxf}}{L(1+\alpha)}(V_{GF} - V_{th}) \quad (3)$$

In this case, due to the high mobility in low temperatures, the transcondutance (gm) increases when the temperature goes down [4]. This increase in the transconductance grows less due to the bigger capacitance rate $(1+\alpha)$ at low temperatures.

The devices GC-SOI MOSFETs show a more emphasized increase due to the reduction of the effective length of channel when the L_{LD}/L increases.

The figure 4 presents the threshold voltage as function of the temperature (4a) and different Graded-Channel devices configuration (4b).

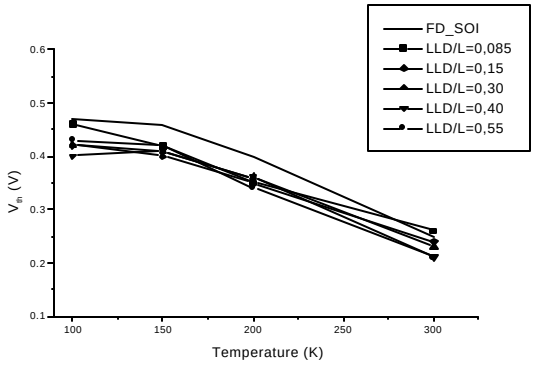

Figure 4a: Threshold voltage versus Temperature.

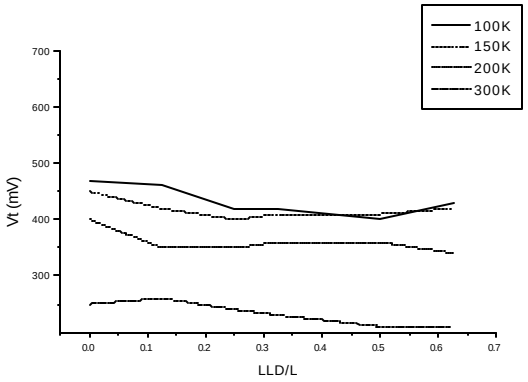

Figure 4b: Threshold voltage versus severals L_{LD}/L

The threshold voltage values presented in the graphics of figure 4 were extracted from a second derivate of the I_{DS} x V_{GF} curves that were got experimentally.

Analyzing the graphics in figure 4, it is possible to note an increase in the threshold voltage is obtained for both GC-SOI MOSFET and conventional SOI when the temperature decreases due to the increase in Fermi potential, the rate capacitance increase (that attenuates

this growth) and besides the reduction of the carriers concentration, which takes place when the temperature goes down [6].

The threshold voltage of the front gate (V_{Th}) for the long-channel thin-film SOI MOSFET is given by [5], considering the back interface depleted, such as the expressions 4, 5 and 6.

$$V_{Th} = V_{FB1} + 2f_F - \frac{Q_b}{2C_{oxf}} - \alpha\left(V_{GB} - V_{FB2} - 2f_F + \frac{Q_b}{2C_{oxb}}\right) \quad (4)$$

where V_{FB1} and V_{FB2} are the Flat-band voltage of first and second interfaces, ϕ_F is Fermi potential, Q_b is the depletion charge in the silicon film and α the capacitance rate. The capacitance rate, like described previously, increase with the temperature decrease due to traps interface.

$$f_F = \frac{kT}{q} \cdot \ln\left(\frac{Na_{fHD}}{ni(T)}\right) \quad (5)$$

and ni(T) is the intrinsic Carrier Density, is given by:

$$ni(T) = 4.9\times10^{15}\left(\frac{m_n^* \cdot m_p^*}{m_o^2}\right)^{0.75} \cdot T^{1.5} \cdot \exp\left(-\frac{Eg}{2kT}\right) \quad (6)$$

where T is temperature in Kelvin, Eg is energy band-gap and m_n^* and m_p^* are the effective masses for electrons and holes, respectively.

3. CONCLUSION

The subthreshold slope is decreased due to the direct influence of the temperature and even though the capacitance rate attenuates this growth, the subthreshold slope approaches of the ideal. The transconductance and the threshold voltage increase with fall of the temperature. In the transconductance this is due to the high mobility, and in the threshold voltage due to Fermi potential increase and reduction of the carriers concentration. The capacitance rate also influence both parameters attenuating yours growth.

It can be noted also that in all the analyzed parameters at low temperature there is an influence of the interface traps capacitance, even though this, as the transconductance and the threshold voltage increase as the subthreshold slope decrease shows the improvement performance of this devices at low temperature.

This work demonstrates that the GC-SOI MOSFET has coherent behavior compared with the conventional SOI MOSFETs devices.

4. REFERENCES

[1] M.A.Pavanello, J.A.Martino, V.Dessard and D.Flandre, "An Asymetric Channel SOI nMOSFET for Reducing Parasitic Effects and Improving Output Characteristics" Solid-State Eletronics, Vol.44, nº7, p.1219-1222, 2000;

[2] M.A.Pavanello, J.A.Martino, V.Dessard and D.Flandre, "An asymetric Channel SOI nMOSFET for Reducing Parasitic Effects and Improving Output Characteristics"-Eletrochemical and Solid-State Letters, vol.1, p.50-52, 2000;

[3] J. P. Colinge; "Silicon On Insulator Tecnology: Materials to VLSI";

[4] M. A. Pavanello, P.G.Agopian, J.A.Martino e D. Flandre, "Low Temperature Operation of Graded-Channel SOI-MOSFETs For Analog Applications", Proceedings of the 5th European Workshop on Low Temperature Electronics, Grenoble, June, 2002.

[5] Dirk J. Wouters, Jean-Pierre Colinge and Herman E. Maes, "Subthreshold Slope in Thin-Film SOI MOSFET's" IEEE Transactions on Electron Devices, vol.37 nº9, September 1990.

[6] Siegfried Selberherr, "MOS Device Modeling at 77K"-IEEE Transactions on Electron Devices, vol.36, nº8, august1989.