# Two-Dimensional Simulation of SOI - MOSFET at High Temperature

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*Abstract* – **Two-Dimensional numerical simulations of SOI-MOSFET were done, varying temperature from 300K to 600K. Some parameters were extract from this device simulation and the results compared to the literature models. The parameters extracted are: threshold voltage ($V_t$), subthreshold slope (S), maximum mobility ($\mu_0$), maximum transconductance ($gm_{max}$) and mobility degradation coefficient ($\theta$).**

## 1. INTRODUCTION

The SOI-MOSFET at high temperatures presents a large field of applications, such as in automotive, aviation, and aerospace industries. The SOI-MOSFET presents fewer faults at high temperature than bulk MOSFET. Comparing bulk MOS devices in relation to SOI-MOSFET devices, the most important device parameters are the threshold voltage ($V_t$) which the variation is 2 to 3 times lower and the junction leakage current that is about 3 to 4 order of magnitude lower.

Two-Dimensional simulations of an SOI-MOSFET device were done varying temperature from 300K to 600K. For these simulations we use Medici simulator v.4.0, to extract main parameters of this device at high temperatures.

## 2. SIMULATION RESULTS

Several numerical simulations were performed using Medici simulator of a device with channel length (L) of 2μm, channel width (W) of 1μm, silicon thickness ($t_{Si}$) of 80nm, buried oxide thickness ($t_{ox}$) of 390nm and gate buried oxide ($t_{oxf}$) of 30nm, varying temperature (300K, 400K, 500K and 600K).

The Medici models used in the simulations were:

TEMPERAT: The lattice temperature for the structure.

ANALYTIC: Specifies that concentration and temperature dependent mobility calculated from an analytic expression is used.

PRPMOB: Specifies that a mobility model using the perpendicular electric field component is used.

FLDMOB: Specifies that a mobility model using the parallel electric field component is used.

CONSRH: Specifies that Shockley-Read-Hall recombination with concentration dependent lifetimes is used.

AUGER: Specifies that Auger recombination is used.

BGN: Specifies that band-gap narrowing is used.

II.TEMP: Specifies that a carrier temperature-based model is used for impact ionization instead of the electric field-dependent model whenever impact ionization is used.

IMPACT.I: Specifies that carrier generation due to impact ionization is included in the solution self-consistently.

The $I_D$ x $V_G$ curves were obtained, from this curves were extracted some parameters of this device, such as threshold voltage ($V_t$), subthreshold slope (S), maximum mobility ($\mu_0$), maximum transconductance ($gm_{max}$) and mobility degradation coefficient ($\theta$).

Figure 1 shows the $I_D$ x $V_G$ curve with $V_D$ = 0,1V. In subthreshold regime, the drain current ($I_D$) increases while temperature increases due to subthreshold slope. But after subthreshold regime while temperature increases, drain current decrease, due to mobility degradation at high temperature.

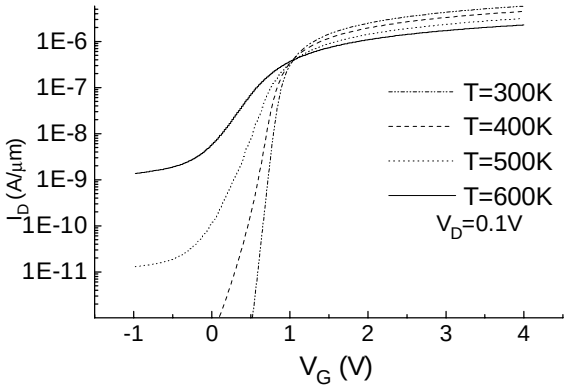


Figure 1: $I_D$ x $V_G$ curve with $V_D$ = 0,1V varying temperature

$$I_D = \mu \cdot C_{ox} \cdot \frac{W}{L}\left[(V_G - V_t)\cdot V_D - \frac{V_D^{\,2}}{2}\right] \quad (1)$$

Where: μ = mobility of the carriers, $C_{ox}$ = Oxide capacitance, W = channel width, L = channel length, $V_D$ = drain-source voltage, $V_t$ = threshold voltage, $V_G$ = gate voltage.

The SOI-MOSFET transconductance, *gm*, is a measure of the effectiveness of drain current control by gate voltage. It is noted in Figure 2 and 3 the transconductance degradation with temperature increases. This degradation has relation with mobility of the carriers reduction. The transconductance equation (2) shows this dependence:

$$gm = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot V_D \quad (2)$$

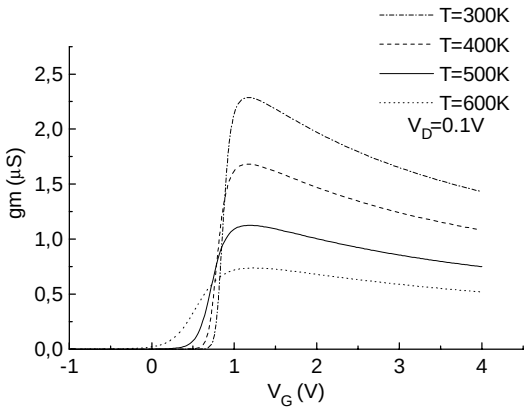


Figure 2: gm x $V_G$ curve varying temperature

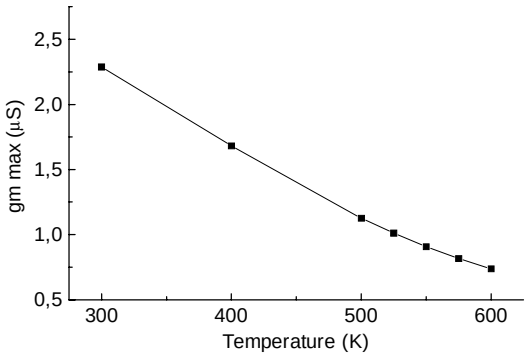


Figure 3 : $gm_{max}$ x T curve

The threshold voltage is the voltage value applicated to the gate, which a sufficient number of movable charges accumulate in channel region, in such a way to invert its surfaces increasing the conduction channel between source and drain. The Figure 4 was extracted from second derivative of $I_D x V_G$ curve simulated. As expected, it is noted in figure 4 the threshold voltage ($V_t$) decreases when temperature increases. The threshold voltage dependence with temperature, after some simplifications, for fully depleted SOI MOSFETs, is given by equation (3):

$$\frac{dV_t}{dT} = \frac{d\phi_F}{dT}\left[1 + \frac{q}{C_{ox}}\sqrt{\frac{\varepsilon_{Si}\cdot Na}{k\cdot T\cdot \ln(Na/ni)}}\right] \quad (3)$$

Where: $\phi_F$ = Fermi potential, q = elementary electron charge, k = Boltzmann constant, T = temperature, Na = concentration of type p dopants, ni = intrinsic electrons concentration, $\varepsilon_{Si}$ = silicon permitivity.

While temperature increase, the intrinsic carriers concentration increase and $\phi_F$ decrease, what make that $xd_{max}$ decrease too. In this moment the fully depleted device becomes partially depleted above a critic temperature, ($T_k$) that is approximately 514 K and the transistor behaves similarly to the bulk one.

This is observed in simulated transistor, as we can see in $V_t$ x T curve, after one temperature the threshold voltage has a sudden roll off, from this moment the fully depleted device becomes partially depleted.

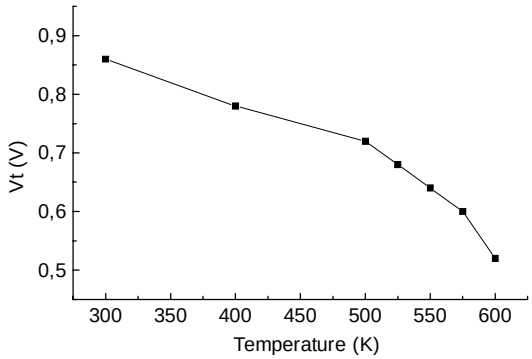


Figure 4: $V_t$ x T curve

The Figure 5 shows the variation of θ (mobility degradation coefficient) in relation with $V_G - V_t$ in several temperatures, calculated using equation 4. It is noted that while temperature increases the θ decrease. Observed to that the curve of 600K has a bigger difference than another curves, we can say that the device is partially depleted.

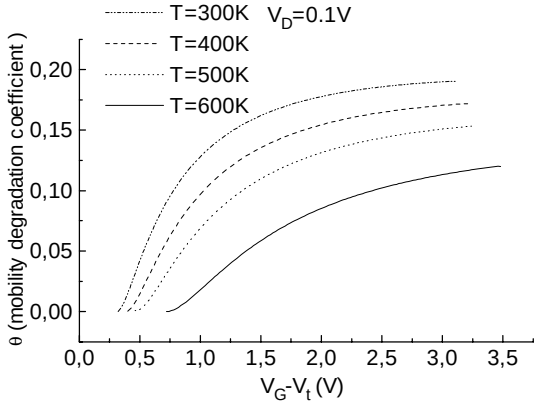


Figure 5: θ x $V_G - V_t$ curve, varying temperature

The maximum mobility ($\mu_{max}$) decreases at high temperature, due to the larger crystalline lattice vibration, due to minority carriers shock. This degradation is shown in Figure 6. The maximum mobility has been extracted in the maximum transconductance.

The mobility dependence with gate bias is given by equation (4):

$$\mu = \frac{\mu_{max}}{1+\theta(V_G - V_t)} \quad (4)$$

Where: $\mu_{max}$ = maximum mobility of the carriers, $V_G$ = gate voltage, $V_t$ = threshold voltage, $\theta$ = mobility degradation coefficient.

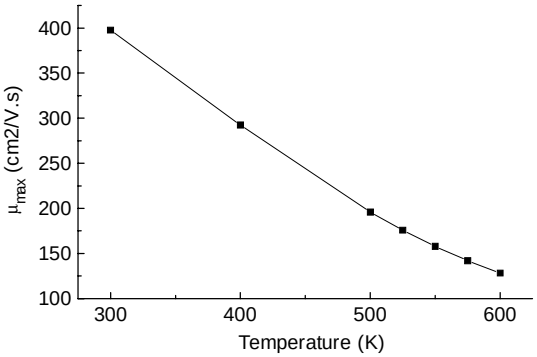


Figure 6: $\mu_{max}$ x T curve

The figure 7 shows S (subthreshold slope) x T curve, observed that the slope increase when temperature increase due to temperature (T) to be directly proportional to subthreshold slope (S), and another terms of equation (5) are smaller. This slope is given by equation (5):

$$S = \frac{kT}{q}\ln(10)\left(1+\frac{C_{depl}}{C_{ox}}\right) \quad (5)$$

Where: $C_{depl}$ = depletion capacitance $C_{depl} = \frac{dQ_{depl}}{d\phi_S}$ (6)

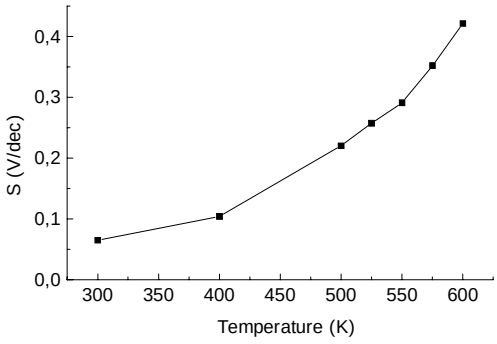


Figure 7: S x T curve

Figure 8 shows $I_D$ x $V_D$ curve varying $V_G$ to obtain a same polarization condition, simulated without Impact Ionization model, with $V_{GT}$ = 200 mV, where $V_{GT} = V_G - V_t$.

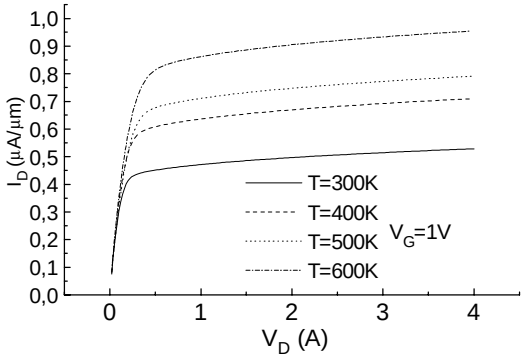


Figure 8: $I_D$ x $V_D$ curve varying temperature, without impact ionization

Figure 9 shows $I_D$ x $V_D$ curve, with impact ionization model. Is observed that when impact ionization model is used the drain breakdown voltage ($BV_D$) decrease, due to parasitic bipolar transistor found in the n-channel SOI-MOSFET, that is not so good.

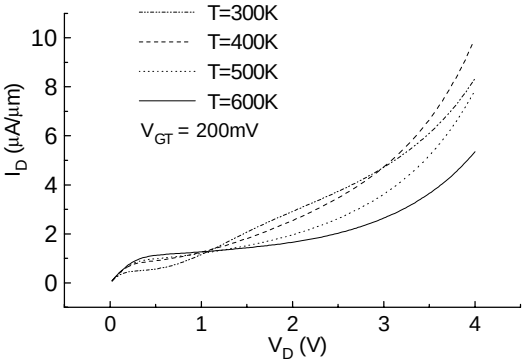


Figure 9: $I_D$ x$V_D$ curve, varying temperature, with impact ionization.

## 3. CONCLUSION

Numerical Two-Dimensional simulations of SOI nMOSFETs at high temperatures were used to study some electrical parameters such as threshold voltage, transconductance, mobility degradation coefficient and subthreshold slope.

It is observed that threshold voltage reduces due to the Fermi potential decrease, the subthreshold slope increases due to large diffusion current, and the maximum mobility decreases due to the larger crystalline lattice vibration. Although the maximum mobility reduces at high temperatures the mobility degradation coefficient decreases as the temperature increases.

## 4. REFERENCES

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