Fabrication and Electrical Characterization of NMOSFET Transistors

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***Abstract*—This work presents an electrical characterization of NMOSFETs devices processed in an Interuniversity Center. The I_D x V_G and I_D x V_D curves were used to extract electrical parameters. The results were compared to literature and a good agreement was found.**

I. INTRODUCTION

THE devices used in this work were processed at AIME – Atelier Interuniversitaire of Microelectronique, Toulousse, France.

The processed wafers have different NMOS circuits and devices such as diodes, capacitors, transistors and resistors. In this work just NMOS transistors were used in the electrical characterization.

Figure 1 shows the long and short channel NMOS transistors used. The experimental results are presented in the Section III.

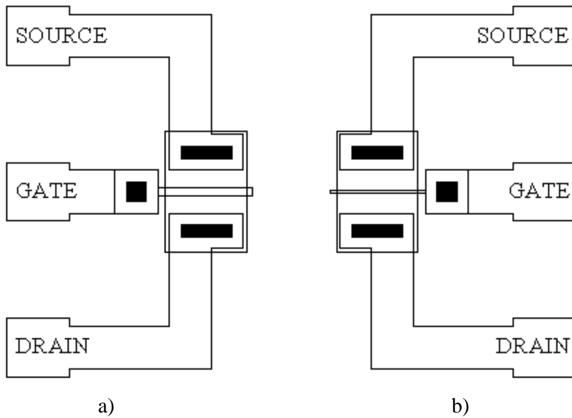

Figure 1: a) Long channel NMOS transistor; b) Short channel NMOS transistor .

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II. PROCESS DESCRIPTION

The goal of the process was to build NMOSFET transistors using polysilicon gate and the P-type substrate. The first step was to deposit a layer of SiO_2 to realize the first photolithography where the active regions were defined.

The gate oxide was grown in a temperature about 1100 ºC and after this, a layer of polysilicon doped with Phosphor was deposited using a LPCVD reactor (Low Pressure Chemical Vapor Deposition). The next stage (photolithography nº 2) defined the location of the source, drain and the channel lengths. Two different mask channel lengths were used (L_m equal 6 and 18µm) and a mask channel width of W_m = 180µm.

Source and drain regions were formed by Phosphor diffusion at 1050 ºC during 15 minutes followed by an annealing of 10 minutes at 1100 ºC. Due to the lateral diffusion of the source and drain regions, there was a reduction in the mask channel length. A resistivity of 0.00117 Ω.cm was obtained in the source and drain regions by four probe measurements.

A SiO_2 L.T.O. (Low Temperature Oxidation) layer of 500 nm was deposited on the whole wafer and placed in a oven (420ºC) to the accomplishment of the photolithography nº 3, that has the objective of open the contacts.

A 500 nm layer of aluminum was evaporated using Vacuum Thermal Method to realize the last photolithography that delineated the interconnections of the components with the metal. To finish the process an annealing of the metal in a temperature about 400 ºC, during 20 minutes, was realized.

III. EXPERIMENTAL RESULTS

After the process, the short channel NMOSFET devices presented an effective channel lengths L_{eff} of 3.17µm, an effective channel doping concentration Na = $9x10^{15}$ cm^{-3}, front gate oxide thickness t_{ox} of about 68.3nm and a junction depth x_j of 1.6 µm.

Figure 2 shows a cross-section of the devices where some used notations are illustrated.

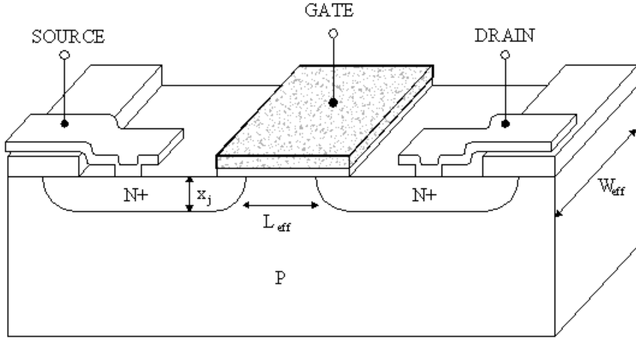

Figure 2: Cross-section of the NMOSFET device where some used notations are illustrated .

The I_D x V_G and I_D x V_D curves were used to extract some parameters, such as threshold voltage V_{th}, Early Voltage V_{EA} and the transconductance g_m. All measurements were performed using a HP4145B Semiconductor Parameter Analyzer. Figure 3 shows the I_D x V_G and g_m x V_G curves with $V_D = 0.1V$.

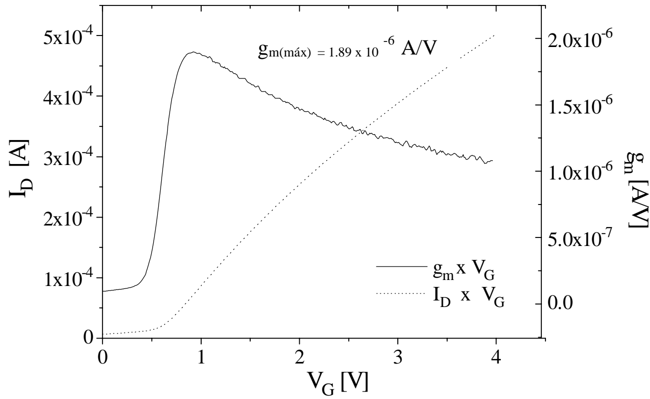

Figure 3: I_D x V_G and g_m x V_G curves.

The Linear Extrapolation Method was used to extract the threshold voltage resulting $V_{th} = 0.53V$. To find the transconductance, equation (1) was derived as a function of V_G resulting equation (2).

$$I_D = \mu \cdot Cox \cdot \frac{W}{L}\left[(V_G - V_{th}) \cdot V_D - \frac{V_D^2}{2}\right] \quad (1)$$

$$g_m = \mu \cdot Cox \cdot \frac{W}{L} . V_D \quad (2)$$

Where μ is the mobility, C_{ox} is the gate oxide capacitance, W the channel width, L is the channel length, V_D is the drain voltage, V_{th} is the threshold voltage, V_G is the gate voltage and g_m is the transconductance. The transconductance is linearly related to the mobility and one can monitor the mobility evolution due to the gate bias increase by measurements g_m. From figure 3 there is a reduction of g_m for V_G larger than 1 V caused by the mobility degradation due to vertical electrical field, as the drain voltage is small.

Figure 4 shows I_D x V_D curves for different V_G. The Early Voltage was extracted from figure 4 resulting $V_{EA} = -22$ V.

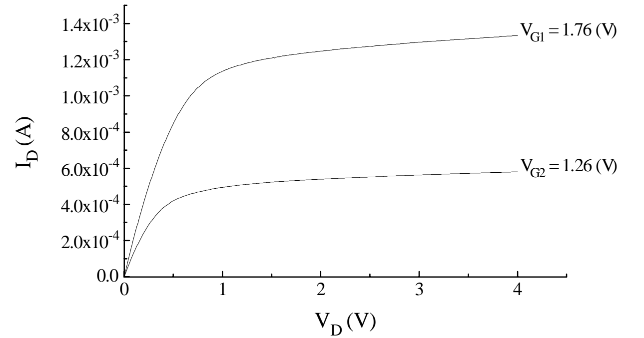

Figure 4: I_D x V_D curves for different V_G.

IV. CONCLUSION

This work has presented a process description of NMOSFETs devices built at AIME – Atelier Interuniversitaire of Microelectronique, Toulousse, France.

An electrical characterization was performed and a threshold voltage $V_{th} = 0.53V$ and Early Voltage $V_{EA} = -22$ V were obtained.

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