

Experimental Determination of Early Failure Rates for Card Assembly by Surface Mount Technology (SMT)

Alex de Macedo, Peter Lubomir Polak, Edson Yuichi Suzuki, Victor Sonnenberg, and Mauricio Massazumi Oka

Abstract—The early failure rate for a card assembled by SMT (Surface Mount Technology) process has been previously determined by the analysis of production yield data available in a database in Celestica, as well as the percentage of the early failures that are forced by the burn-in. However, concern about the data validity and calculation methodology had come out. In this work the previously determined failure rates for the selected card were confirmed in carefully controlled experiment. Additionally, the possibility of determining the time-to-fail during the burn-in, that would allow determining the burn-in parameters, using the available testing system was evaluated.

Index Terms—Burn-in, Weibull plot, SMT, early failure.

I. INTRODUCTION

IN many industrialized products, including electronics, it is observed that part of the products fails prematurely, before reaching the expected mean-lifetime. The early failures in electronics assembly are attributed to variations in production processes and miss handling of the components, which introduces weaknesses in some of the components. The burn-in intends to force the occurrence of all early failures, preventing fragile products to be shipped to the consumer. For this purpose the product is submitted to an effort of convenient extent and duration. The task is to determine the type and extent of the effort (for example, increase of the temperature) as well as its duration, balancing the requirements of reliability

Manuscript received May 29, 2002. This work was carried out at Celestica in cooperation with FATEC and EPUSP.

Alex de Macedo is undergraduate student of the Faculdade de Tecnologia de São Paulo, Pça. Cel. Fernando Prestes, 30, CEP 01124-060, São Paulo, SP, Brazil, (e-mail: anderlexm@ig.com.br).

Peter Lubomir Polak, is undergraduate student of the Faculdade de Tecnologia de São Paulo, Pça. Cel. Fernando Prestes, 30, CEP 01124-060, São Paulo, SP, Brazil; (e-mail: peterpolak@uol.com.br).

Edson Yuichi Suzuki is with Celestica, Rodovia Presidente Dutra, km 214 P2, CEP 07210-902, Cumbica, Guarulhos, SP, Brazil, (e-mail: eysuzuki@celestica.com).

Victor Sonnenberg is with the Faculdade de Tecnologia de São Paulo, Pça. Cel. Fernando Prestes, 30, CEP 01124-060, São Paulo, SP, Brazil; (e-mail: sonnen@lsi.usp.br).

Mauricio Massazumi Oka is with the Electronics System Department, of the Escola Politécnica da Universidade de São Paulo, Av. Professor Luciano Gualberto, trav. 3, n° 158, CEP: 05508-900, São Paulo, SP, Brazil, (e-mail: oka@lsi.usp.br).

and total cost. In order to design the process, the burn-in parameters must be determined, which means that the Weibull curve must be plotted for the selected card [1]. The knowledge of the distribution of the time-to-failure or the early failure rates for various burn-in duration are required to plot the Weibull curve.

The database in Celestica has been previously analyzed, regarding to the assembly yield of a selected card in order to design an experiment that would allow determining the burn-in parameters [2]. However, many assumptions were necessary and a data filtering was needed in order to eliminate inconsistent data. The goal of this paper is to give support to the assumptions made and thus corroborate the conclusions in the previous work.

II. EXPERIMENTAL PROCEDURE

For the burn-in study, a double-sided card, with approximate dimension of 7 cm x 7 cm, with SMD (Surface Mount Device) components assembled only on one of the faces was chosen. Each card has a 32 pins connector, an ejector, about 50 SMD components, and two analog IC's (Integrated Circuits). There are two card versions, differing basically by the two IC's. One of these versions has two IC's with PLCC (Plastic Leaded Chip Carrier) type package of 32 pins with 1.27 mm pitch, which is named type A. The other version has two IC's with 48 pins SOP (Small Outline Package) type package with 0.65 mm pitch, which is named type B. Both types of cards were considered in order to get a larger amount of data. 8,960 cards were analyzed in the present work.

After the card assembly by standard SMT process, burn-in was carried out in a chamber at 45 ± 5 °C for 30 h. During the burn-in the cards were biased and they were cyclically submitted to a simplified electrical testing using a personal computer (PC). The simplified-testing is a subset of the complete-testing carried out later. The cards were mounted in proper racks in order to achieve biasing and communication with the PC. 33 % of the assembled cards were of the type A and 67 %, of the type B. After the burn-in the cards were submitted to the complete-testing, in a proper tester, at room temperature. Ultimately, in a last attempt to confirm the card

fail, defective cards were individually tested using a diagnosis program, which allows determining precisely the type and localization of the defect.

III. RESULTS AND DISCUSSION

The simplified-testing is carried out cyclically during the burn-in. Thus the simplified-testing would allow determining the time-to-fail. However the simplified-testing has revealed only 14.3 % of the defects. Therefore, with the available system, it is not possible to reliably determine the time-to-fail during the burn-in. It is noteworthy that the knowledge of the statistical distribution of the time-to-fail would allow determining the burn-in parameters [1]. We can conclude that the only available way for plotting the Weibull curve is to determine the failure rate for several burn-in times.

In the first run of the complete-testing, some faulty cards were identified. After a second run, only 10.0 % of these faults were confirmed. In order to overcome this limitation of the testing equipment, a quite complex job-flow consisting of several test cycles is followed in Celestica. This requirement makes it very difficult to trace the faulty card and thus data acquisition must be conducted very carefully.

After completing the whole testing job-flow each faulty card was individually tested with a diagnosis program. The purpose was to ultimately confirm the defect and help the card rework by precisely determining the defect type and localization. Some working cards were still found.

The ultimate amount of defects is presented here as the ratio of the presently determined failure rate to the one determined previously, from the analysis of the production yield data [1]. The amount of defects was 0.90 ± 0.30 a.u. (arbitrary units) for the version A card and 1.10 ± 0.23 a.u. for the version B card. Therefore both versions are equivalent from the point of view of susceptibility to early failure. This assumption was made arbitrarily in the previous work [1] but the present work gives support to it.

Assuming that both card versions are identical from the point of view of susceptibility to early failure, a failure rate of 1.03 a.u. is found, that is very close to previously determined value [1].

It was found that 10.7 % of the defects were variation of electrical characteristics in integrated circuits. This value is also very close to the one previously found from the analysis of the Celestica's database (10.6 %) [1]. This type of defect is the most suitable to be evidenced by the burn-in for the selected card [1].

It would be necessary to analyze much more than the 8,960 cards, assembled for this work, in order to observe larger amounts of early failures. Therefore, the failure rates presented in this work can not be considered conclusive yet. But the fact that the failure rates are so close to the values calculated from the production yield data available in Celestica is a strong indication that the values are correct.

The failure rates must be determined for several burn-in

times in order to plot the Weibull curve. It becomes clear that a huge amount of cards must be analyzed.

IV. CONCLUSIONS

Larger amount of cards needs to be analyzed in order to determine more reliable fault rates. There are strong evidences that the burn-in would be capable of revealing a very small amount of defects, of the order of 10.6 % of the defects, thus the majority of defects can probably be detected even without a burn-in.

ACKNOWLEDGMENT

The authors wish to express their gratitude to Celestica that provided the means to realize this work.

REFERENCES

- [1] F. Jensen and N. E. Petersen, *Burn-in – An Engineering Approach to Design and Analysis of Burn-in Procedures*. New York: John Wiley and Sons, 1983, pp. 21–32.
- [2] P. L. Polak, A. de Macedo, E. Y. Suzuki, V. Sonnenberg, and M. M. Oka, "Determination of Early Failure Rates for Card Assembly by Surface Mount Technology (SMT) from Production Yield Data," submitted for the Student Forum of the 17th Symposium on Microelectronics Technology and Devices (2002).