DESIGN OF 14 SEGMENTS DISPLAY CONTROLLER

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Abstract: In this paper is described the design of 14 segments display (alphanumeric) controller. The design was based in the concepts taught in the undergraduate course and was used the NMOS technology for it implementation. The design validation was tested using the Orcad Pspice software and the final project (part of it) was sending for fabrication through the PMU available by Centro de Componentes Semicondutores (CCS) at Unicamp.

1. Introduction

In this paper is discussed the project of 14 segments (alphanumeric) display controller, also known as "English Flag" due to the characteristic central cross (see figure 1). This display type is used thoroughly in electronic equipments where is necessary the presentation of alphanumeric information, as for instance: Cd-players, clocks, and any other equipment that demands an alphanumeric interface with the user.

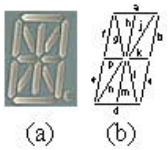

Figure 1: (a) 14 segments display.
(b) Specification of display LEDs.

The motivation for this project was given due to the opening of the course: "Project of Integrated Circuits using NMOS technology", offered by the Department of Electrical Engineering – Faculty of Engineering of Ilha Solteira, UNESP. The objective of this course was allow the design of integrated circuit using this technology by the Electrical engineering undergraduate student. The concepts used in this design must to be teach in the previous undergraduate course. The paper is divided as follow. In the section 2 the logical gates are described. In the section 3 and 4 the combinational and sequential circuits, are presented and discussed, respectively. The general conclusions are finally presented in the section 5.

2. Logical Gates

As the objective of the project was to develop digital circuits using NMOS transistors, the necessary logical gates for the implementation should be provided based in the transistor level For this project we used the simpler logical gates as NOT (figure 2), NAND (figure 3) and NOR (figure 4).

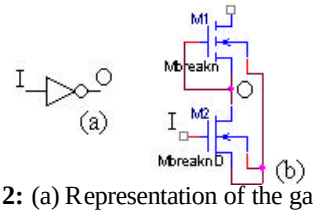

Figure 2: (a) Representation of the gate NOT.
(b)Gate NOT implemented with NMOS transistors.

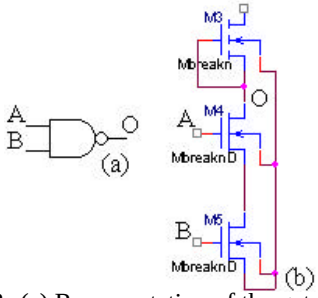

Figure 3: (a) Representation of the gate NAND.
(b) Gate NAND implemented with NMOS transistors.

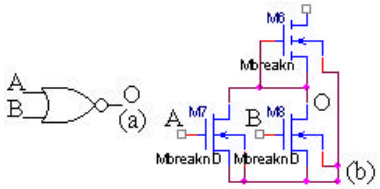

Figure 4: (a) Representation of the gate NOR. (b)Gate NOR implemented with NMOS transistors.

3. Combinational Circuit

Starting with a true table, it was implemented a combinational circuit of 5 inputs and the 14 output necessary to control the display.

Each letter of the alphabet (or symbol) it was associated to a binary entrance. The 5 input are necessary so that the logic can cover the whole alphabet. Like this, when the entrance goes 00000, the display will show "_" (space), however when the input goes 00001, we will have as exit the letter "A", for 00002 we will have "B", and so on. The true table will be presented to proceed.

The Boolean equations of the circuit were reduced using the Karnaugh Diagram.

4. Sequential Circuit

The sequential circuit for this project can be implemented in several ways. Your function is basically the one binary accountant. He serves as a memory of words or sentences and your exits are the entrances of the combinational circuit.

As each letter of the alphabet is related to a binary input in the combinational circuit, the binary accountant should generate a sequence of binary inputs that produce the wanted sentence.

For each previously programmed sentence it should have a sequential circuit specific that generates those sequence of inputs.

We can have several independent accountants circuits, each one prepared to generate a specific sequence. With this, it should have another circuit that can enable just one accountant per time, so that, just this generates the inputs of the combinational circuit.

5. General conclusions

Some alterations of the circuits, so much combinational as sequential, could result in a smaller cost of components. A study more deepened it was able to, for instance, to analyze the advantages of using negative logic, what would probably reduce the gates number in the combinational circuit. In the sequential circuit, we can use several types of available flip-flop and to evaluate which of them makes possible a better economy of components.

The main idea of this project was make a circuit with specific practical purpose and the obtained results were satisfactory.

References

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(2) Texas instruments. The TTL Logic Data Book Standard TTL, Schotthy, Low-Power Schottky, 1988