Mixed-Signal Analog-Digital Circuits Design for Sigma-Delta Modulation Applied to Programmable Analog Arrays

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Abstract

Analog circuit design is a challenging activity. It depends on several factors, such as a reliable device modeling, specific expertise and knowledge of design modules. In order to develop a reliable design methodology for CMOS analog circuit design, a extensive study was made aiming the design of basic building blocks used in Sigma-Delta modulators (ΣΔM). This paper presents the design of a continuous time band-pass ΣΔM developed for a HPAA architecture.

1. Introduction

The development of VLSI (*Very Large Scale Integration*) technology, coupled with the demand for systems integrated on a single chip, has resulted in a tremendous potential for the design of analog integrated circuits. Most VLSI systems require analog circuits or systems such as reconstruction filter, digital-analog and analog-digital converters, and so on. Analog design depends on several factors, such as a reliable device modeling and the individual experience and background of the designer. With the constant integration of analog and digital systems (mixed-signal design), the design constrains change considerably, becoming necessary to examine closely its design in a purely digital technology.

The main goal is to develop analog CAD tools and design techniques to achieve a faster and better design with low cost. An important design technique proposed in [1], is the use of TAT (Trapezoidal Association of Transistors) composite transistor on the semi-custom Sea-of-Transistor (SOT) array. In [3], analog design techniques based on a pre-diffused digital transistor array were used to implement an analog and mixed-signal system. A 2nd order Sigma-Delta Modulator was developed, designed and fabricaded on a semi-custom transistor array [1].

This work proposes the design of a continuous time band-pass Sigma-Delta Modulator, and its building blocks, developed for a HPAA (High Performance Analog Array) architecture [4], using a full-custom design technique and a pre-diffused digital transistor array design technique. This paper is organized as follows: section 2 presents the analog system overview, the band-pass ΣΔ modulator topology. Section 3 discusses the analog circuit design methodology and shows the study (design and simulation) of the basic building blocks used in Sigma-Delta modulators. Finally, section 4 presents our conclusions and future work.

2. The Analog System implementation

Sigma-Delta modulators (ΣΔM) are mixed signal systems wich are very popular nowadays. ΣΔM are being used in a wide spectrum of applications, because they can be implemented in conventional digital CMOS process with small area and power. Allied with the CMOS compatibility characteristic, the ΣΔM may achieve high resolution with robustness. These circuits are especially insensitive to circuit imperfections and component mismatch and provide a means of exploiting the enhanced density and speed of scaled digital VLSI circuits [7], avoiding the difficulty of implementing complex analog circuit functions within a limited analog dynamic range. In [4] a new architecture for analog programmable circuits is proposed, a High Performance Analog Array (HPAA) architecture, using a continuous time band-pass Sigma-Delta Modulator (BPΣΔM). Thus this work proposes the development of an analog system, a BPΣΔM, aiming a HPAA architecture.

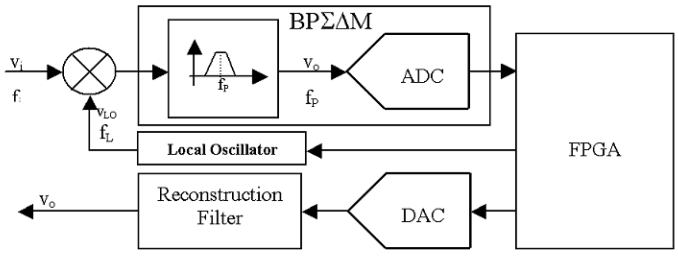

Figure 1 - Basic architecture of the HPAA system

3. Analog basic building blocks design

In order to develop a reliable design methodology for CMOS analog circuit design, an extensive study was made aiming the basic building blocks used in Sigma-Delta modulators. ΣΔ Modulator consists of an integrator and a coarse comparator enclosed in a feedback loop. First, the study was concentrated in 3 basic analog building blocks: current mirror, common-source amplifier and differential amplifier.

Analog integrated circuit design is clearly a technology-driven activity. The designer must understand the process deeply enough to be able to model, lay out, and test his chips. The first step is to characterize the technology about to be used. Several technology parameters that are supplied by the foundry are determined for a specified from the SPICE MOSFET BSIM3v3.2.2 model for the AMS0.35µm technology.

A reliable design model based in [2], [6] and [8] was studied here. The model is suitable to hand, calculator, or computer analysis. The primary application of the model is to simulate or solve the small-signal behavior. The behavior includes the biasing of the active devices, including capacitances.

The devices are characterized in the saturation region. An important parameter for analytic analog design is the LAMBDA (λ) parameter that emulates the output resistance of the transistor. This parameter depends directly on the channel length L, yet it is assumed to be constant on level 1 SPICE. This parameter was estimated for several channel length (L=0.3µm, L=1µm and L=2µm) through SPICE simulation.

With all the technology parameters necessary for analog design determined, the next step is the development of the blocks. The circuit design methodology used here is the based on [8]. The gm/ID method considers the relationship between the ratio of the dc transcondutance *gm* to the drain current ID and the normalized drain current ID/(W/L).

This methodology is strongly related to the performance of the analog circuit, and it gives an indication of the device operating region and provides a important tool for calculating the transistors dimensions. Here the gm/ID versus ID/(W/L) curve is obtained analytically, using a MOS transistor model that provides a continuous representation of the transistor current and small-signal parameters in all regions of operations (like the EKV model shown in [8]), and from SPICE simulation using the BSIM3v3.2.2 model. Figure 2 shows the calculated and simulated plots of gm/ID versus ID/(W/L) for NMOS and PMOS AMS0.35µm transistors.

The gm/ID methodology was applied to the design of the basic analog building blocks. We analized 3 blocks: a current mirror, a single-stage differential amplifier and a common-source amplifier. We assume that the bias current is known (based in [3]) and equal to 600µA, the load capacitor (CL) is 10pF and the supply voltage (VDD) is 3.3V. The design procedure for the amplifiers aims the best performances in terms of dc gain (Av), transition frequency (F_{3db}) and phase margin (PH).

The design procedure includes several steps: the drain current of each transistor is determined from the specified bias current; choosing the values of gm/ID , ID/(W/L) is determined for each transistor from the gm/ID versus ID/(W/L) curves; the transistors lengths are determined by a trade-off between area and stability on one side and dc gain (the LAMBDA parameter depends of the transistor lengths) on the other side (here, the transistor channel length L is considered 5 times the minimum-length allowed by the technology); an extensive simulation is made to validate the electrical performance of the circuit; recalculate the geometrical sizes of the transistors to improve the circuit performance; and, finally, the validation of the circuit.

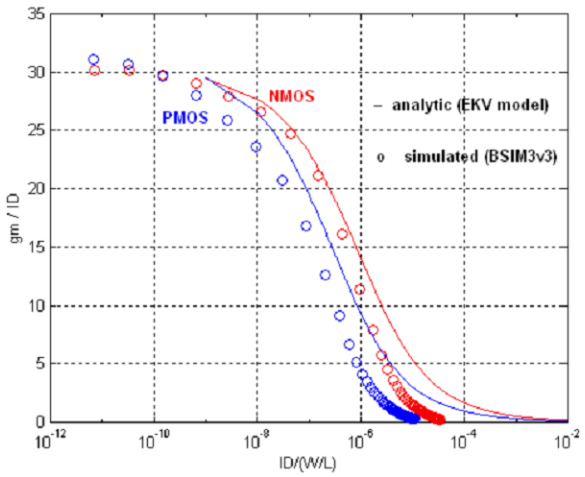

Figure 2 – Calculated and simulated gm/ID versus ID/(W/L) curves for NMOS and PMOS AMS0.35µm transistors

Tables 1 and 2 show simulation results from 2 analog building blocks: current mirror and common-source amplifier. Figure 3 shows the simulated plots from the full-custom Common-Source Amplifier Gain and Phase Margin. The design follows the specification developed in [3], therefore some comparisons between two the different technologies can be made. We also compare the gm/ID

based method results with the results obtained from the conventional design in the same technology.

Table 1. Current Mirror – PSPICE Simulation

Tecnology	AMS0.35µm	
	Conventional method	gm/ID method
VDD (V)	0 - 3.3	0 - 3.3
Iin (uA)	600	600
Iout (uA)	600.16	601

Table 2. CS Amplifier– PSPICE Simulation

Tecnology	0.5µm [3]	AMS0.35µm	
		Conventional method	gm/ID method
VDD (V)	0 - 3	0 - 3.3	0 – 3.3
A_V (db)	31.4	42.8	42
PM (°)	89.6	89.8	89.6
F_{3db} (KHz)	915	413.8	318.6
Vo_{max} (V)	2.72	3.03	3.04
Vo_{min} (V)	292m	198m	223.9m

Table 3. Differential Amplifier– PSPICE Simulation

Tecnology	AMS0.35µm	
	Conventional method	gm/ID method
VDD (V)	0 - 3.3	0 – 3.3
A_V (db)	41.13	37.8
PM (°)	85.2	87.75
F_{3db} (KHz)	180	198.9

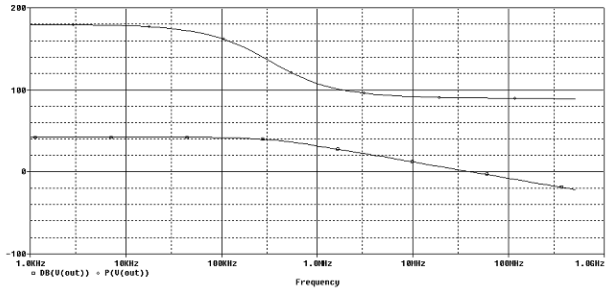

Figure 3 - Full-custom Common-Source Amplifier Gain and Phase Margin designed in the gm/ID methodology, electrical simulation (PSPICE) for AMS0.35µm technology

4. Conclusions and Future Works

The comparisons show the good results using the gm/ID methodology. In the common-source implementation, we can notice a similar DC gain and Phase Margin, proving the design methodology studied. There are some differences, mostly on the transition frequency due to difference between the transistors models.

With a reliable design methodology defined on Section 3, the next step is the implementation of the continuous time band-pass Sigma-Delta Modulator. The system's specifications have been developed aiming the application showed in [4]. After the full-custom design, the same system will be implemented on a semi-custom digital transistor array with the same design techniques studied in [3], using a layout generator tool developed in [5] for further comparisons and prototyping, closing the complete cycle of the analog circuit design process.

5. References

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