DESIGN OF ADDER ARCHITECTURES FOR JPEG COMPRESSION

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ABSTRACT

This paper presents an architectural exploration on the baseline JPEG compressor [1] proposed and designed by Agostini [2]. This exploration was made with the substitution of the operators used in the 2-D DCT calculation architecture of the compressor. The impacts of these substitutions were evaluated in terms of performance and resources utilization. The designed operators focused in the carry lookahead, hierarchical carry lookahead and carry select architectures [3, 4, 5], with the goal to increase the JPEG compressor performance. The operators were described in VHDL, synthesized and validated. They were inserted in the 2-D DCT architecture to the whole module synthesis. The 2-D DCT was synthesized for an Altera FPGA [6]. With this space project exploration, the higher performance obtained for the 2-D DCT was 23% higher than the original, using 11% more logic cells.

1. INTRODUCTION

The JPEG compression of gray scale images can be divided in three main steps that are 2-D DCT, quantization and entropy coding.

In the JPEG compressor, the 2-D DCT is the most critical module to be implemented because of its high algorithm complexity. In the architectural level, this critical path is responsibility of the sum operations on wide inputs, with the consequent delay generated by the carry propagation in the ripple carry architecture used in the original adders [2].

2. TWO DIMENSIONAL DCT ARCHITECTURE

The 2-D DCT architecture used in the JPEG compressor is generically presented in Fig. 1. This architecture was designed to reach a high operating frequency and to allow the use of pipeline techniques. Thus, the architecture was divided into two 1-D DCT architectures and one transpose buffer.

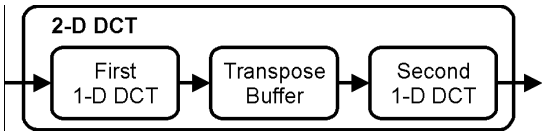

Figure 1 – Generic 2-D DCT architecture

2.1. One Dimensional DCT Architecture

The 1-D DCT architecture proposed by Agostini [2] is presented in the Fig. 2. This architecture is composed by five adders, one multiplier, six ping-pong registers and twelve multiplexers.

The ripple carry adder architecture is used in the adders and in the multiplier. Ripple carry occupies reduced area, but reaches low performances provoked by the slow carry propagation. This carry propagation defines the critical path of the 1-D DCT architecture and, for consequence, of the 2-D DCT architecture.

3. ALTERNATIVE ADDER ARCHITECTURES

Three alternative adders architectures were designed in this paper: carry lookahead (CLA), hierarchical carry lookahead and carry select (CSA). All three architectures have as purpose to speed up the carry propagation [5].

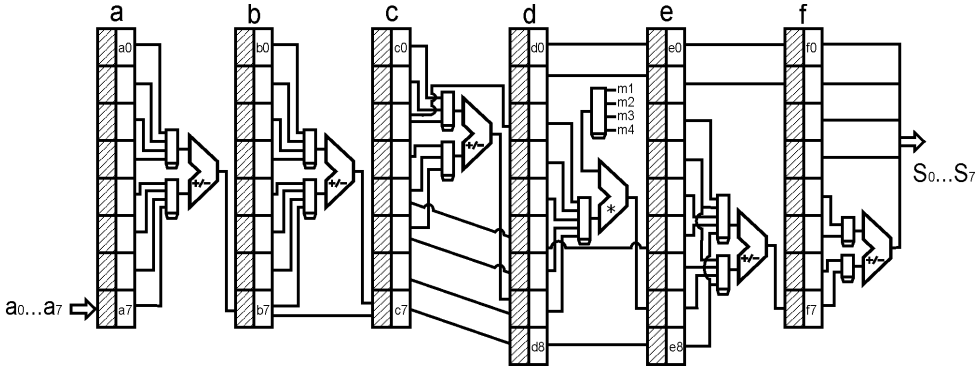

Figure 2 – One dimensional DCT architecture

The CLA adder uses a technique that bases on examining all the adder input stages and, simultaneously, to produce the appropriate carries for each one of these stages. All the carries are calculated at the same time, in parallel and two auxiliary functions are used: carry generate and carry propagate.

Another designed architecture was the hierarchical CLA. The hierarchical CLA approach has the purpose to decrease the CLA equations complexity. In this architecture a control block is used to group *m* adders of *n*-bits width forming an *m* x *n*-bits adder.

An additional approach is the CSA adder [5]. Usually, a CSA adder is divided in two adder sessions. Ripple carry propagation is assumed within the adder sections. Each adder section is duplicated, one with carry and other without carry into the lowest-order bit in the section [5]. A multiplexer selects the appropriate sum in each section.

4. SYNTHESIS RESULTS

Initially, all the described operators were synthesized separately. After, they were synthesized inside of the first and second 1-D DCT modules. Finally, 2-D DCT was synthesized with the new described operators.

The synthesis results for Altera ACEX1K FPGAs [6] are presented in the following tables. The occupied logic cells, the maximum operating frequency, the frequency gain and the resources loss are the parameters showed on the tables. The synthesis of the first and second 1-D DCT were directed for the EP1K50TC144-1 device, and the first 1-D DCT synthesis results are showed in Tab. 1.

Table 1 - 1st 1-D DCT comparative synthesis results

1st 1-D DCT	RCA	CLA	H.CLA	CSA
Logic Cells	1660	1664	1734	1842
Frequency (MHz)	26,45	28,32	28,73	29,15
Frequency Gain (%)	-	7,08	8,62	10,21
Resources Loss (%)	-	0,24	4,46	10,96

Tab. 2 presents the same comparison of Tab. 1, but for the second 1-D DCT.

Table 2 - 2nd 1-D DCT comparative synthesis results

2nd 1-D DCT	RCA	CLA	H.CLA	CSA
Logic Cells	2241	2243	2331	2490
Frequency (MHz)	24,33	25,25	24,5	24,93
Frequency Gain (%)	-	3,78	0,7	2,47
Resources Loss (%)	-	0,09	4,02	11,11

The 2-D DCT synthesis was directed for EP1K100QC208-1 devices and the synthesis results are showed in Tab.3.

Table 3 - 2-D DCT comparative synthesis results

2-D DCT	RCA	CLA	H.CLA	CSA
Logic Cells	4181	4192	4343	4621
Frequency (MHz)	21,88	22,67	24,03	27,10
Frequency Gain (%)	-	3,61	9,83	23,86
Resources Loss (%)	-	0,26	3,87	10,52

As can be seen in the Tab. 3, the performance gains was of 3,61% for the CLA architecture, 9,83% for the hierarchical CLA and 23,86% for the CSA. The losses in terms of resources usage were of 0,26% for the CLA architecture, 3,87% for the hierarchical CLA and 10,52% for the CSA.

5. CONCLUSIONS

This paper presented the design of adder architectures for use in JPEG compression, more specifically for use in the 2-D DCT of a JPEG compressor. Seventy five VHDL descriptions were designed, in a total of 8100 code lines for the three architectural alternatives used in the operators implementation. The synthesis results were presented too.

The best 2-D DCT performance was obtained using carry select adders. In this case, the frequency was more than 20% higher than the original 2-D DCT architecture using ripple carry adders. In this case, the impact in terms of resource usage was less than 11%.

The best relation between the performance gains and the resources losses was found with the use of carry lookahead adders, that increases de 2-D DCT performance with very low impacts in terms of resources usage.

In this paper were not presented global comparative results for the JPEG compressor. The impacts were just estimated and the estimations indicates that the resources usage impact will be shorter than the impacts obtained into the 2-D DCT, once the other JPEG compressor blocks will not be changed. By the other way, the impacts in terms of frequency gains will be approximately the same that the results founded to the 2-D DCT, once the 2-D DCT is the most critical path into the JPEG compressor.

Considering that the main goal of this paper was the increasing of the JPEG compressor performance, the obtained results were considered satisfactory.

6. REFERENCES

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