

# A GM-C BUMP EQUALIZER FOR LOW-VOLTAGE APPLICATIONS

R. Galembeck<sup>1</sup>, J. A. de Lima<sup>2</sup>, and M. C. Schneider<sup>1</sup>

<sup>1</sup>Electrical Engineering Dept, Universidade Federal de Santa Catarina, Florianópolis – SC, Brazil

<sup>2</sup>Electrical Engineering Dept, Universidade Estadual Paulista, 12516-410 Guaratinguetá – SP, Brazil

**ABSTRACT:** A 2nd-order low-voltage CMOS bump equalizer is presented. Its topology comprises a bandpass section and a current mirror. The basic building block of the filter is a MOSFET transconductor, programmable by means of either a DC voltage or a digitally controlled current divider. The bump-equalizer as part of a battery-operated hearing aid device is designed for a 1.4V-supply and a 0.35 $\mu$ m CMOS fabrication process. The circuit performance is supported by a set of simulation results, which indicates a center frequency from 600Hz to 2.4kHz, a quality-factor between 1 and 5, and an adjustable gain at the center frequency in the range of  $\pm 6$  dB.

## I. INTRODUCTION

This work focuses on the design of an equalizer intended for hearing-aid applications. The 2nd-order low-voltage (LV) continuous time bump-equalizer comprises a bandpass section and a programmable current amplifier. The main building block is a transconductor whose transconductance depends linearly on the drain-to-source voltage of a MOSFET operating in the triode region [1,2]. One of the most appealing features of our filter is that all building blocks such as current mirrors, common-mode feedback circuits, and current sources were derived from the basic transconductor topology. Moreover, the tuning strategy is very simple - a DC voltage tunes directly the center frequency of the bump equalizer, while two digital words control the quality factor and the boost/dip coefficient.

This communication is organized as follows. Section II shows the bump-equalizer topology. The fundamentals of the transconductor as well as the topologies of the basic building blocks of the filter are presented in Section III. Circuit design and simulation data are presented in section IV. Concluding remarks are summarized in Section V.

## II. BUMP-EQUALIZER TOPOLOGY

Figure 1 shows the block diagram of the bump equalizer, composed of a classical two-integrator loop filter followed by the bump/dip factor  $k$  and a summing node at the output. The current

transfer function is given by

$$\frac{I_O}{I_{IN}} = \frac{s^2 + sk \frac{g_m/C}{Q} + (g_m/C)^2}{s^2 + s \frac{g_m/C}{Q} + (g_m/C)^2} \quad (1)$$

for  $C_1=C_2=C$ .

In the next sections, we show how to implement the transconductor  $g_m$  as well as the programmable current mirror represented by the block -  $k$  in Figure 1.

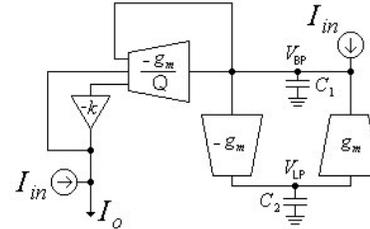


Figure 1 - Block diagram of the bump equalizer.

## III. BASIC BUILDING BLOCKS

a) Transconductor circuit

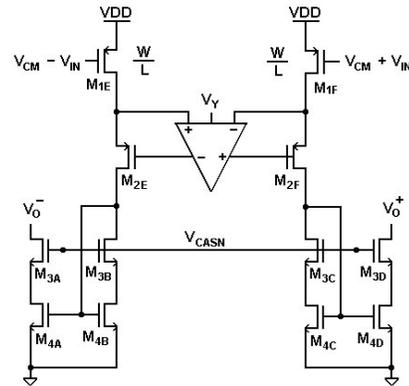


Figure 2 – Transconductor circuit.

The simplified schematic of the pseudo-differential transconductor is shown in Figure 2. High-gain voltage amplifiers keep  $M_{1E}$  and  $M_{1F}$  in the triode region by imposing their drain voltages at  $V_Y$ . Biasing  $M_{1E}$  and  $M_{1F}$  in strong inversion results in a linear dependence of the transconductance  $g_m$  on  $V_{DS}$  according to

$$g_m = \frac{\partial I_D}{\delta V_{in}} = \frac{W_1}{L_1} \mu_p C'_{ox} V_{TUNE} \quad (2)$$

with  $V_{TUNE} = V_{DD} - V_Y$ .

Both the offset voltage of the operational amplifier and the noise level impose a lower bound for  $V_{TUNE}$ , which is safely kept over 30mV in our design. We have used current mirrors for the inversion of the output currents for proper combination with DC bias currents from the CMFB circuit of Figure 3. The output-conductance of the  $g_m$  stage is inherently low.

*b) Common-mode feedback circuit*

The CMFB circuit in Figure 3 is a scaled replica of the transconductor. It must provide the DC current for proper operation of the transconductors. The CMFB operates as follows. Assume the DC output current of the transconductor in Figure 3 equals  $I_{CM}$ . The output DC voltage stabilizes for equal DC output currents of the transconductor and CMFB block. Therefore, the DC current of the CMFB in Figure 3 is equal to  $I_{CM}$  if the arithmetic mean value of  $V_o^+$  and  $V_o^-$  equals  $V_{CM}$ . Since the outputs  $V_o^+$  and  $V_o^-$  are 180° out of phase, the quiescent voltage of the output equals  $V_{CM}$ . Note that one controls the center frequency  $g_m/C$  by changing  $g_m$  through  $V_Y$  of both the transconductor as well as its replica, the CMFB block, responsible for the generation of the bias current. Therefore, the  $V_{CM}$  deviations against  $g_m$  variations are kept to a minimum.

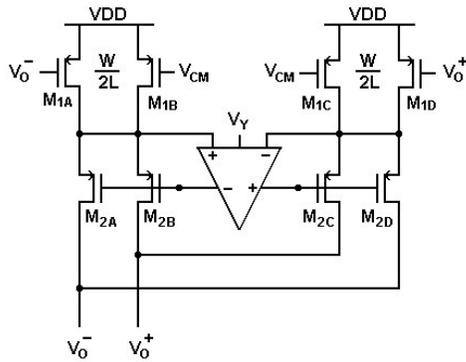


Figure 3 - Common-mode feedback (CMFB) circuit.

*c) Control of the quality factor (Q)*

A simple way to control the  $Q$  is just to deviate a fraction of the transconductor output current from the output node to the  $V_{SS}$  node, as illustrated in Figure 4.

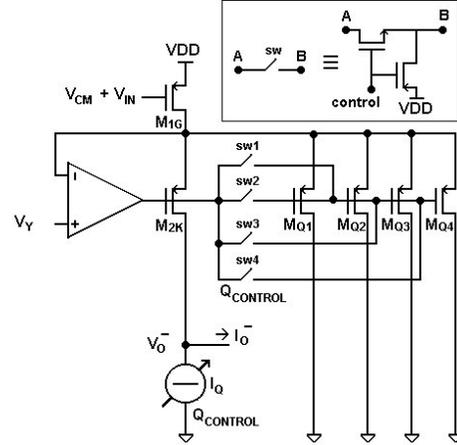


Figure 4 - Transconductor with  $Q$  control.

*d) Control of the current gain (k)*

The current mirror illustrated in Figure 5 implements the current gain block ( $-k$ ). It consists of a transconductor with the output short-circuited to the input (I-to-V converter), followed by a transconductor (V-to-I converter). The output current of the V-I converter is controlled by a set of switches whose ON/OFF states are determined by  $k$ , the current gain.

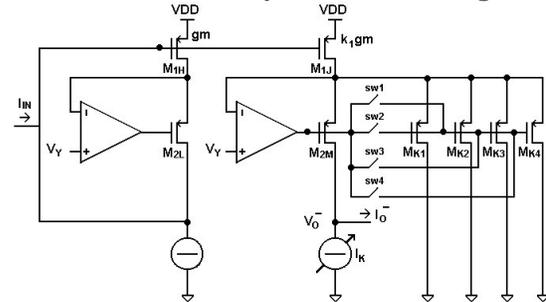


Figure 5 - Programmable current mirror (k-block).

#### IV. SIMULATION RESULTS

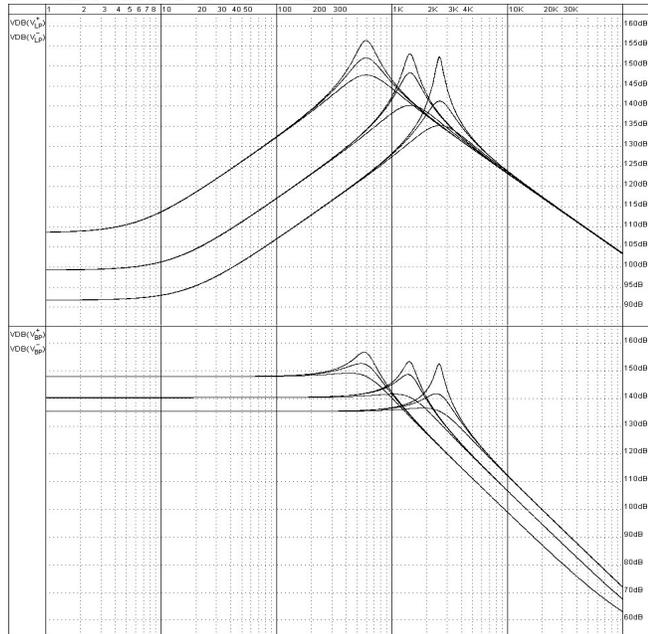


Figure 6 – Smash simulations of the lowpass and the bandpass sections for different  $g_m$ 's and  $Q$ 's.

The simulations presented in figure 6 feature the bandpass and the lowpass small signal frequency responses for different values of  $w_o$  ( $V_{TUNE}$  at 40, 100 and 300 mV). The quality factor was set to 1, 2, and 5.

#### V. CONCLUDING REMARKS

The circuit simulations met the specified project parameters for quality-factor, center frequency and gain. The layout is now being prepared so that the circuit can be integrated in a 0.35 $\mu$ m CMOS process.

#### VI. REFERENCES

- [1] J. L. Pennock, "CMOS triode transconductor for continuous-time active integrated filters," *Electronics Letters*, vol. 21, no. 18, pp. 817-818, 29<sup>th</sup> August 1985.
- [2] J. A. de Lima and C. Dualibe, "A linearly-tunable CMOS transconductor with improved common-mode stability and its application to gm-C filters," *IEEE TCASII*, vol.48, no.7, July 2001.