GENERAL PURPOSE FOLDED-CASCODE CMOS OPAMP DESIGN

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ABSTRACT

This paper presents a single-ended folded-cascode CMOS operational amplifier, designed for general purpose applications. Primary specifications are a gain better than 80dB, GBW of 10MHz, systematic offset lower than 200µV, THD less that 0.1% at 3.5Vpp output and a load of 20pF, operating with a single supply voltage of 5V. The circuit was fabricated using AMIS 1.5um technology, available from MOSIS through the Educational Program.

1. INTRODUCTION

Operational amplifiers are one of the many basic building blocks in analog design. This paper presents a methodology for an opamp design with load capacitance using the ACM (Advanced Compact Mosfet Model) equations. The folded-cascode configuration was chosen because it improves common-mode input range and increases the output swing [1] if compared to the conventional cascode amplifier. This paper is divided as follows. In Section 2, we describe the circuit and its operation. In Section 3, we present the methodology employed to determine the size of the transistors using the ACM equations [2,3]. In Section 4, we present a comparison between theoretical, simulation and experimental results. We finish the paper with the conclusions, in Section 5.

2. CIRCUIT DESCRIPTION AND OPERATION

The topology used for the folded-cascode opamp is shown in figure 1. Bias voltages, indicated in figure 1, were designed according to [4], in a way such that the transistors are biased in the edge of saturation.

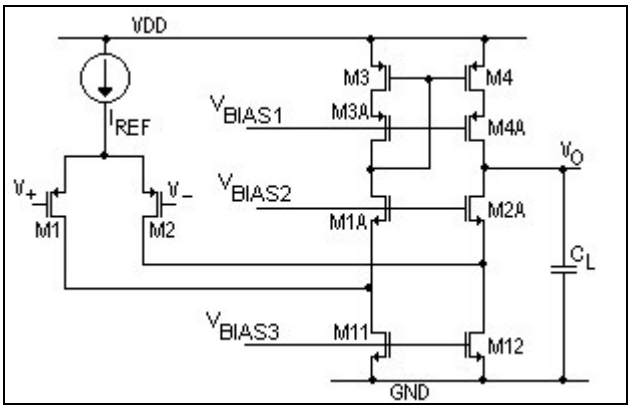

Figure 1: Opamp circuit

The off-chip reference current source, I_{REF}, is used to bias the input differential pair formed by M1-M2. V_{BIAS3} provides a voltage to M11-M12 in a way that they work as two current sources for the folded-cascode topology. M1A and M2A are connected in a common-gate configuration with V_{BIAS2} and are part of the folded-cascode output stage. M3, M3A, M4 and M4A form a low-voltage cascode current mirror biased by V_{BIAS1}. C_L is the load capacitance.

With equal voltages at the input nodes V_+ and V_-, the current in each transistor of the differential pair is half the reference current. When V_+ is higher than V_-, the current in M1 becomes higher than in M2. Since M11 and M12 form two current sources, the difference in the current in M1A and M2A is compensated with an increase in the drain-source voltage of M2A and, consequently, in the output voltage. Similar analysis can be made when V_+ is lower than V_- when the output voltage falls.

3. DESIGN METHODOLOGY

Expression (1) gives the relation between the bandwidth, GBW, and the gate transconductance, g_{mg}, according to the load capacitance [1]. With GBW of 10MHz, the g_{mg} is 1.26mA/V.

$$g_{mg} = 2\pi \cdot GBW \cdot C_L \tag{1}$$

For a proper operation, all the transistors must be in saturation [1]. In this situation, the drain current, I_D, and the forward inversion level, i_f, in the differential pair are related with the gate transconductance by [2,3]

$$g_{mg} = \frac{2 \cdot I_D \left(\sqrt{1 + i_f} - 1 \right)}{n \cdot \phi_T \cdot i_f} \tag{2}$$

where n is the slope factor and $\ddot{O}_T$ is the thermal voltage. We choose I_D=120µA to limit power consumption and i_f=33 not to make M1 and M2 so large, because i_f and the aspect ratio are inversely proportional, as will be shown later. Since that all the current in these transistors is provided from the reference current, we have I_{REF}=240µA. M11 and M12 work as current sources, and we make them equal to I_{REF}. So, the currents that flow in the transistors M1A-M3A-M3 and M2A-M4A-M4 is the same as in the differential pair.

M3 and M4, M3A and M4A, M1A and M2A and M11 and M12 must be saturated, within a 3.5Vpp output signal. So their saturation voltage, V_{DSSAT}, given by (3) [2,3], must be lower than 375mV. In order to avoid the effects of process parameters variation, we choose i_f=100.

$$V_{DSSAT} = \phi_T \cdot \left(\sqrt{1+i_f} + 3\right) \quad (3)$$

The aspect ratio, W/L, of each transistor can be determined by expression (4) that relates the drain current in saturation, technological parameters and the forward inversion level [2,3].

$$I_D = i_f \cdot \mu \cdot n \cdot C'_{ox} \cdot \frac{\phi_T^2}{2} \frac{W}{L} \quad (4)$$

ì is the carrier mobility, n is the slope factor, C'$_{ox}$ is the oxide capacitance/area.

Table 1 summarizes drain currents, inversion levels, aspect ratios, widths and lengths for all transistors. The final length was chosen with help of simulations, in order to avoid short channel effects, to achieve the specified gain and to reduce the output offset voltage.

	i_f	I_D (µA)	W/L	W (µm)	L (µm)
M1, M2	33	120	360	1440	4
M1A, M2A	135	120	62.5	400	6.4
M3, M4, M3A, M4A	100	120	120	480	4
M11, M12	68	240	62.5	400	6.4

Table 1: Transistors' sizes

4. RESULTS

The circuit was fabricated with the AMIS 1.5µm, available from MOSIS through the Educational Program. Theoretical, simulation and experimental results in three different chips were compared to assess the opamp design. Due to limitations of the measurement equipment, the load capacitance was set to 26pF. In order to provide compatible results, simulations were also done with this load. Table 2 summarize them.

Operating point and DC transfer simulations were made in order to determine the linearity, the offset and power consumption. First, the opamp was connected in the follower configuration in order to determine the output voltage range for which THD<0.1%. Offset was measured with both inputs shorted and set to 2.5V. It was, then, referenced to the input.

Slew-rate, SR, is determined by the maximum variation of the output voltage in a period of time, and is given by the ratio of the available current, I_{REF}, and the load capacitance. Transient analysis was made to determine it with a 2Vpp input square signal around the operating point.

Frequency response was carried out to verify the performance achieved by the opamp by means of small-signal simulations and theoretical formulations from the equivalent circuit. Each transistor was substituted by its model, to determine the gain at low frequencies, the dominant pole, transition frequency, f_T, and phase margin. The DC gain, A_{VO}, is given by

$$A_{VO} = g_{mg} \cdot R_O \quad (5)$$

where R_O is the output resistance, approximated by

$$R_O \approx \left[\frac{g_{ds2A} \cdot (g_{ds12} + g_{ds2})}{g_{ms2A}} + \frac{g_{ds4A} \cdot g_{ds4}}{g_{ms4}} \right]^{-1} \quad (6)$$

g_{ds} is the output transconductance and g_{ms} is the source transconductance.

	Theoretical	Simulation*	Measurements*
Output voltage for THD<0.1%	3.75Vpp	3.7 Vpp	3.84 Vpp
Offset	105 µV	122 µV	150-650 µV
Power	2.64 mW	2.6 mW	2.6 mW
Slew-rate	12 V/µs	7.2 V/µs	5.3-5.7 V/µs
A_{VO}	81 dB	82 dB	72-73 dB
Dominant pole	881 Hz	644 Hz	-
f_T	10.3 MHz	7.8 MHz	7.2 MHz
Phase Margin	68°	70°	66-68°
Settling time large @ 0.1%	170 ns	250 ns	244-250 ns
Settling time small @ 1%	180 ns	150 ns	162-168 ns

Table 2: Results (* C_L=26pF)

Figure 2 shows the layout of the operational amplifier integrated circuit.

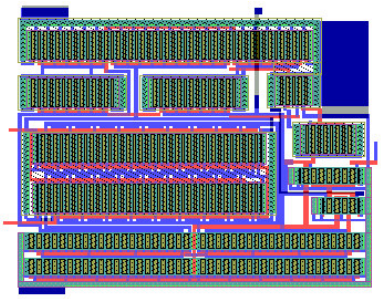

Figure 2: Layout of the opamp

5. CONCLUSIONS

The design of a general purpose folded-cascode operational amplifier using ACM equations was shown here. Experimental results were compared with theoretical and simulated ones and showed that they agreed very well.

6. REFERENCES

[1] Gray, P., Hurst, P., Lewis, S., Meyer, R., Analysis and Design of Analog integrated Circuits, *John Wiley & Sons, Inc., Fourth Edition.*

[2] A. I. Cunha, M. C. Schneider, C. Galup-Montoro, "An MOS transistor Model for analog circuit design", *IEEE J. Solid-State Circuits, vol. 33, pp. 1510-1519, Oct. 1998.*

[3] C. Galup-Montoro, M. C. Schneider, A. I. Cunha, "A current-based MOSFET model for integrated circuit design", in Low-Voltage/Low-power Integrated Circuits and Systems, *E. Sánchez-Sinencio and A. G. Andreou, Eds. New York: IEEE Press, 1999.*

[4] Johns, D., Martin K., Analog Integrated Circuit Design, *John Wiley & Sons, Inc., 1997.*