DESIGNING TWO PARALLEL MULTIPLIER ARCHITECTURES FOR DSP

Leomar S. Rosa Jr., Marcos R. Boschetti, Émerson B. Hernandez, André B. Soares, Eduardo Costa[†]*, Sergio Bampi.*

Instituto de Informática – Universidade Federal do Rio Grande do Sul (UFRGS)
[†]UCPEL – Univ. Católica de Pelotas
P O Box 15.064 – 91.501-970 – Porto Alegre – RS – Brazil
{leomarjr, marcosrb, barbieri, borin, bampi}@inf.ufrgs.br

ABSTRACT

This paper investigates an implementation of two different multiplier architectures for DSP applications, like multiply-accumulate(MAC). The Baugh-Wooley and Hybrid multipliers were developed and laid out in a 0,35µm technology using the Cadence tool set with some preliminary results showing area overhead.

1. INTRODUCTION

Modern digital systems have an increasing demand for computational power. Even ordinary portable devices as cell phones and personal assistants need to perform complex and computing intensive algorithms [1].

A key module present in these circuits datapaths is the integer multiplier. As an example, a common operation in many digital signal processing applications is the multiply-accumulate (MAC). Then, the design of efficient integer multiplier architectures is essential for DSP datapaths. This paper is divided as follows: section 2 presents the two architectures studied in this work. Section 3, the design flow used in the development from the logical level to physical implementation. Section 4 shows some comparative results while section 5 draws final conclusions and future works.

2. MULTIPLIER ARCHITECTURES

In this section we present two different approaches for a 16 x 16 bit multiplier in 2´s complement. The first one is the well known Baugh-Wooley [2] [3], an interesting implementation case, since it leads to very regular designs. The second architecture is the hybrid array multiplier, introduced in [4] [5], that operates on an hybrid binary-gray encoding, which is designed specially to offer low-power consumption for correlated input operands.

2.1. Baugh-Wooley Architecture

The algorithm for direct 2's complement array multiplication has been proposed by Baugh and Wooley. The primary advantage of this algorithm is that the signs of all the partial products are positive, and thus allowing the array to be similar to conventional standard array structures.

2.2. Hybrid-coded array multiplier

The parallel multiplication operation is performed from additions of partial products sequences with basic 2bx2b multiplier modules, to reduce by 2 the number of partial products. Each two-bit group (m=2) in the operand is Gray-coded. These partial products are generated by intermediary multiplication cells and carry is propagated to each individual group.

3. DESIGN FLOW

The first step is the definition of the basic building blocks of each multiplier. Baugh-Wooley is divided in five regular blocks that define the basic structures, while the Hybrid multiplier is composed by three different types of 2bx2b multiplier full-custom logic, comprising unsigned and signed multiplication blocks. Electrical optimizations, use of complex gates and regular layout were done for the basic blocks. SPICE simulations of all these blocks (1,2, 3,4, 5, and F=full adder in Fig. 1) were done.

3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
3	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	
3	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	
3	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	
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3	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	
5	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	
F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

Figure 1 – Baugh-Wooley Floorplan

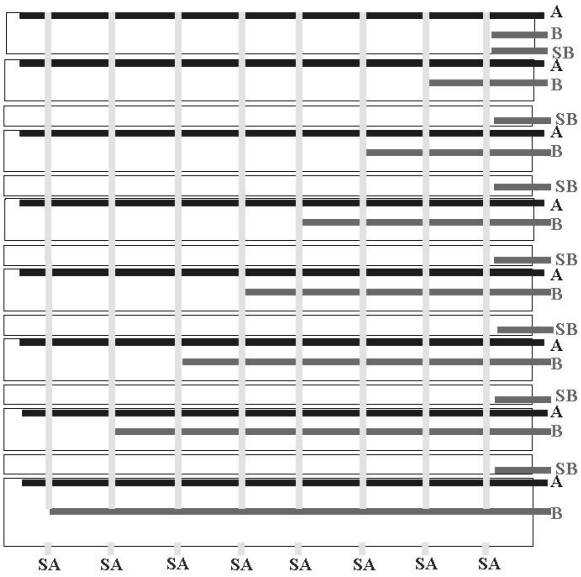

Figure 2 – Hybrid Floorplan

Both architectures have hierarchical and regular constructions, allowing the compact floorplanning shown in figures 1 and 2.

4. RESULTS

Full custom layout results show a larger silicon usage for the Baugh-Wooley multiplier, as we can compare on figures 3 and 4. However, the designer's experience demonstrated that the regularity of the Baugh-Wooley was key to allow an easier and faster layout, compared to the hybrid one. Table 1 compares the area and total number of transistors for both architectures. The Cadence tool set was used, namely the Virtuoso tool for layout, and the Spectre electrical simulator for validation purposes. Switch level simulation results at gate level were done previously [6]. An UltraSparc II, 296MHz, running SunOS Release 5.7 with 256 Mb RAM, 33 Mhz PCI, was used for circuit extraction (CET data, Table 1).

Table 1 – Preliminary Results

Architectures	Area (μm^2)	Transistors	CET time
Baugh-Wooley	527.800	9.862	28min 47s
Hybrid	336.517	9.228	23min 19s

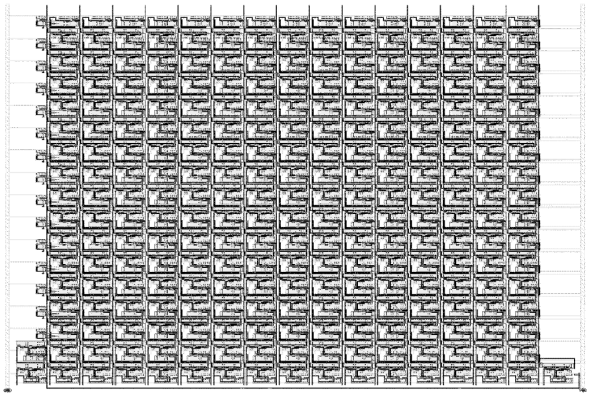

Figure 3 – Baugh-Wooley Layout

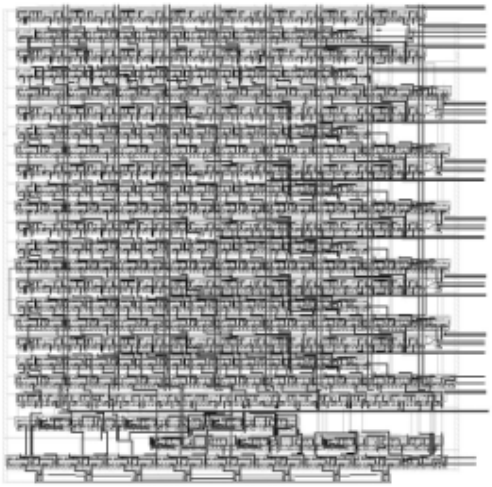

Figure 4 – Hybrid Layout

5. CONCLUSIONS

This paper presented the development of two different architectures for 16-bit multiplication. The area used by the Baugh-Wooley is 56% larger than the hybrid. The regularity is an advantage of the former. Delay and power comparisons are addressed in future work, in which carry speed-up is addressed. It is important to identify the approach best suited for the specific DSP design requirement (low power, high performance). The hybrid array multiplier with m=2 is a good choice for low power designs as shown in [5].

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